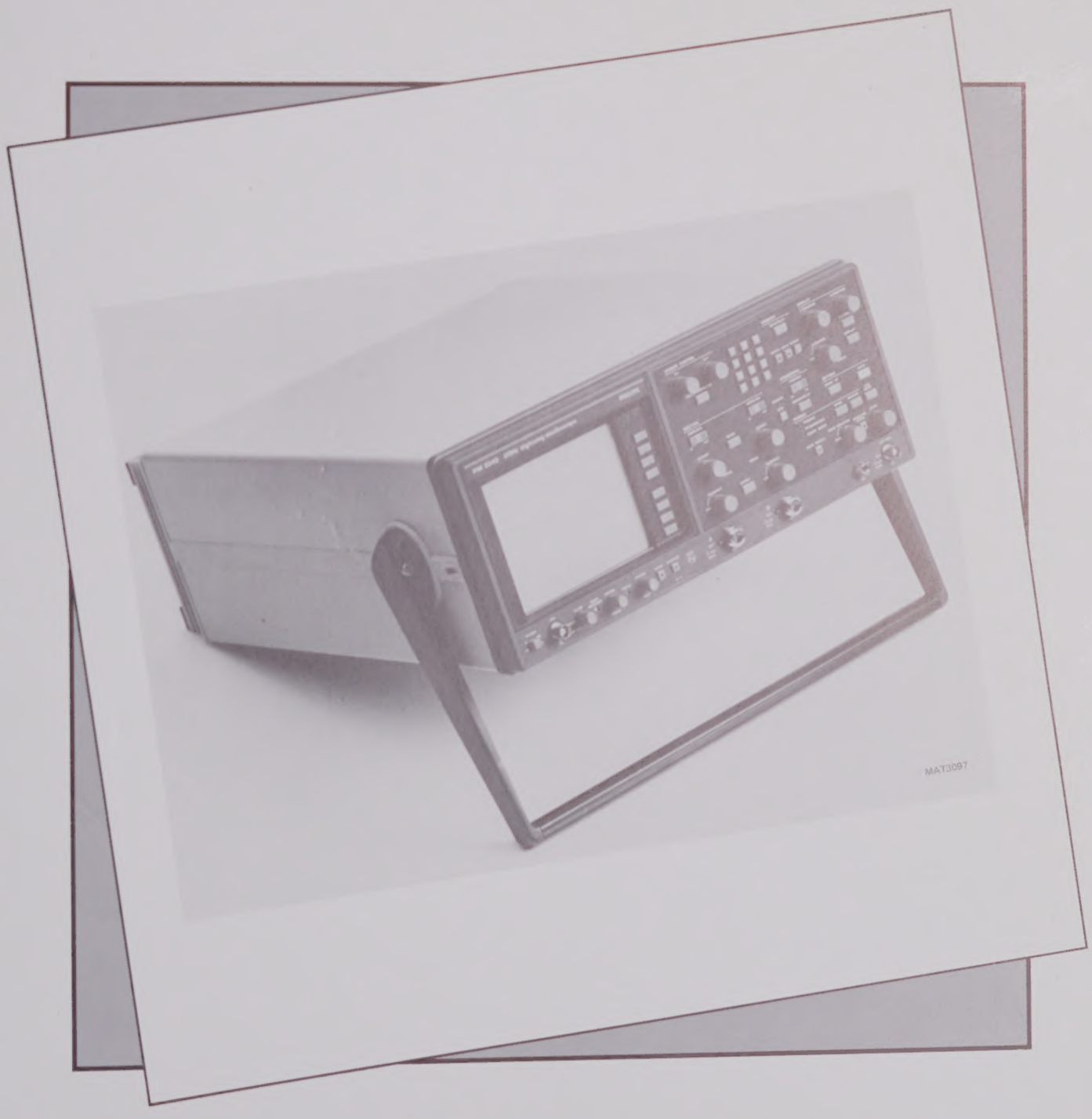
PHILIPS

2 GHz Digitizing Oscilloscope
PM3340

TEST & MEASUREMENT

CUSTOMER SUPPORT



4822 872 05325
880601

Service Manual

MOORE

2 GHz Digitizing Oscilloscope

PM3340

Service Manual

4822 872 05325
880601

WARNING: These servicing instructions are for use by qualified personnel only. To avoid electric shock do not perform any servicing other than that contained in the Operating Instructions unless you are fully qualified to do so.

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IMPORTANT

In correspondence concerning this instrument please quote the typenumber and serial number as given on the type plate.

NOTE: *The design of this instrument is subject to continuous development and improvement. Consequently, this instrument may incorporate minor changes in detail from the information contained in this manual.*

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SAFETY INSTRUCTIONS

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1.0 SAFETY INSTRUCTIONS

Read these pages carefully before installation and use of the instrument.

1.1 INTRODUCTION

The following clauses contain information, cautions and warnings which must be followed to ensure safe operation and to retain the instrument in a safe condition.
Adjustment, maintenance and repair of the instrument shall be carried out only by qualified personnel.

1.2 SAFETY PRECAUTIONS

For the correct and safe use of this instrument it is essential that both operating and servicing personnel follow generally-accepted safety procedures in addition to the safety precautions specified in this manual.
Specific warning and caution statements, where they apply, will be found throughout the manual.
Where necessary, the warning and caution statements and/or symbols are marked on the apparatus.

1.3 CAUTION AND WARNING STATEMENTS

CAUTION: Is used to indicate correct operating or maintenance procedures in order to prevent damage to or destruction of the equipment or other property.

WARNING: Calls attention to a potential danger that requires correct procedures or practices in order to prevent personal injury.

1.4 SYMBOLS

High voltage ≥ 1000 V (red)

Live part (black/yellow)

Read the operating instructions

Protective earth (grounding) terminal (black)

1.5 IMPAIRED SAFETY PROTECTION

Whenever it is likely that safety-protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation. The matter should then be referred to qualified technicians.
Safety protection is likely to be impaired if, for example, the instrument fails to perform the intended measurements or shows visible damage.

1.6 GENERAL CLAUSES

1.6.1 WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts and accessible terminals which can be dangerous to live.

1.6.2 The instrument shall be disconnected from all voltage sources before it is opened.

1.6.3 Bear in mind that capacitors inside the instrument can hold their charge even if the instrument has been separated from all voltage sources.

1.6.4 WARNING: Any interruption of the protective earth conductor inside or outside the instrument, or disconnection of the protective earth terminal, is likely to make the instrument dangerous.
Intentional interruption is prohibited.

1.6.5 Components which are important for the safety of the instrument may only be renewed by components obtained through your local PHILIPS organisation. (See also chapter 12).

1.6.6 After repair and maintenance in the primary circuit, safety inspection and tests, as mentioned in chapter 14 have to be performed.

INTRODUCTION 2

INTRODUCTION

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2.0 INTRODUCTION

This dual channel digitizing storage oscilloscope features sampling techniques that allow display of signals with a frequency up to 2 GHz. The sampling system can operate in normal and in high resolution eye pattern mode.
The instrument is extremely easy to use because of the AUTO-SET pushbutton, which automatically sets the various controls of the instrument to suit the input signal value.
The brightness is independent of the time base settings.
The M68000 microprocessor gives a wide choise of measurement and display possibilities, which can be selected via the ergonomic designed front panel.

Figure 2.1 2 GHz digitizing oscilloscope.

The oscilloscope is provided with integrated circuits, which guarantee highly-stable operation.

Furthermore, connection to the local mains is simplified by a tapless switched-mode power supply that covers most voltage ranges in use: 90 V...264 V a.c.

All these features make this oscilloscope suitable for a wide range of high-frequency measuring applications, such as in telecomunnications, component testing and development of fast computers.

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CHARACTERISTICS

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3.0 CHARACTERISTICS

General

This instrument has been designed and tested in accordance with IEC publication 348 for Class I instruments.
This specification is valid after the instrument has warmed up for 30 minutes.

Properties expressed in numerical values with tolerances stated, are guaranteed by the manufacturer.
Numerical values without tolerances or limits are typical and represent the characteristics of an average instrument.
For definition of terms, reference is made to IEC publications 351, 395 and 548.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.1	CATHODE RAY TUBE		
3.1.1	Type	Philips D18-190GH/129	180 mm rectangular single beam tube.
3.1.2	Usefull screen area (h. x w.)	100 mm x 120 mm	For graticule see 3.1.7.
3.1.3	Screen type	GH (P31)	
3.1.4	Total accelera-tion voltage	16 kV	
3.1.5	Spot size	0,3 mm	Tube only.
3.1.6	Maximum trace distortion		Deviation from straight line.
	-@ screen periphery	1 mm	Outside central 80 mm (vert.) x 100 mm (hor.)
3.1.7	Graticule	Internal, fixed	
	-Illumination	Continuously variable	
	-Size (h. x w.)	80 mm x 100 mm	Centered @ 50 mm from top of CRT screen (hor.) and @ 50 mm from left edge of CRT screen (vert.).
	-Engravings		
	division lines	@ 10 mm	Horizontal and vertical.
	2 mm tick marks	@ 2 mm	On vertical and horizontal central axes.
	0.5 mm tick marks	@ 2 mm	On horizontal lines # 2,3,4,6,7,8.
	dots	@ 2 mm	On dotted lines @ 1,5 div. and 6,5 div. from top of graticule.
	percentages	100-90-10-0 %	To facilitate rise and fall time measurements.
3.1.8	Orthogonality	$90 \pm 0{,}5^{o}$	Measured @ centre of screen. (Angle between X and Y axes, when traces are written in X and Y direction alternately).
3.1.9	Intensity	Blank to max. intensity	Separate front panel controls for trace and text.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.1.10	Focus	Manually set	Common screwdriver control on front for trace and text.
3.1.11	Trace rotation		Screwdriver control on front; direction of screwdriver rotation same as direction of trace rotation.
	-Minimum range	14^{o}	Either X or Y trace can be aligned with graticule, when environmental magnetic field is within 0,1 mT.
3.2	SIGNAL ACQUISITION		
3.2.1	Sampling type	Equivalent time	Sequential sampling
3.2.2	Sources	Channel A Channel B	
3.2.3	Modes		Both channels sampled simultaneously.
	-Source select	Single channel Dual channel Added	
	-Polarity	Inverted Non inverted	Each channel can independently be inverted.
	-Processing	Eye-pattern Average Multiple sampling Absolute Min/Max	} Channels simultaneously in Single and Dual mode
3.2.4	Range		
	-Vertical		
	Single channel Dual channel Added	} 10 div	Signal A and Signal B (including offset) and Added signal should remain within screen. Overflow signal A or B indicated in Added signal.
	-Horizontal	10,2 x time/div	Display in unmagnified position.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.2.5	Resolution		
	-Vertical	1:1024	10 Bits
	-Horizontal	64...512 sampl./acq.	Both channels have same resolution
	Normal display	512 sampl./acq. 256 sampl./acq. 128 sampl./acq.	
	Fast display	64 sampl./acq.	
	Eye pattern		
	-Single Channel	4096 sampl./acq.	Acquired over 512 positions.
	-Dual Channel	2048 sampl./acq.	Each Channel, acquired over 512 positions.
3.2.6	Minimum Acquisition time		Acquisition time = Hor. Resolution x sample processing time.
	-512 sampl/acq. - 64 sampl/acq.	< 25 ms < 10 ms	} Minimum acquisition time } supposes trigger delay = } zero and hold off time = } minimum.
3.2.7	Max. time difference between Channels	35 ps	
3.3	CHANNELS A AND B		
3.3.1	Input connector	N-type With probe read out	Probe read out causes instrument to change V/div indication (when probe fitted with a probe indicator).
3.3.2	Input impedance	50 ohm $\pm$ 1%	
	-Max. VSWR		
	Upto 1 GHz	1:1,3	Referred to Z_o = 50 ohm
	Upto 2 GHz	1:1,4	Referred to Z_o = 50 ohm
3.3.3	Input coupling	d.c.	
3.3.4	Spurious emission		
	-Max. strobe emission (pk...pk)	< 100 mV	
	-Max. trigger emission (pk...pk)	< 100 mV	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.3.5	Max. non destructive input voltage		
	-d.c.	5 V	
	-a.c. (r.m.s.)	5 V	
	-a.c. (peak)	5 V	
3.3.6	Deflection coefficient		
	-Steps		
	Normal modes	1 mV/div...200 mV/div	In 1-2-5 sequence of 8 steps.
	Limits of error (Ambient 15...35°C)		After first hor. div. Add 1,5% for ambient: 0...50°C.
	-Up to memory	± 1,5%	} Error limit input
	-Overall	± 1,5%	} impedance excluded
	-Eye pattern mode	5 mV/div...200 mV/div	In 1-2-5 sequence of 6 steps.
	Limits of error (Ambient 15...35°C)		Add 5% for ambient: 0...50°C.
	-Up to memory	± 10%	
	-Overall	± 10%	
	-Vernier		
	Ratio	3,0 : 1	
	Resolution	1 : 4096	12 Bits
	Limits of error	± 3%	
3.3.7	Dynamic range	±0,8 V	Center of dynamic range can be positioned by d.c. Offset control. Compression at limits of dynamic range: In normal mode less than 1% In eye pattern mode less than 5%.
3.3.8	D.C. offset		
	-Range	± 1,6 V	
	-Resolution	0,01 div.	
3.3.9	Frequency response	d.c....2,0 GHz	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.3.10	Pulse response		
	-Rise time (Ambient 15...35°C	175 ps or less	Tested with a 70 ps rise time pulse. Calculated from Bandwith x Risetime=0,35. Add max. 25 ps for ambient: 0...50°C.
	-Aberrations		
	Overshoot	4% or less	
	Tilt	2% or less	
	Ringing after transient	4% or less	
3.3.11	Visible signal delay	9 ns	
3.3.12	Max. base line instability		
	-Jump (Ambient 15...35°C)		Conditions: No signal at inputs A and B. Offset channel A is zero. Offset channel B is zero. Add 100% for Ambient: 0...50°C.
	When switching to ADD mode	0,3 div	
	When switching from 5 mV/div to 200 mV/div position	0,4 div	
	When using invertor switch	0,5 div	Variable vernier is cal. position
	When rotating vernier	0,25 div	
	When switching from 20 us/div to 1 ns/div in 5 mV/div	0,6 div	
	-Drift	< 1 mV/h	
	-Termperature coefficient	< 1 mV/K	Measured in 5 mV/div.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.3.13	Common mode rejection ratio		} Both channels at same } attenuator setting; } vernier of V/div
	-Up to 100 MHz	40:1	} adjusted for best CMMR.
	-Up to 500 MHZ	10:1	} Measured with max. 8 div } input at each channel } (± 4 div around zero).
3.3.14	Minimum channel isolation	1000:1	Measured with full scale input signal in 200 mV/div.
3.3.15	Maximum noise	0,5 mV (RMS)	In 1 mV/div and 2 mV/div automatic smoothing.
3.3.16	Average		Average formula after the first front change: Si(N)=Si(N-1)+ (Si(N)-Si(N-1))/C i-th sample; N-th sweep; C is average constant.
	-Average constant C	2...64	In powers of 2.
	-Smooth	C=4	
3.3.17	Multiple sampling		Number of samples at each position is selectable in powers of 2.
	-Number of sampling	1...32	

3

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.4	TRIGGERING		
3.4.1	Sources		
	-Internal	A, B	
	Coupling	a.c. (150 kHz, -3dB)	Time constant: 1 us.
	-External	EXT	
	Input connector	BNC	
	Input impedance	50 ohm ± 1%	
	Coupling	a.c. (150 kHz, -3dB)	Time constant: 1 us.
	Max. non-destructive input voltage	± 5 V	
3.4.2	Modes		
	-Manual	TRIGGER SYNCRONIZE COUNTDOWN	
	-AUTO	AUTO SELECT	Selects automatically between TRIGGER, SYNCHRONIZE, COUNT DOWN and SENS HIGH or LOW, depending on input frequency and amplitude.
3.4.3	Sensitivity (peak to peak) (Ambient 15...35°C)		Min. signal required is equal or less than indicated values. Add 10% for 0...50°C.
	-TRIGGER mode		
	SENS HIGH		
	-Up to 100 MHz	10 mV	
	-Up to 200 MHz	20 mV	
	SENS LOW		
	-Up to 100 MHz	100 mV	
	-Up to 200 MHz	200 mV	
	-SYNCHRONIZE mode	2 mV	Up to 100 MHz.
	-COUNT DOWN mode		See figure 3.1.
	SENS HIGH	50 mV	
	SENS LOW	200 mV	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.4.4	Dynamic Range		
	-TRIGGER mode		
	SENS HIGH	200 mV	
	SENS LOW	2 V	
	-SYNCHRONIZE mode	100 mV	
	-COUNT DOWN mode		
	SENS HIGH	200 mV	
	SENS LOW	2 V	
3.4.5	FREQUENCY RANGE		
	-TRIGGER MODE		
	Max. trigger frequency	> 200 MHz	
	-SYNCHRONIZE mode		
	Max. synchronize frequency	> 100 MHz	
	-COUNT DOWN mode		
	Min. count down frequency	< 160 MHz	
	Max. count down frequency	> 2 GHz	
3.4.6	Level		
	-Range		
	SENS HIGH	$\pm$ 4 mV	
	SENS LOW	$\pm$ 40 mV	
	-Resolution	1 : 16.384	14 Bits
3.4.7	Slope Selection		In TRIG mode (for COUNT DOWN, SYNC only positive going).
		Positive going (+) Negative going (-)	
3.4.8	Jitter	< 7 ps (RMS)	Time-base of 1 ns/div.

3

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.5	TIME BASE		
3.5.1	Acquisition modes	Recurrent Single scan Multiple scan Multiple eye Save/Stop on Difference	
3.5.2	Deflection coefficient		
	-Time-base steps	1 ns/div...20 us/div	In a 1-2-5 sequence.
	Limits of error (Ambient 15...35°C)	± 3%	Measured between + and - 4 div from graticule center. Add 0,5% of full scale for ambient 0...50°C.
	-Magnifier steps	x1...x50	In a 1-2-5 sequence.
	Limits of error	add 2%	to time-base limits of error.
3.5.3	Delay		
	-Range		
	20 ns/div... 20 us/div	0...10 div	}
	10 ns/div	-1...9 div	}
	5 ns/div	-2...8 div	} Time-base magnifier: x1.
	2 ns/div	-4...5 div	}
	1 ns/div	-9...0 div	}
	-Resolution	1 div	
	-Limits of error	± 1 ns ± 3%	
3.5.4	Hold-off		
	-Range (approx.)		
	512 sampl./acq.	47 us...85 us	
	512 sampl./acq. and average	47 us...85 us	
	256 sampl./acq.	47 us...85 us	
	128 sampl./acq.	90 us...150 us	
	64 sampl./acq.	150 us...230 us	
	-Resolution	1 : 2048	11 bits

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.6	MEMORY		
3.6.1	Memory size		
	-Registers	4	Registers #0, #1, #2, #3
	-Register depth	4096 words	
	-Wordlength	10 bits	
3.6.2	Functions	Clear	Register #0 is cleared, and blanked if DOTS is selected.
		Save	Contents of register #0 is saved in selected register (#1, #2 or #3).
		Write	Acquired signal is written into register #0.
		Lock	Memory system is locked, including register #0.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.7	DISPLAY		
3.7.1	Sources	Register #0 Register #1 Register #2 Register #3	} } In any combination. } }
3.7.2	Display expansion		
	-Horizontal		
	Steps:	1x...64x	In Y versus t. In Eye Pattern only 1x.
		1x...8x	In A versus B In Eye Pattern only 1x.
	Vernier ratio	1:2 < V ratio	Continuously variable between steps. Recalculated value is displayed with an accuracy of ± 5 %.
	-Vertical		
	Steps	0.2x, 1x and 5x	Both in Y versus t and A versus B modes.
3.7.3	Display manipulations	Dot join	Linearly interpolated between measured dots.
		Invert	Any register can be inverted.
3.7.4	Position ranges		All channels can be positioned independently.
	-Horizontal	± 5 div	From screen centre.
	-Vertical	± 5 div	From screen centre.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.8	SETTING MEMORY		
3.8.1	Memory size	Max. 251 front settings	
3.8.2	Functions		
		Save	Actual settings are stored in memory, replacing contents of memory cell indicated on CRT.
		Insert	Actual settings are stored in memory; insertion is after memory cell indicated on CRT.
		Delete	Contents of memory cell indicated on CRT is deleted.
		Recall	Actual settings are replaced by contents of memory cell indicated on CRT. Actual settings are saved in "last setting" memory (= memory cell #0).
		(Recall) Next	Actual settings are replaced by contents of memory cell indicated on CRT increased by 1. Actual settings are saved in "last setting" memory (= memory cell #0).
		(Recall) Previous	Actual settings are replaced by contents of memory cell indicated on CRT decreased by 1. Actual settings are saved in "last setting" memory (= memory cell #0).

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.9	ANALYZE FACILITIES		
3.9.1	Measure		
	-Amplitude	RMS voltage	}} Including or excluding
		Mean voltage	}} offset voltage.
		Peak to Peak voltage	} Result calculated from
		Peak to Zero voltage	} part between cursors or
		Overshoot	} markers if LOCATE is
		Preshoot	} choosen.
	-Time	Risetime	
		Pulse width	
		Duty cycle	
		Frequency	
		Phase	
	-Mathematics	Add	}
		Substract	} Result of calculation
		Multiply	} displayed in selected
		Divide	} register and scalable
		Differentiate	} for optimum display.
		Integrate	}
		Delay Channel	}
		Histogram	Amplitude density versus absolute amplitude of an input signal.
		F.F.T.	
		Filter	
3.10	AUTO SETTING		
3.10.1	Setting time	Typical 3 s	During plot: AUTO SET not possible.
3.10.2	CRT functions		
	-Focus	}	
	-Trace intensity	} Not influenced	
	-Text intensity	}	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.10.3	Display functions		
	-Select	To register #0	
	-X-position	Zero	
	-Y-position	Zero	
	-Invert	Off	Only for register #0.
	-X-expand	x1	Vernier calibrated.
	-Y-expand	x1	
	-A versus B	Off	Only for register #0.
	-Dots	Joined	
3.10.4	Cursors	Off	
	-Calculation	Off	
3.10.5	Text		
	-Reduced	Off	
	-Bottom text lines	Not affected	
3.10.6	Vertical acquisition		
	-Y-deflection source	Every source having a triggerable signal at its input	Channel A if no trigger is found.
	-Y-deflection coefficient		Each channel is independently set.
	Input voltage > 10 mV	Approx. 4 div	
	Input voltage < 10 mV	Channel at 5 mV/div	} Vernier in calibrated } position.
	-Modes		
	Invert	Off	
	Add	Off	
	Average	Off	
	Eye pattern	Off	
	Multiple sampling	Off	
	-Offset	Zero	
	-Y baseline position		
	In single channel display	Centre of screen $\pm$ 0,3 div	
	In dual channel display		
	-Ch. A	2 $\pm$ 0,3 div above centre screen	
	-Ch. B	2 $\pm$ 0,3 div below centre screen	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.10.7	Horizontal acquisition		
	-Mode	Recurrent 512 sampl./acq.	
	-TB deflection coefficient		
	80 kHz < signal freq. < 2 GHz	Min. 2, max 6 signal periods over 10 div	
	When no trigger found	100 ns/div	
3.10.8	Triggering		
	-Delay	Off	
	-Source		
	Triggerable signal at EXT	Ext	If Extern was selected.
	No trig. signal at EXT but trig. signal at channel A or B	Channel A or B	Channel with lowest input frequency is selected. Default: Channel A.
	No triggerable signal at any input	Channel A	
	-Mode	AUTO SELECT	
	-Level	Zero	
	-Slope	Positive going	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.11	CURSORS		
3.11.1	Cursor intensity control	Independent of trace intensity but combined with text intensity	
3.11.2	Resolution		
	-Horizontal	1:512	
	-Vertical	1:1024	
	-Read out	3 digits	
3.11.3	Voltage cursors		
	-Limits of error (Ambient 15...35°C)	± 1,5%	Referred to input at N-connector, error of probes etc. excluded. Add 3% for ambient: 0...50°C.
	-Cursor Range	Visible part of signal	Cursors cannot pass each other (to avoid negative readings).
3.11.4	Time cursors		
	-Limits of error	±3%	
3.12	CALIBRATOR		
3.12.1	Wave form		
	-Shape	Square wave	
	-Duty cycle	50 ± 0,01%	
	-Rise time (Ambient 15...35°C)	< 1,5 ns	Add 0,4 ns for ambient 0...50°C.
	-Max. overshoot and ringing	± 3%	
3.12.2	Output		
	-Connector	BNC	
	-Impedance	50 ohm ± 1%	
	-Voltage (peak to peak)	1V ± 1%	Into 50 ohm.
	-Current	20 mA ± 2 %	Into 50 ohm.
	-Frequency	100 kHz ± 0,1%	

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	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.13	POWER SUPPLY		
3.13.1	Source voltage a.c. (r.m.s)		
	-Nominal	100 V...240 V	
	-Limits of operation	90 V...264 V	
3.13.2	Source frequency		
	-Nominal	50 Hz...400 Hz	
	-Limits of operation	45 Hz...440 Hz	
3.13.3	Source waveform characteristics		@ Nominal source voltage.
	-Max. waveform deviation factors	10%	
	-Max. Total Harmonics	10%	
	-Max. Individual harmonic	5%	
	-Crest Factor	1,27...1,56	
3.13.4	Allowable power source interruption	At least 20 ms	@ Nominal source voltage. After this time oscilloscope settings are saved before instrument goes down. Automatic power up after restoration of Power line voltage. (For setting retention: see 3.15.1).
3.13.5	Power consumption (a.c. source)	135 W	@ Nominal Source Voltage

3.14 INTERFACES AND OPTIONS

For specification of interfaces and options refer to the separate manuals of these.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.15	SUNDRIES		
3.15.1	Data and settings retention		When instrument is switched off or during line power failure.
	-Memory back up voltage	2 V < MBUV < 3,5 V	
	-Memory back up current drain	Typical 12 uA	@ 25°C.
	-Recommended Batteries:		
	type	LR 6	According to IEC 285, (= Alkaline manganese penlight battery), e.g. PHILIPS LR6 (9299 000 20734) or DURACELL MN 1500.
	quantity	2 pcs	
	-Temperature rise of batteries	20°C	After warming up period of instrument.
	-Retention time	Typical 2 years	@ 25°C, with recommended (fresh) batteries.
	-Temperature Range	0...+70°C	@ -40...0°C settings retention is uncertain. It is advised to remove batteries from instrument when it is stored during longer periods (> 24 h) below -30°C or above 60°C. UNDER NO CIRCUMSTANCES BATTERIES SHOULD BE LEFT IN THE INSTRUMENT AT TEMPERATURES BEYOND THE RATED RANGE OF THE BATTERY SPECIFICATION.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.15.2	Probe Read Out		With Philips probe provided with indicator ring.
	-V/div read out		
	Passive 10:1 probe	10x higher	}
	Passive 10x attenuator	10x higher	}
	Passive 100:1 probe	100x higher	} Offset read out is changed accordingly.
	Passive 100x attenuator	100x higher	}
	-Cursor Read Out		
	Passive 10:1 probe	10x higher	
	Passive 10x attenuator	10x higher	
	Passive 100:1 probe	100x higher	
	Passive 100x attenuator	100x higher	
3.15.3	Analog plot output		
	-Connector	DIN 5 pole 45°	
	-Functions	Screen dump	Included channel identifiers.
		Memory dump	Register selectable.
	-Sensitivity	1 V/Full screen ± 3%	} Horizontal and vertical.
		1 V/Full memory ± 3%	}
	-Pen lift	TTL compatible	Pen-up is selectable (0 or 1). Open collector output; max. 12 V.
	-Plot time per dot	20 ms...2 s	Software selectable, signal dependent.
	-Plot order	Channel A first	In dual channel operation; with more registers starting with the lowest number.
	Registers	0,1,2,3	Skipping non selected register.
	Channels	A,B	Within one register, skipping non selected channel.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.16	MECHANICS		
3.16.1	Height		Fits 5E in 19 inch rack.
	-Without feet and accessory pouch	176 mm (6,9 inch)	Add 15 mm (0,6 inch) for feet.
	-Feet and accessory pouch included	250 mm (9,8 inch)	
3.16.2	Width without handle	419 mm (16,5 inch)	Add 46 mm (1,8 inch) for handle.
3.16.3	Depth		
	-Handle excluded	570 mm (22,5 inch)	Add 35 mm (1,4 inch) for protective cover.
	-With extended handle	670 mm (26,4 inch)	
3.16.4	Mass	18,7 kg	
3.16.5	Operating position	Horizontal	Standing on feet; may be tilted by handle.
		Vertical	Standing on rear feet.
		Tilt	By means of tilt boil handle.
	-Maximum stock pile	3	
3.16.6	Finish	Epoxy powder coated	
3.16.7	Printed circuit boards	Glass laminate epoxy	
3.16.8	Cooling	Fan aided convection	Maintenance free.

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.17	ENVIRONMENTAL		
3.17.1	General		
	The characteristics are valid if instrument is checked in accordance with the official checking procedure. Details on these procedures and failure criteria are supplied on request.		
3.17.2	Meets environmental requirements of:	MIL-T-28800D Type III Class 5, Style D	
3.17.3	Temperature		Memory back-up batteries removed from instrument, unless batteries meet temperature specifications (see also 3.15.1).
	-Operating		
	Min. low temperature	0°C	Cf. MIL-T-28800D par. 3.9.2.3 tested cf. par. 4.5.5.1.1.
	Max. high temperature	+ 50°C	Cf. MIL-T-28800D par. 3.9.2.4 tested cf. par. 4.5.5.1.1.
	-Non operating (Storage)		
	Min. low temperature	-40°C	Cf. MIL-T-28800D par. 3.9.2.3 tested cf. par. 4.5.5.1.1.
	Max. high temperature	+ 75°C	Cf. MIL-T-28800D par. 3.9.2.4 tested cf. par. 4.5.5.1.1.
3.17.4	Maximum humidity		Cf. MIL-T-28800D par. 3.9.2.2 tested cf. par. 4.5.5.1.1.
	-Operating and non-operating (storage)	95% Relative humidity	
3.17.5	Recovery time	2 h	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.17.6	Maximum altitude		Cf. MIL-T-28800D par. 3.9.3 tested cf. par. 4.5.5.2. Memory Back-up batteries removed from instrument, unless batteries meet maximum altitude specs.
	-Operating	4,5 km (15000 feet)	Maximum operating temperature derated 3°C for each km (for each 3000 feet) above sea level.
	-Non-operating (storage)	12 km (40000 feet)	
3.17.7	Vibration (operating)		Cf. MIL-T-28800D par. 3.9.4.1 tested cf. par. 4.5.5.3.1.
	-Freq. 5...15 Hz		
	Sweep time	7 min	
	Excursion (pk to pk)	1,5 mm	
	Max. acceleration	7 m/s^2 (0,7 x g)	15 Hz
	-Freq. 15...25 Hz		
	Sweep time	3 min	
	Excursion (pk to pk)	1 mm	
	Max. acceleration	13 m/s^2 (1,3 x g)	25 Hz
	-Freq. 25...55 Hz		
	Sweep time	5 min	
	Excursion (pk to pk)	0,5 mm	
	Max. acceleration	30 m/s^2 (3,0 x g)	55 Hz
	-Resonance dwell	10 min	@ each resonance freq. (or @ 33 Hz if no resonance was found). Excursion cf. 3.17.7.
3.17.8	Shock (operating)		Cf. MIL-T-28800D par. 3.9.5.1 tested cf. par. 4.5.5.4.1.
	-Amount of shocks		
	-Total	18	
	-Each axis	6	(3 in each direction).
	Shock wave form	half sine wave	
	Duration	11 ms	
	Peak acceleration	300 m/s^2 (30 x g)	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.17.9	Bench handling		Cf. MIL-T-28800D par. 3.9.5.3 tested cf. par. 4.5.5.4.3.
	-Meets requirements of:	MIL-STD-810 method 516, proced. V	
3.17.10	Salt atmosphere		Cf. MIL-T-28800D par. 3.9.8.1 tested cf. par. 4.5.6.2.1.
	-Structural parts meet requirements of:	MIL-STD-810 method 509, proced. I salt solution 20%	
3.17.11	EMI (Electro magnetic interference) meets requirements of:	MIL-STD-461 Class B	Applicable requirements of Part 7: CE03, CE07, CS01, CS02, CS06, RE02, RS02, RS03.
		VDE 0871 and VDE 0875 Grenzwertklasse B	
3.17.12	Magnetic radiated susceptibility		Tested conforming IEC 351-1 par. 5.1.3.1.
	-Maximum deflection factor	7 mm/mT (0,7 mm/gauss)	Measured with instrument in a homogeneous magnetic field (in any direction with respect to instrument) with a flux intensity (peak to peak value) of 1,42 mT (14,2 gauss) and of symmetrical sine wave with a frequency of 45...66 Hz.
3.17.13	Packing		
	Meets requirements of:	NLN-L88	

	CHARACTERISTIC	SPECIFICATION	ADDITIONAL INFORMATION
3.17.14	Transportation		
	Meets requirements of:	AN-D628	
	-Packaged transportation drop Meets requirements of:	Nat. safe transp. ass. procedure 1A-B-2	
	-Packed transportation vibration Meets requirements of:	Nat. safe transp. ass. procedure 1A-B-1	
3.18	SAFETY		
3.18.1	Meets requirements of:	IEC 348 Class I VDE 0411 Class I UL 1244 CSA 556B	
3.18.2	Approvals	VDE 0411 (applied for)	When shipped with universal European plug.
		UL 1244 (applied for)	When shipped with North American power plug.
		CSA 556 (applied for)	When shipped with North American power plug.

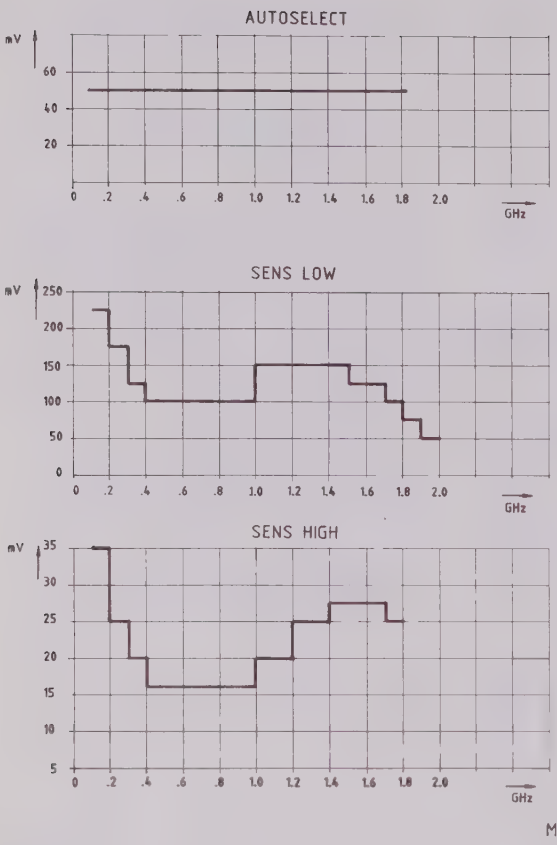

Figure 3.1 Trigger sensitivity count down

PERFORMANCE CHECK 4

PERFORMANCE CHECK

CONTENTS

4.0 Performance check..... 4-1
4.1 General information..... 4-1
4.2 Recommended test and calibration equipment..... 4-2
4.3 Preliminary settings..... 4-2
4.4 Checking procedure..... 4-3

4.0 PERFORMANCE CHECK

4.1 GENERAL INFORMATION

WARNING: Before switching-on, ensure that the instrument has been installed in accordance with the Installation Instructions outlined in chapter 3.0 of the Operating Manual.

This procedure is intended to:

- check the instrument's main specification points.
- be used for incoming inspection to determine the acceptability of newly purchased instruments and/or recently recalibrated instruments.
- check the necessity of recalibration after the specified recalibration intervals.

NOTE: The procedure does not check every facet of the instruments calibration; rather, it is concerned primarily with those parts of the instrument which are essential to measurement accuracy and correct operation. Removing the instrument covers is not necessary to perform this procedure. All checks are made from the outside of the instrument.

If the test is started within a short period after switching-on, bear in mind that steps may be out of specification, due to insufficient warming-up time.

Warming-up time under average conditions is 30 minutes.

The performance checks are made with a stable, well-focussed, low-intensity display. Unless otherwise noted, adjust the intensity and trigger-level controls as needed.

NOTES:

* At the start of every check, the controls always occupy the preliminary settings AUTO SET position, unless otherwise stated.

* The input voltage has to be supplied to the channel A input; unless otherwise stated.
  Unless otherwise stated, the switches TIME/DIV, OFFSET A and B, X-POSITION, TRACE INTENS and TEXT INTENS must be put in such a position that a good read-out of the phenomena of interest is obtained.

* Tolerances given are for the instrument under test and do not include test equipment error.

* The input impedance of 50 ohm of the oscilloscope under test is correct if the generator types are used that are given in chapter 13.1 "Recommended test and calibration equipment". If you use other types ofcalibration equipment, this may cause problems.

* For some checks, we make use of service routines. If you want additional information concerning these service routines refer to chapter 11 "Trouble shooting".

* In some checks in this chapter channel B is mentioned between brackets behind channel A. It is advised to perform the channel A checks first. After that the checks for channel B can be done.

4.2 RECOMMENDED TEST AND CALIBRATION EQUIPMENT

A complete list of all material necessary for both this performance check and also the adjusting procedure is given in chapter 9.2 in this manual.

4.3 PRELIMINARY SETTINGS

- Switch the oscilloscope on.
- Check that all the LED´s in the front panel are on for 1 sec. during the power up routine of the instrument´s microprocessor.
- Press AUTO.
- Check that after adjustment of TEXT INTENS and TRACE INTENS the read-out information and a horizontal line become visible at the CRT-screen.

4.4 CHECKING PROCEDURE

A. POWER SUPPLY

	IMPORTANT	The measurements of the power supply must be done with LIFE VOLTAGES. Therefore it is strongly advised to use a variable mains transformer with isolated primary and secondary windings. Nevertheless, these tests must only be done by a QUALIFIED TECHNICIAN who is aware of the danger involved.
A.1	SUBJECT	Mains voltage range.
	TEST EQUIPMENT	Variable mains voltage transformer (and digital multimeter)
	SETTINGS	- Connect the oscilloscope (switched off) to the output of the variable mains voltage transformer. If the transformer has no output voltage read-out, you must connect the digital multimeter (a.c. voltage range) to the outputs of the transformer. - Connect the variable mains transformer to the mains and adjust the output voltage.
	REQUIREMENTS	- Check that the oscilloscope starts up normally when switched-on at any voltage in the range 90...264 V (a.c). Preferred check points are 110, 220 and 240 V (a.c.).
	MEASURING RESULTS	.....
	SETTINGS	- Switch the oscilloscope on at a mains voltage between 90...264 V (a.c.). - Connect the input of Ch. A with the CAL voltage. - Press AUTO. - Adjust AMPL/DIV of Ch. A, TIME/DIV and other controls to a well-defined display of the CAL output voltage.

REQUIREMENTS

- Check that the display stays stable over the mains voltage range 90...264 V (a.c.).

MEASURING RESULTS .....

- Switch the oscilloscope off and disconnect the variable transformer from the mains.

A.2 SUBJECT

Mains voltage current.

TEST EQUIPMENT

Variable mains voltage transformer and digital multimeter.

SETTINGS

- Connect the oscilloscope to the variable mains transformer. In one of the mains conductors of the oscilloscope the digital multimeter (a.c. current range) must be present.
- Connect the transformer to the mains and switch the oscilloscope on. Graticule illumination must be on.

REQUIREMENTS

- Measure the current drain of the oscilloscope according to the table below (approximate rms value):

Mains voltage:	Current:
110 V (a.c.)	1,5 A
220 V (a.c.)	0,9 A
240 V (a.c.)	0,85 A

MEASURING RESULTS .....

Disconnect the variable mains transformer from the mains and connect the oscilloscope directly to the mains voltage.

B. C.R.T. DISPLAY SECTION

SUBJECT

Trace distortion.

TEST EQUIPMENT

L.f. sine-wave generator.

SETTINGS

- Press AUTO.
- Shift the Ch. A trace in the vertical mid of the screen.

REQUIREMENTS

- Check that the Ch. A trace is exactly in parallel with the horizontal graticule lines.
- If not correct this with the screwdriver control TRACE ROT.
- Shift the Ch. A trace upwards and downwards and check if the deviation from the straight line does not exceed 0,1 div measured outside the central 8x10 div.

MEASURING RESULTS .....

SETTINGS

- Press AUTO.
- Apply a 200 kHz/1,6 V (pp) sine wave voltage to the Ch. A input socket.
- Adjust the generator´s output voltage to 8 div vertical deflection.
- Select vertical display of Ch. A and B
- Shift the Ch. A and Ch. B display in the vertical mid of the screen.
- Select in the DISPLAY section A versus B display and switch register Ø on.

REQUIREMENTS

- Check that a vertical line of 8 div is displayed.
- Shift this line to the left and the right by means of X-POSITION and check if the deviation from the straight line does not exceed 0,1 div outside the central 8x10 div.

MEASURING RESULTS .....

	SETTINGS	- Shift the vertical line in the horizontal mid of the screen.
	REQUIREMENTS	- Check that the angle between the vertical graticule lines and the displayed line does not exceed 0,5 degree. This equals a horizontal deviation of 0,1 div max between top and bottom of the line.
	MEASURING RESULTS	.....

C. VERTICAL DEFLECTION

C.1	SUBJECT	Vertical deflection coefficients Ch. A (B).
	TEST EQUIPMENT	Calibrated sq. wave generator adjusted via internal switch (behind left-hand side panel) to deliver a calibrated d.c. voltage.
	SETTINGS	- Press AUTO. - Select channel A (B) for vertical display. - Position the time base line on one of the lower graticule lines. - Apply a 2V calibrated d.c. voltage (into 1 M.ohm) to input A (B). Halves into 50 ohm. - Check for a vertical displacement of the time base line of 5 div + or - 1,5% (+ or - 10% in EYE PAT mode) if the input signal is applied.
	MEASURING RESULTS	.....
	SETTINGS AND REQUIREMENTS	- Change the channel A (B) AMPL/DIV setting into respectively 100 mV, 50 mV and so on according to the table below. - Position the time base line without input signal on one of the lower graticule lines. - Apply a calibrated d.c. voltage of respectively 1 V, 0,5 V and so on according to the table below. - Check for a vertical displacement of 5 div + or - 1,5 % (+ or - 10% in EYE PAT mode) if the input signal is applied. Note: the above measuring method is chosen because the instrument can not trigger on the 1 kHz calibrated sq.wave signal. The vertical channels however are d.c. coupled.

Generator voltage	AMPL/DIV setting	Requirement Displacement	Accuracy Normal	Accuracy EYE PAT	Measuring results
1 V	100 mV	5 div.	+/-1,5%	+/-10%	
.5 V	50 mV	5 div.	+/-1,5%	+/-	
.2 V	20 mV	5 div.	+/-1,5%	+/-	
.1 V	10 mV	5 div.	+/-1,5%	+/-	
50 mV	5 mV	5 div.	+/-1,5%	+/-	
20 mV	2 mV	5 div.	+/-1,5%	-	
10 mV	1 mV	5 div.	+/-1,5%	-	

- Disconnect the input signal.

C.2 SUBJECT — Variable gain control.

TEST EQUIPMENT — Calibrated sq.wave generator in d.c. range.

SETTINGS
- Press AUTO.
- Select channel A (B) for vertical display.
- Turn the VARIABLE control out of the CAL position to 100 mV/div.
- Position the time base line on one of the lower graticule lines.
- Apply a calibrated d.c. voltage of 1V (into 1 M.ohm) to input A (B). This voltage halves into 50 ohm.

REQUIREMENT
- Check for a vertical displacement of the time base line of 5 div (+ or - 3%) if the input signal is applied.

MEASURING RESULT .....

SETTINGS AND REQUIREMENTS
- Turn the VARIABLE control maximally out of the CAL position.
- Disconnect the input signal.
- Position the time base line on the bottom graticule line.
- Apply the signal again and check for a vertical deflection of 7,5 div minimal.

MEASURING RESULT .....

IMPORTANT — Switch the calibrated sq. wave generator back from d.c. to 1kHz with the internal switch. This is not necessary if another PM3340 oscilloscope needs to be checked.

C.3

SUBJECT	DC-offset range.
TEST EQUIPMENT	L.f. sine-wave generator.
SETTINGS	- Press AUTO. - Select channel A (B) for vertical display. - Apply a sine wave signal of 1,6 V/200 kHz to the channel A (B) input. - Adjust the generator to an amplitude of 8 div.
REQUIREMENT	- Check that it is possible to adjust the OFFSET control so that the sine-wave can be shifted outside the graticule.
MEASURING RESULT	.....

C.4

SUBJECT	Vertical dynamic range Ch. A (B)
TEST EQUIPMENT	Constant amplitude sine-wave generator.
SETTINGS	- Apply a sine-wave of 200 MHz/800 mV (pp) to the Ch. A (B) input. - Press AUTO. - Readjust the output signal of the generator so that 4 div are displayed. - Select 100 mV/div with the Ch. A (B) AMPL/ DIV control so that 8 div signal are displayed on the screen.
REQUIREMENTS	- Check that the displayed sine-wave is free from distortion.
MEASURING RESULTS	.....

C.5 SUBJECT — Common mode rejection ratio (CMRR).

TEST EQUIPMENT — Constant amplitude sine-wave generators SG503, SG504 and a power splitter with 2 exactly identical output cables. SG503 is used to measure CMRR at 100 MHz; SG504 is used to measure at 500 MHz.

SETTINGS
- Connect the SG503 (SG504) generator to the power splitter.
- Connect the outputs of the power splitter via exactly identical coax cables with the channel A and B input sockets.
- Adjust the SG503 (SG504) generator frequency to 100 MHz (500 MHz) and its output voltage to approximately 1V.
- Press AUTO.
- Adjust the generator's output voltage to a deflection of 8 div via ch. A and B.
- Select ch. A INVERT and ADD mode.
- Adjust the VARIABLE control of ch. A or B to minimal signal amplitude on the screen.

REQUIREMENT
- Signal amplitude displayed on screen must be equal or smaller than 0,2 div (0,8 div).

MEASURING RESULTS .....

C.6 SUBJECT — Pulse response.

TEST EQUIPMENT — Pulse generator with rise-time $\leq$70 ps.

SETTINGS
- Apply the fast-rising pulse to the channel A (B) input.
- Press AUTO.
- Adjust the AMPL/DIV control so that the pulse amplitude is as high as possible within the graticule.
- Adjust the TIME/DIV control to 1 us.
- Adjust LEVEL so that display starts at leading edge of pulse.
- Select TIME/DIV: 1 ns.
- EXPAND the time base settings via the MAGN/DELAY menu and keep the leading edge of the pulse within the graticule by adjustment of the DELAY value.
- Press LOCK.

- Measure the rise time with the CURSOR/ANALYSE menu via the selections MEASURE, TIME and RISE. The cursors must be positioned at beginning and end of the rising slope. For the RISE LIMIT 10%/90% must be selected.
- Press WRITE.

REQUIREMENT

The rise-time measured on the screen must be 189 ps or less. This value takes into account the rise-times of generator and oscilloscope.

MEASURING RESULT .....

C.7 SUBJECT

Base line instability.

TEST EQUIPMENT

--

SETTINGS

- Press AUTO without input signals.
- Select Ch. A and B for vertical display.
- Position the A and B lines in the vertical mid of the screen with OFFSET A and B.
- Select function ADD.

REQUIREMENTS

- Check that the line that should be in the vertical mid of the screen does not have a displacement of more that 0,3 div. from the vertical mid of the graticule.

MEASURING RESULTS .....

SETTINGS

- Switch channel A and B on.
- Switch up and down through the range 5 ... 200mV of the Ch. A and B AMPL/DIV control. This happens if you keep the knob fixed in one of its two switching positions.

REQUIREMENTS

- Check that the Ch. A and B lines do not jump more than 0,4 div.

MEASURING RESULTS .....

SETTINGS	- Switch channel A and B on. - Switch the softkey functions "A-INVERT" and "B-INVERT" repeatedly on and off.
REQUIREMENTS	- Check that the Ch. A and B lines do not jump more than 0,5 div.
MEASURING RESULTS	.....

SETTINGS	- Switch channel A and B on - Turn the controls VARIABLE gain Ch. A and B repeatedly between their extreme positions.
REQUIREMENTS	- Check that the Ch. A and B line do not move more than 0,25 div.
MEASURING RESULTS	.....

C.8

SUBJECT	Average function.
TEST EQUIPMENT	Constant amplitude sine-wave generator SG503 and l.f. sine-wave generator.
SETTINGS	- Press AUTO. - Apply a l.f. sine-wave of 100 kHz/1,2 V (pp) to the Ch. A input. - Adjust generator amplitude to 6 div. - Apply a h.f. sine-wave of 250 MHz/0,2 V (pp) from the constant amplitude generator to the Ch. B input socket. This is the artificial noise signal. - Ch. B input sensitivity must be 200 mV/div - Select ADD mode for vertical display. The display now shows the 100 kHz/6 div sinewave with much 245 MHz "noise" superimposed.

REQUIREMENTS - Select via vertical MODE and PROCESSING the AVERAGE mode. Now you can select the value "C" between 2...64. The higher C is choosen, the cleaner the display becomes: the noise is eliminated. A high C value has the disadvantage that the correction action lasts longer

MEASURING RESULTS .....

D. HORIZONTAL DEFLECTION

D.1 SUBJECT Deflection coefficients time base.

TEST EQUIPMENT Time marker generator.

SETTINGS
- Press AUTO.
- Apply the output signal of the time marker generator to input Ch. A.

REQUIREMENTS
- Check the TIME/DIV coefficient errors according to the table below. This must be measured across the central 8 horizontal divisions.

Time markers(pp) pulse frequency	time base setting .../div	Max. coefficient error	Measuring results
20 us	20 us	+or- 3%	.....
10 us	10 us	+or- 3%	.....
5 us	5 us	+or- 3%	.....
2 us	2 us	+or- 3%	.....
1 us	1 us	+or- 3%	.....
500 ns	0,5 us	+or- 3%	.....
200 ns	0,2 us	+or- 3%	.....
100 ns	0,1 us	+or- 3%	.....
50 ns	50 ns	+or- 3%	.....
20 ns	20 ns	+or- 3%	.....
10 ns	10 ns	+or- 3%	.....
5 ns	5 ns	+or- 3%	.....
2 ns	2 ns	+or- 3%	.....
1 ns	1 ns	+or- 3%	.....

- Remove the input signal.

D.2 SUBJECT — Trigger sensitivities.

TEST EQUIPMENT — Constant sine-wave generator SG503.

SETTINGS

- Apply the output voltage of the generator to input A of the oscilloscope.
- Adjust the output voltage to 250 kHz/10 mV.
- Press AUTO.
- Select TRIGGER MODE TRIGG´ED and HIGH SENS.
- The trigger sensitivities can be checked according to the table below. The trigger source is identical to the input to which the generator is applied.
  The trigger sensitivity is sufficient if the signal on the screen is refreshed constantly (compare the memory mode LOCK where this is not done). During the now following test steps adjustment of TIME/DIV may be necessary. Also small LEVEL adjustments may be necessary to obtain a triggered signal.

SETTINGS, REQUIREMENTS AND RESULTS

generator output	scope input, sensitivity, mode	requirement, result
250 kHz/10 mV	A, HIGH, TRIGG´ED	triggered signal: .....
250 kHz/10 mV	B, HIGH, TRIGG´ED	triggered signal: .....
250 kHz/10 mV	EXT, HIGH, TRIGG´ED	triggered "line": .....
250 kHz/100 mV	A, LOW, TRIGG´ED	triggered signal: .....
250 kHz/100 mV	B, LOW, TRIGG´ED	triggered signal: .....
250 kHz/100 mV	EXT, LOW, TRIGG´ED	triggered "line": .....
200 MHz/20 mV	A, HIGH, COUNTDOWN	triggered signal: .....

TEST EQUIPMENT — Constant sine-wave generator SG504 and frequency doubler HP11721A.

SETTINGS

- Connect the generator´s output head to the input of the frequency-doubler. For a good functioning of the frequency doubler it is necessary to drive it with a generator voltage higher then 2 V. The correct input voltages for the oscilloscope can be made with attenuator pieces of good quality between frequency-doubler output and scope input and by varying the generator voltage between 2 and 5,5 Volt. Combinations of 2 attenuators are possible.
- The trigger mode must be COUNTDOWN because the sensitivity checks are in the range 0,5...2 GHz.
- Check the trigger sensitivities according to the table below (readjust TIME/DIV if necessary for a good display):

SETTINGS, REQUIREMENTS
AND RESULTS

Generator output	Doubler output	scope input sensitivity	requirement, results
245 MHz	20 mV	A, HIGH	triggered signal, ...
0.9 GHz *	25 mV *	A, HIGH	triggered signal, ...
0,9 GHz *	25 mV *	B, HIGH	triggered signal, ...
1 GHz *	50 mV *	A, LOW	triggered signal, ...
1 GHz *	50 mV *	B, LOW	triggered signal, ...

*) Adjust the output voltage at 245 MHz to respectively 20, 25 or 50 mV. Then turn the frequency up to 1 GHz.

SETTINGS

- Apply the output signal of frequency doubler via the necessary attenuators to a power splitter. The splitter´s output signals are applied to respectively input input A and input EXT.
- Select channel A for vertical display.
- Select EXT as trigger source.
- Select trigger modes COUNTDOWN and SENS HIGH (SENS LOW).
- Adjust the generator signal via the channel A display to an amplitude of 25 mV (50 mV) at a generator frequency of 245 MHz. Increase the generator frequency then to 900 MHz (1000 MHz).

REQUIREMENT

- Check for a stable triggered display via channel A.

MEASURING RESULT .....

d.3 SUBJECT Trigger mode switching.

TEST EQUIPMENT Constant sine-wave generator SG 503.

SETTINGS

- Apply a 140MHz sine-wave of 1V to ch. A.
- Press AUTO SET.
- Vary the generator frequency in the range 140 ... 170 ... 140 MHz.

REQUIREMENT

- Check via the front panel LED´s that the trigger mode changes from TRIGGER to COUNT DOWN at 160MHz (typical value).
- Check that the trigger mode changes from COUNTDOWN to TRIGGER at 150 MHz (typical).

MEASURING RESULT .....

E.	CURSORS	
	SUBJECT	Time cursor accuracy.
	TEST EQUIPMENT	Time marker generator.
	SETTINGS	- Apply 20 us time marker signal to the Ch. A input. - Press AUTO. - Select a suitable AMPL/DIV position for Ch. A. - Select 20 us/div for the time base. - Press LOCK. - Press CURSOR/ANALYZE and softkey ON. - Select REG Ø/ch. A for 1st and 2nd cursor - Position the 1st CURSOR and the 2nd CURSOR so that they cover a distance of 8 time marker intervals.
	REQUIREMENTS	Check for a time cursor read-out of 160 us + or - 0,5 us.
	MEASURING RESULTS	.....
	SETTINGS	- Select WRITE again.

F.	CALIBRATION VOLTAGE	
	SUBJECT	Calibration voltage accuracy.
	TEST EQUIPMENT	Digital multimeter adjusted to the d.c. voltage range
	SETTINGS	Connect the digital multimeter to the CALibration output socket.
	REQUIREMENTS	Check for a voltage read out of 1000 mV (+or- 10 mV).
	MEASURING RESULTS	.....

4

G.	PLOT OUTPUT	
	SUBJECT	Accuracy of vertical and horizontal plot output voltages.
	TEST EQUIPMENT	Digital multimeter and 1.f. sq.wave generator.
	SETTINGS	- Plug the plot cable into the DIN plot output socket at the rear of the instrument. - Apply a sq.wave signal of 10 kHz/1,2 V (pp) to input A and B. - Press AUTO. - Select 200 mV/div for Ch. A and B. - Position the two sq.wave signals in the vertical mid of the screen with OFFSET A and B. - Increase the generator´s output voltage so that the displayed signal is 6 divisions. - Select TIME/DIV: 10us. - Select 100 mV/div for Ch. A and B. - Select A versus B via the DISPLAY mode and switch register RØ on. - Select 20 ms/DT via the menus SAVE/PLOT, SELECT and ANALOG. - Press softkey RETURN two times and then ANALOG so that the oscilloscope starts the plot action. This can be seen because the dot moves from left to right in the bottom of the screen.
	REQUIREMENTS	- Measure with the digital multimeter (d.c. voltage range) the maximum voltage at the vertical plot output (red banana plug, black is mass). This voltage must be 1000 mV + or - 30 mV. - Measure with the digital multimeter (d.c. voltage range) the maximum voltage at the horizontal plot output (blue banana plug, black is mass). This voltage must be 1000 mV + or - 30 mV.
	MEASURING RESULTS	.....

DISMANTLING THE INSTRUMENT 5

DISMANTLING THE INSTRUMENT

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5.3 Access to parts for the adjusting procedure..... 5-2

5.0 DISMANTLING THE INSTRUMENT

5.1 GENERAL INFORMATION

This section provides the dismantling procedures required for the removal of components during repair operations.
All circuit boards removed from the instrument must be adequately protected against damage, and all normal precautions regarding the use of tools must be observed.
During dismantling a careful note must be made of all disconnected leads so that they can be reconnected to their correct terminals during assembly.

CAUTION: Damage may result if:

- the instrument is switched on when a circuit board has been removed.
- a circuit board is removed within one minute after switching-off the instrument.

5.2 REMOVING THE COVERS

The instrument is protected by three covers: a front protection cover, a top cover and a bottom cover. To facilitate the removal of the instrument's covers, first put the front protection cover in position.

Then proceed as follows:

- Hinge the carrying handle clear of the front protection cover.
- Stand the instrument on its protective front cover on a flat surface.
- Unscrew the two screws A and B present in the left foot and the two screws C and D present in the right foot at the rear panel and remove these feet (see figure 5.1).
- The top cover and the bottom cover (without carrying handle) can be removed by shifting them backwards and lifting them of the instrument.

NOTE: When reinstalling the top and bottom covers again, take care that the wiring (coaxial cables and flat cables) is not damaged.
Reinstalling the top and bottom covers has to be done in the reversed order as described above.

5.3 ACCESS TO PARTS FOR THE ADJUSTING PROCEDURE

After performing the actions which are described in section 5.2, all adjustment points are easily accessible.

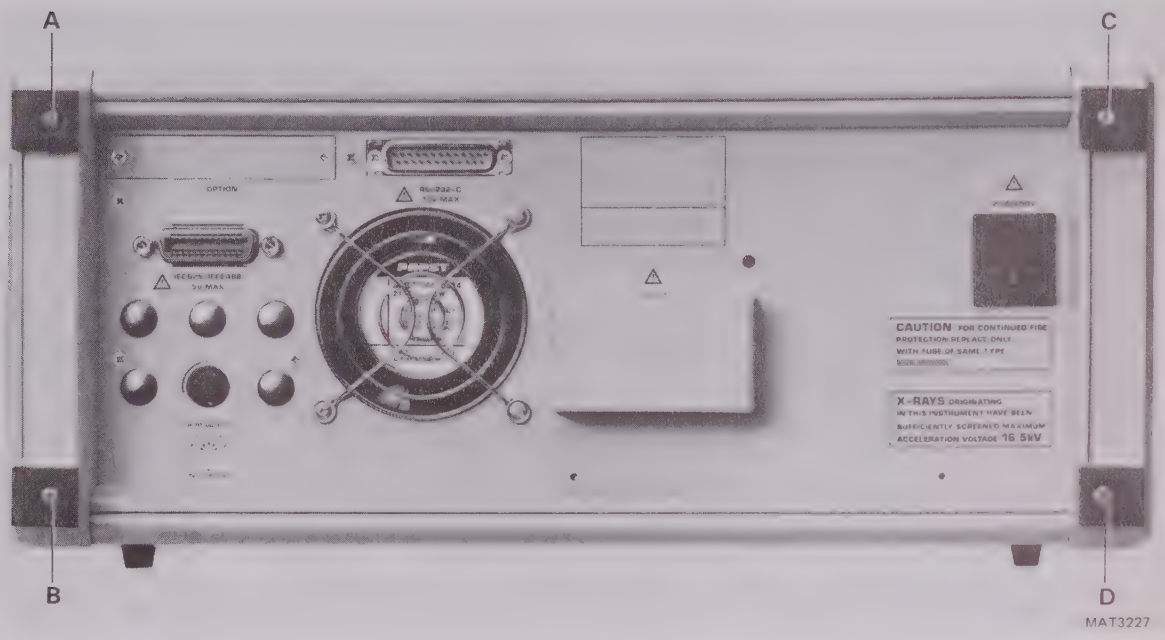

Figure 5.1 Removing the rear feet.

BLOCKDIAGRAM AND DESCRIPTION 6

BLOCK DIAGRAM AND DESCRIPTION

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6.0 BLOCKDIAGRAM AND DESCRIPTION

This chapter serves to explain the main functions of the oscilloscope. The system can be divided into a number of sections:

- Acquisition section
- Calculation section
- Display and plot section
- Front section
- Control section
- Power supply section

6.1 ACQUISITION SECTION

By means of the acquisition section the analog signals are sampled and converted into digital codes.
Before conversion the analog input signals must be adapted so that an Analog to Digital Converter (ADC) is able to convert them.

6.1.1. The vertical channels (units A54...A57, A69).

The vertical section consists of two identical channels A and B with a sensitivity range of 1 mV/div...200 mV/div in a 1-2-5 sequence.
Each channel includes a probe indication.
Since both channels are identical, only channel A is described.

The input signal is applied to the SAMPLING GATE via a TRIGGER PICK-OFF and a 30 nsec DELAY LINE.
The TRIGGER PICK-OFF supplies a trigger signal with an amplitude of about one tenth of the input signal to the TRIGGER INPUT unit.
The DELAY LINE compensates the time delay in the trigger circuits, which enables the trigger point to be displayed on the screen.
The SAMPLING GATE takes samples of the input signal on receipt of a sampling pulse from the SAMPLING DRIVER, which gets the sampling pulses on its turn from the FAST RAMP unit.
The SAMPLING GATE is supplied by the AVALANCHE VOLTAGE circuit and the SNAPP OFF CURRENT circuit.The samples are first amplified by the PRE-AMPLIFIER and the AMPLIFIER of which the amplification factor is depending on the selected vertical sensitivity of the instrument.
The TRACK & HOLD circuit, which is controlled by the TRACK & HOLD CONTROL holds the samples for a while.

Next the samples go via the VARIABLE circuit to the CHANNEL SWITCH. This switch selects channel A or channel B or switches between them if both channels are selected.

Via the BRIDGE, the selected OFFSET and the feedback signal from the FEEDBACK ATTENUATOR are added to the input signal.
The feedback attenuation factors and the amplification factors are set by the microprocessor via the VERTICAL LATCH.

6.1.2 The management circuit (unit A25).

The feedback codes from the DPU are converted from 2's complement code to straight binary code by CODE CONVERT and applied to FEEDBACK LATCH A and FEEDBACK LATCH B.
Via the FEEDBACK DAC, which converts to an analog signal and a multiplier VARIABLE, the feedback signal is applied to the VERTICAL SIGNAL unit.
The CHANNEL SWITCH DRIVER buffers the channel switch control signal.

Data from and to the microprocessor are buffered by the BIDIRECTIONAL DATA BUFFER.
The address bus is buffered by the ADDRESS BUFFER, which is controlled by the I/O SELECT DELAY. The ADDRESS DECODER selects one of the STATUS FLIPFLOPS and the INPUT PORT. Via the STATUS FLIPFLOPS, the microprocessor sets the hardware corresponding to the settings made on the front panel.

Via the INPUT PORT the probe type information is read from the PROBE DETECTION circuit on the DISTRIBUTION unit. Also a number of trigger status signals are read via this port.

Four DACs supply the offset signals to the VERTICAL SIGNAL unit. These DACs are: OFFSET DAC FINE A, OFFSET DAC COARSE A, OFFSET DAC FINE B and OFFSET DAC COARSE B.

6.1.3 The ADC circuit (unit A11)

Signal levels from the CHANNEL SWITCH are applied via a CORRECTION CIRCUIT to a TRACK AND HOLD circuit which is able to hold the levels for a time long enough for the ADC circuit behind it to do the conversion to a 12-bit digital word. The ADC is able to perform conversion in 2.5 us and is controlled by the ADC LOGIC. The 12-bit digital code is converted from straight binary into two's complement by the CODE CONVERT circuit and then latched in the SAMPLE DATA LATCH for further data handling by the Digital Processing Unit (DPU).
The ADC output is also connected to an OVERFLOW DETECTION circuit, which on its turn is connected with the DPU.

6.1.4 The trigger circuits (units A31, A32 and A34)

The signals from the TRIGGER PICK-OFFS and an EXTernal trigger signal are applied to the TRIGGER SELECTOR on the TRIGGER INPUT unit. The selected trigger signal is led via the X1/X10 AMPLIFIER to the PRESCALER, which is used for the count down mode.
The TRIGGER AMPLITUDE DETECTOR detects if the amplitude of the trigger signal is sufficient for triggered mode or count down mode.
The trigger signal from the PRESCALER is applied to the BUFFER on the THREE STAGE TRIGGER unit.
Via the SLOPE CONTROL, the trigger signal is led to the three stages STAGE 1, STAGE 2 and STAGE 3. Via LEVEL CONTROL these stages receive a trigger level signal.
After the HOLD OFF time being elapsed, which is marked by a signal from the SYNC SWITCH on the FAST RAMP unit, the three stages change over in sequence on receipt of a trigger signal, resulting in a signal from STAGE 3, which starts the FAST RAMP GENERATOR on the FAST RAMP unit.

In synchronized mode, the stages are released continuously via the SYNC CONTROL, which results in a signal to the FAST RAMP GENERATOR, directly after the hold off time.

The trigger signal from the TRIGGER INPUT unit is applied via a FILTER/AMPLIFIER, to the DIVIDER HIGH AMPLITUDE and the DIVIDER LOW AMPLITUDE. Their output signals are used for the trigger mode control by the UPPER FREQUENCY DETECTOR, the LOWER FREQUENCY DETECTOR, the COUNT DOWN CONTROL and the TRIGGER MODE CONTROL.
The microprocessor determines the triggermode via the TRIGGER LATCH.
The TRIGGER LEVEL ADAPTION adapts the signal from the TRIGGER LEVEL DAC on the Management unit for the Three Stage Trigger unit.

6.1.5 The time-base circuits (units A51 and A52)

When a trigger occurs, a signal from STAGE 3 on the Three Stage Trigger unit starts the FAST RAMP GENERATOR. When the signal crosses the level of the stair signal from ADD INVERT, the FAST RAMP/STAIR COMPARATOR generates a sampling pulse, which is applied to the SAMPLING DRIVER.
This causes a sample of the input signal to be taken. There is also a sampling signal applied to the Acquisition Control Logic on the GRAM unit.
When the fast ramp reached its end level, the END OF FAST RAMP COMPARATOR sets the HOLD OFF FLIPFLOP, which on its turn blocks further trigger pulses from the Three Stage Trigger unit via the SYNC SWITCH. The Three Stage Trigger unit also resets the FAST RAMP GENERATOR.
When the HOLD OFF FLIPFLOP is set, the HOLD OFF INTEGRATOR is started. The slope of the output signal is determined by the microprocessor, via the HOLD OFF DAC. The end level of this signal is determined by the END OF HOLD OFF COMPARATOR, which resets the HOLD OFF DAC.
The stair signal, which is used for the sequential sampling system, is generated by the STAIR COUNTER and the STAIR DAC. After every sample, the Acquisition Control Logic on the GRAM generates a count pulse to the STAIR COUNTER. The binary value of the output signal is incremented, which result in an increase of the output signal of the STAIR DAC.
To obtain a trigger delay this signal can be attenuated by the STAIR ATTENUATOR and a d.c. signal from the TRIGGER DELAY DAC can be added to it, before it is inverted in the ADD INVERT circuit.
Via the TIME-BASE LATCH, the Microprocessor controls various settings on these units, depending on the selected front panel settings. It also controls the slope of the fast ramp via the FAST RAMP DAC.

6.1.6 The acquisition control logic (unit A5)

The ACQUISITION CONTROL LOGIC (ACL) controls the timing of the acquisition system.
Via the ACL LATCH it is informed by the microprocessor about the selected front panel settings. The ACL RESET LOGIC resets the ACL under control of the ILØ1--LT signal from the microprocessor or TRRY from the DPU Control.

6.2 THE CALCULATION SECTION (units A8 and A9)

The calculation section consists of a Data Processing Unit (DPU unit A9) which is a very fast microcomputer system with a cycle time of 125 nsec.
It takes data from the ADC, performs calculations on it and sends the data to the TRACE DATA LATCH and to the FEEDBACK LATCHES. All data are transported via the BUFFER.

The possible calculations are:

- adding of both channels in ADD mode
- inverting of one or both channels
- averaging
- linear interpolation
- overflow detection

To perform the calculations the DPU has a number of calculation registers and function blocks:

- REGISTER I, II and III
- SHIFT REGISTER
- +/- (complement function)
- ADDER
- LIMIT DETECTION

An overflow at the ADC is detected by the OVERFLOW DETECTION circuit, which enables the REFLECTION SUPPRESSION.

The DPU has registers in which data are stored. These are:

- PRE-TRIGGER RAM.
  This is used as general workspace, e.g. for interpolation calculations.
- AVERAGE RAM.
  Used for average calculations.
- FLAG RAM.
  In this ram is stored wether samples are real samples or samples obtained by interpolation. If an overflow occurs, this is also stored by means of a flag. Flags are stored by means of the FLAG HANDLER.

The DPU is controlled by the DPU control (unit A8). The heart of the DPU control is the CONTROL MEMORY. This serves as a program memory for the DPU.
This memory is loaded for the various functions by the microprocessor system via the ADDRESS MULTIPLEXER and the BUFFER.
The DPU control has a PIPELINE REGISTER, which holds the current instruction, while the next instruction is fetched from the CONTROL MEMORY.
The instruction which is fetched depends on the address given by the ADDRESS MULTIPLEXER.
This address depends on data given by the STATUS MULTIPLEXER, which on its turn gets status signals from various function blocks.
The PIPELINE REGISTER is controlled by the START/STOP logic and the CONTROL LATCH.
When a DPU program is finished, the START/STOP LOGIC informs the microprocessor system about this via interrupt line ILØ2--LT.
The INSTRUCTION REGISTER and the CONTROL REGISTER, control the operation of the DPU control.

The ADDRESS GENERATOR generates addresses for the PRE TRIGGER RAM, the AVERAGE RAM and the FLAG RAM.
The ADDRESS GENERATOR consists of an ADDRESS REGISTER and a PRETRIGGER COUNTER, which can be loaded via a buffer. The MULTIPLEXER selects the ADDRESS from the PRETRIGGER COUNTER or from the ADDER. The ADDER adds the addresses from the ADDRESS REGISTER and the OFFSET JUMP REGISTER. The latter enables the DPU to make jumps in program execution.
The TRIGGER ADDRESS COMPARATOR has no function in this instrument.
The ADDRESS DECODER enables the microprocessor system to have control over the calculation section.

6.3 DISPLAY AND PLOT SECTION (units A1, A2, A3 and A4)

The display section consists of hardware to display trace data as well as text data on the C.R.T display.
A complete display cycle for all traces and all texts to be displayed, is realized in less than 20 ms. This results in a stable and flicker-free display.

Trace data words from the DPU system which have to be copied to the TRACE MEMORY in the display section are latched in the TRACE DATA LATCH in the rhythm of the DPU clock and the display section is for each new trace data word informed via the HANDSHAKE LOGIC (signal sample ready) that it is available for storage in REGISTER RØ of the TRACE MEMORY.
Addresses for the TRACE MEMORY are then generated by the COPY ADDRESS COUNTER. This counter which is corrected to the TRACE MEMORY via ADDRESS MULTIPLEXER II starts each new copy cycle for a complete new trace with the generation of address zero. It counts then by the same rhythm as the DPU. After the storage of each trace data word in the TRACE MEMORY, a sample ready acknowledge signal is given to the DPU via the HANDSHAKE LOGIC.

6.3.1 The SAVE function

When a SAVE function is selected, the contents of REGISTER RØ is copied in one or more of the REGISTERS R1, R2 or R3.
The trace data words are then first saved in the SAVE LATCH before they are saved in the selected REGISTER.
The REGISTER can be addressed then by the DISPLAY ADDRESS COUNTER via ADDRESS MULTIPLEXERS I AND II.

6.3.2 Trace display

X=t display mode

The trace data words to be displayed are transferred from the TRACE MEMORY via the DISPLAY CONTROL LATCH to an INVERT stage which offers the facility to invert the stored data before display. This facility can be softkey selected per register.
Data passes then a VERTICAL EXPAND stage of which the expand factor is set in combination with the gain factor of the Y AMPLIFIER later in the signal path. In this way, the Y/5, Y*1 and Y*5 vertical expand modes are realized.
The resulting data are latched in a LATCH and vertical position information, which is calculated by the microprocessor and applied via a VERTICAL POSITION LATCH, can be added by a VERTICAL POSITION ADDER stage. It is then converted from 2's complement into straight binary by the CODE CONVERT circuit and latched in a YDAC LATCH before the

conversion by the digital to analog converter YDAC. The converter output signal can then be deglitched by a SAMPLE AND HOLD circuit and influenced by a DOT JOIN/SMOOTH circuit. It is then amplified by a Y AMPLIFIER by a factor which depends on the selected vertical expand factor. The signal is then applied to a Y FINAL AMPLIFIER which directly drives the vertical deflection plates of the C.R.T.

Horizontal deflection signals are derived from the addresses for the TRACE MEMORY, which are generated by the DISPLAY ADDRESS COUNTER. These addresses are applied via the DISPLAY ADDRESS DATA BUFFFER to the HORIZONTAL EXPAND I CIRCUIT.
Horizontal expand factors of *1, *2, *4 and *8 can be realized. After expansion, horizontal position information, which is calculated by the microprocessor system and applied via a HORIZONTAL POSITION LATCH, can be added by a HORIZONTAL POSITION ADDER stage.
An additional expand factor of *1 or *8 can be realized in the HORIZONTAL EXPAND II circuit before the conversion by the digital to analog converter XDAC.
The converter output signal can then be deglitched by a SAMPLE AND HOLD circuit and influenced by a DOT JOIN/SMOOTH circuit. It is then amplified by an X AMPLIFIER of which the gain factor depends on the setting of the continuous X-EXPAND control on the frontpanel. This information is applied via an X-EXPAND LATCH and an X-EXPAND DAC to the X-AMPLIFIER.
The signal is then applied to an X FINAL AMPLIFIER which directly drives the horizontal deflection plates of the C.R.T.

A versus B display mode

This display mode is only selectable in dual channel mode.
The channel B TRACE MEMORY contents is applied to the vertical deflection plates of the CRT in a way as described for the X=t display.

For horizontal deflection the channel A TRACE MEMORY contents is used instead of the addresses from the DISPLAY ADDRESS COUNTER. The channel A trace data is converted from 2's complement into straight binary via the CODE CONVERT circuit and then transferred via the AVSB DATA BUFFER to the horizontal signal path and the horizontal deflection plates as described before for the X=t display addresses.

6.3.3 Text display

The text which has to be displayed, is generated by the microprocessor system and stored in the TEXT MEMORY.
Data is transferred from the microprocessor data bus via the DATA/TEXT BIDIRECTIONAL LATCH to the TEXT MEMORY.
Addresses from the microprocessor address bus are applied to the TEXT MEMORY via ADDRESS MULTIPLEXER I.

Each dot to be displayed on the C.R.T screen is stored in the TEXT MEMORY by a word consisting of a vertical and a horizontal coordinate and an intensity flag.

There are a number of different text blocks like:

Top area text	(TAT)
Trace area text	(TRAT)
Bottom area text	(BAT)
Softkey text	(SKT)
Miscellaneous text	(MSC)

The vertical coordinates are applied to the vertical deflection plates of the C.R.T. via a TEXT/TRACE BIDIRECTIONAL BUFFER and in a way as described for the X=t display.

The horizontal coordinates are applied via the LINE TEXT DATA BUFFER (for TAT, TRAT and BAT) or via the SOFTKEY TEXT DATA BUFFER (for SKT) or via the AVSB DATA BUFFER (for MSC) to the horizontal signal path and the horizontal deflection plates as described before for the X=t display addresses.

The intensity flag is used to inform the Z-stage about normal or intensified display.

6.3.4 Display control

Each display cycle, which consists of a fixed sequence of trace data blocks followed by a fixed sequence of text blocks, is controlled by the microprocessor system.
The microprocessor system places via a DATA BUFFER preset and control data into a number of OUTPUT PORTS, an Z + INTERRUPT TIMER and a PRESET REGISTER for the DISPLAY ADDRESS COUNTER, at the start of the display of each display data block.

At the same moment new position information is placed in the VERTICAL POSITION LATCH and in the HORIZONTAL POSITION LATCH.

At the end of each display block an interrupt signal IL$\emptyset$5--LT is generated which is applied to the microprocessor system to ask for the actual preset and control data for the next display block.

6.3.5 Z-control (unit A1 and A15)

The Z-AMPLIFIER is controlled by the following circuits:

- Reflection detection circuit
- Overscan detection circuit
- Z detection circuit

Reflection detection

Reflection is caused by adding a position information to a signal information in the vertical as well as in the horizontal signal path which causes an overflow in the highest (non-existing) bits. Such an overflow causes the top of the signal being displayed at the bottom of the display like it is a reflection. In a similar way an underflow causes a reflection in the top of the display. Both situations can also occur in horizontal direction. These reflection can be detected by the REFLECTION DETECTION circuit and via the Z-DETECTION circuit suppressed by the Z-AMPLIFIER.

Overscan detection

Signals have to be displayed within the trace area of 8x10 divisions of the C.R.T. screen. Overscan in one of the four screen area directions is detected by the OVERSCAN DETECTION circuit and suppressed by the Z-AMPLIFIER.

Z-detection

Via the Z-DETECTION which is controlled by the Z-TIMER circuit the trace will be blanked when no traces or texts have to be displayed. The text can also be intensified if required. The last, for example, for active functions.
The Z-DETECTION output signal is applied to the Z-AMPLIFIER where it is influenced by the INTENSITY controls for the trace as well as for the text. The resulting signal is applied via the final Z-AMPLIFIER to the Wehnelt Cylinder of the CRT thus controlling the intensity of the trace on the screen. The focussing of the trace is controlled via the FOCUS block, under the influence of a FOCUS control by a signal which is applied to the focus grid of the CRT.

The a.c. and d.c. components of the output blanking signal from the Z-AMPLIFIER are guided along different paths.
The a.c. path runs straight to the FINAL Z-AMPLIFIER via a high voltage capacitor.
The d.c. component is modulated with 200 kHz by a MODULATOR, guided via a high voltage capacitor to the high voltage part and demodulated again by a DEMODULATOR. The resulting components are added and applied to the FINAL Z-AMPLIFIER and from there to the Wehnelt cylinder of the C.R.T.

6.3.6 Plot-output (unit A1)

Once per cycle of 20 ms a value can be plotted via the ANALOG PLOT INTERFACE. The X and Y informations are derived from the FINAL AMPLIFIERS and the penlift control is realized via the Z-AMPLIFIER stage.

6.3.7 Option handling

For OPTION handling, e.g. like the Interface, the TRACE MEMORY as well as the TEXT MEMORY can be addressed via the microprocessor system address bus.

The data flows from the microprocessor system data bus to or from the TRACE MEMORY and the TEXT MEMORY is realized via the DATA/TEXT and TEXT/TRACE BIDIRECTIONAL latches.

6.3.8 Calibrator (unit A53)

A CALIBRATOR generator generates a 100 kHz 1 Vp-p into 50 ohm calibration signal for the user which can be used to check the calibration of the system.

6.4 FRONT SECTION (units A13 and A14)

The front section contains a number of softswitches (the softkeys beside the CRT inclusive) and rotary controls (optical switches) of which the settings are read by the microprocessor system.

The softswitches are placed in a FRONT SWITCH MATRIX which places a row of switch settings in the FRONT SWITCH BUFFER each time that the matrix is addressed by the microprocessor system. The complete matrix is scanned every 40 ms.

The optical switches generate interrupt signals ILØ3--LT for the microprocessor system when they are operated by the user and the microprocessor in turn addresses the circuit after which the information (from the ROTARY ENCODER) about the direction of rotation is placed on the data bus for interpretation by the microprocessor system.

The front section also contains a number of front panel leds which are controlled by the microprocessor system via LED DRIVERS.

The addresses which are generated by the microprocessor system, are decoded by a number of ADDRESS DECODERS.

6.5 CONTROL SECTION (units A5 and A6)

The control section consists mainly of a powerfull MICROPROCESSOR system configuration, with an 68000 uP, a RAM MEMORY for data and a ROM MEMORY containing the system software. The MICROPROCESSOR is running at a frequency of 8 MHz which is provided by a CLOCK GENERATOR which is driven by a 16 MHz OSCILLATOR.

An ADDRESS DECODER decodes a number of addresses resulting in a number of I/O SELECT signals for the various units and a number of MEMORY SELECT signals for the various memories via the I/O and MEMORY SELECT BUFFERS.

Interrupt signals from various units are applied to an INTERRUPT PRIORITY LEVEL DECODER. From here the interrupt with the highest priority is send to the MICROPROCESSOR.

A WATCHDOG circuit detects abnormal program sequences via an OUTPUT PORT and resets the MICROPROCESSOR via the RESET/HALT block in order to restart the program. This is done by a monostable flip flop.

A BUS ARBITER controls the system bus and can give the control over the bus to processors which are fitted on options, if they ask for bus control via their BUS REQUEST signals.

The battery voltage is compared with a reference voltage by a COMPARATOR. The battery status as well as the settings of the on board SERVICE switches are applied via an INPUT PORT to the microprocessor system.
A too low battery voltage results via a SUPPLY VOLTAGE SWITCH in the saving of the memory contents.

The following functions are performed by this control section:

- Front panel settings are read and processed.
- Front panel leds are controlled.
- Time base, trigger delay counter, events counter and acquisition control logic circuits are set in accordance to the user selected settings.
- Digital processing circuits are provided with a separate program which depends on on the selected functions.
- The display system for trace, text and analog plot out data is controlled.
- If an option is installed, the complete handling is controlled.

6.6 POWER SUPPLY SECTION (units A19 and A20)

The mains voltage is applied via a MAINS SWITCH + FUSE to a MAINS FILTER and to a full-wave RECTIFIER. The rectified voltage is doubled, by means of a VOLTAGE DOUBLER, if the mains voltage is below 140V. This voltage is applied to a TRANSFORMER via a FLYBACK CONVERTER. The secondary voltages are rectified by RECTIFIERS and smoothed to supply voltages for the various circuits in the instrument. These voltages are regulated by a feedback to the CONTROL + PROTECTION CIRCUIT. This circuit gives protection against over-temperature and against over- or under-voltage,
For the +5 V a separate +5 V STABILIZER is fitted.

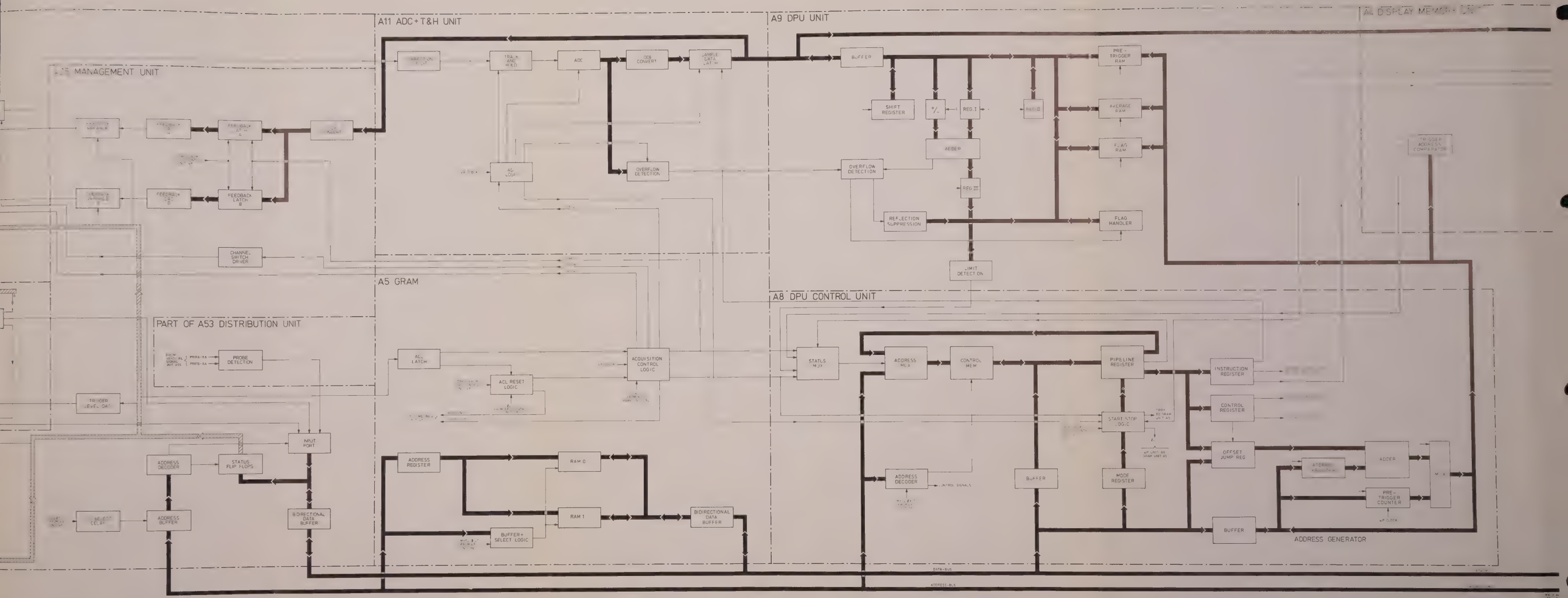
The voltages for the CRT filament and the CRT cathode are generated by an EHT converter. The cathode voltage is also multiplied in the EHT CONVERTER resulting in a high tension for the acceleration grid of the CRT.

The LINE TRIGGER CIRCUIT is not used in this instrument.

A REFERENCE VOLTAGE SOURCE circuit provides a reference voltage for internal use.

This section also contains a POWER DOWN/UP DETECTION circuit for the microprocessor. Via interrupt signal ILØ7--LT the microprocessor is informed about the status of the power supply.

The fan is controlled via the FAN CONTROL circuit, depending on the temperature of the oscilloscope.


A11 ADC+T&H UNIT
A9 DPU UNIT
A6 DISPLAY MEMORY UNIT
A5 MANAGEMENT UNIT
A5 GRAM
PART OF A53 DISTRIBUTION UNIT
A8 DPU CONTROL UNIT
ADC
BUFFER
SHIFT REGISTER
REG I
REG II
REG III
ADDER
OVERFLOW DETECTION
REFLECTION SUPPRESSION
LIMIT DETECTION
PRE-TRIGGER RAM
AVERAGE RAM
FLAG RAM
FLAG HANDLER
TRIGGER ADDRESS COMPARATOR
FEEDBACK LATCH B
CHANNEL SWITCH DRIVER
PROBE DETECTION
INPUT PORT
ADDRESS DECODER
STATUS FLIP FLOPS
ADDRESS BUFFER
BIDIRECTIONAL DATA BUFFER
ACQUISITION CONTROL LOGIC
ACL RESET LOGIC
ADDRESS REGISTER
RAM 0
RAM 1
BUFFER+ SELECT LOGIC
BIDIRECTIONAL DATA BUFFER
STATUS MUX
ADDRESS MUX
CONTROL MEM
PIPELINE REGISTER
START/STOP LOGIC
MODE REGISTER
INSTRUCTION REGISTER
CONTROL REGISTER
OFFSET JUMP REG
PRE-TRIGGER COUNTER
ADDER
BUFFER
ADDRESS GENERATOR
DATA BUS
ADDRESS BUS

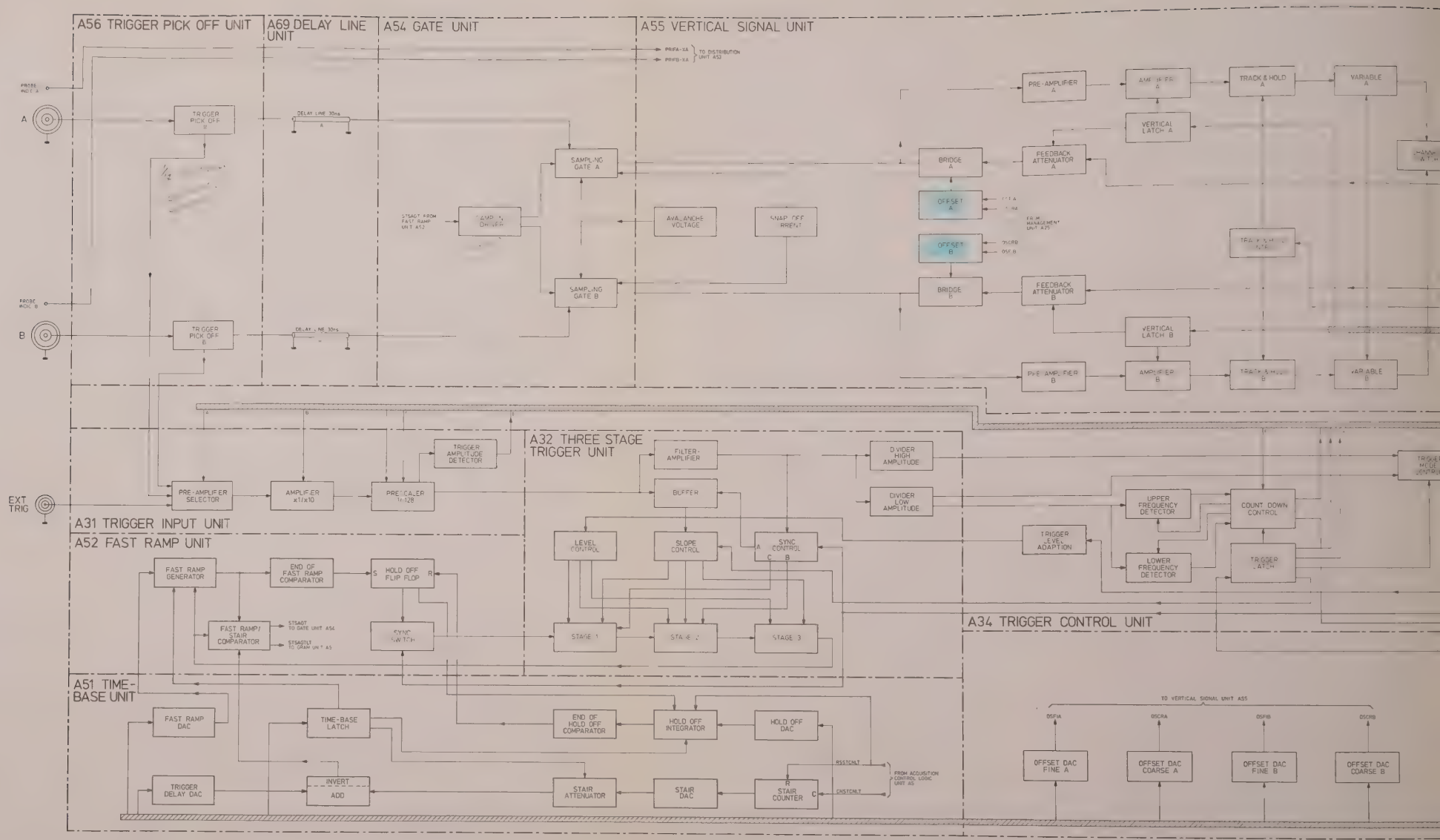
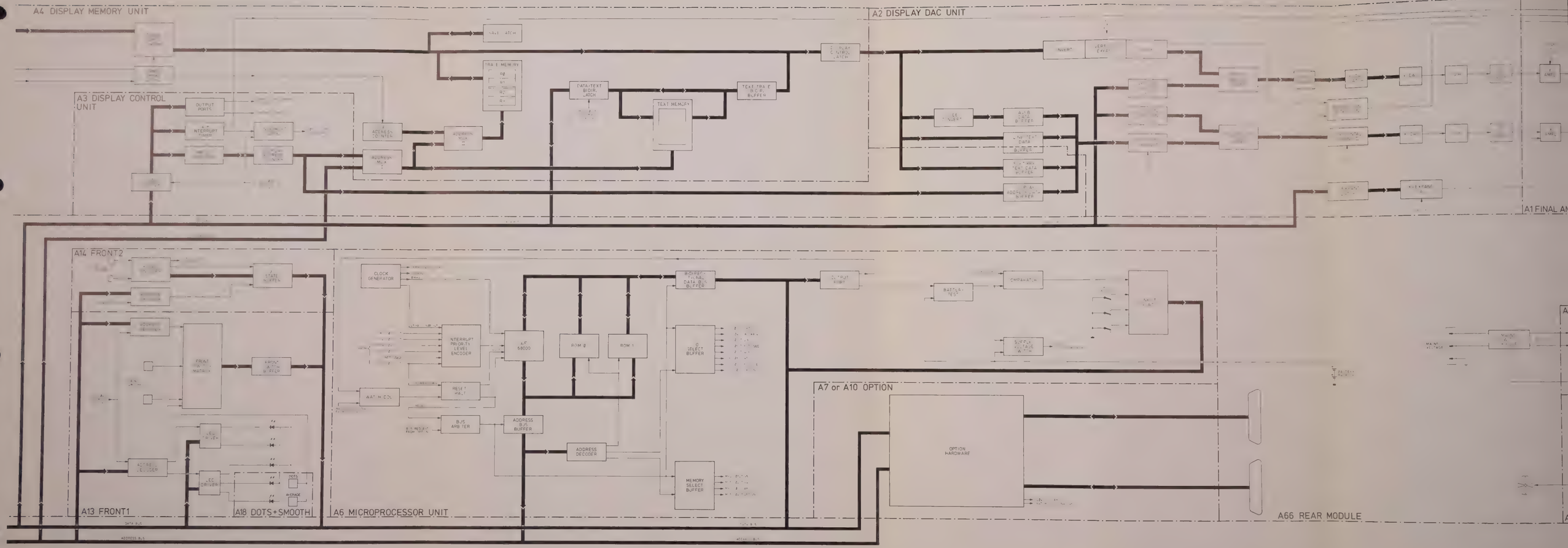


Figure 6.1 Detailed blockdiagram (part 1).


A4 DISPLAY MEMORY UNIT
A2 DISPLAY DAC UNIT
A3 DISPLAY CONTROL UNIT
OUTPUT PORTS
INTERRUPT TIMER
ADDRESS COUNTER
ADDRESS MUX
TRACE MEMORY
DATA/TEXT BIDIR. LATCH
TEXT MEMORY
TEXT/TRACE R.C.P. BUFFER
DISPLAY CONTROL LATCH
INVERT
VERT. EXPAND
A1 FINAL AM
A14 FRONT2
STATE BUFFER
FRONT PANEL BUFFER
LED DRIVER
KEY DRIVER
DOTS
AVERAGE
A13 FRONT1
A18 DOTS+SMOOTH
CLOCK GENERATOR
INTERRUPT PRIORITY LEVEL ENCODER
WAIT/HOLD
RESET HALT
BUS ARBITER
MC 68000
ROM 0
ROM 1
ADDRESS BUS BUFFER
ADDRESS DECODER
BIDIRECTIONAL DATA BUS BUFFER
I/O SELECT BUFFER
MEMORY SELECT BUFFER
A6 MICROPROCESSOR UNIT
BATTERY TEST
COMPARATOR
SUPPLY VOLTAGE WATCH
A7 or A10 OPTION
OPTION HARDWARE
A66 REAR MODULE

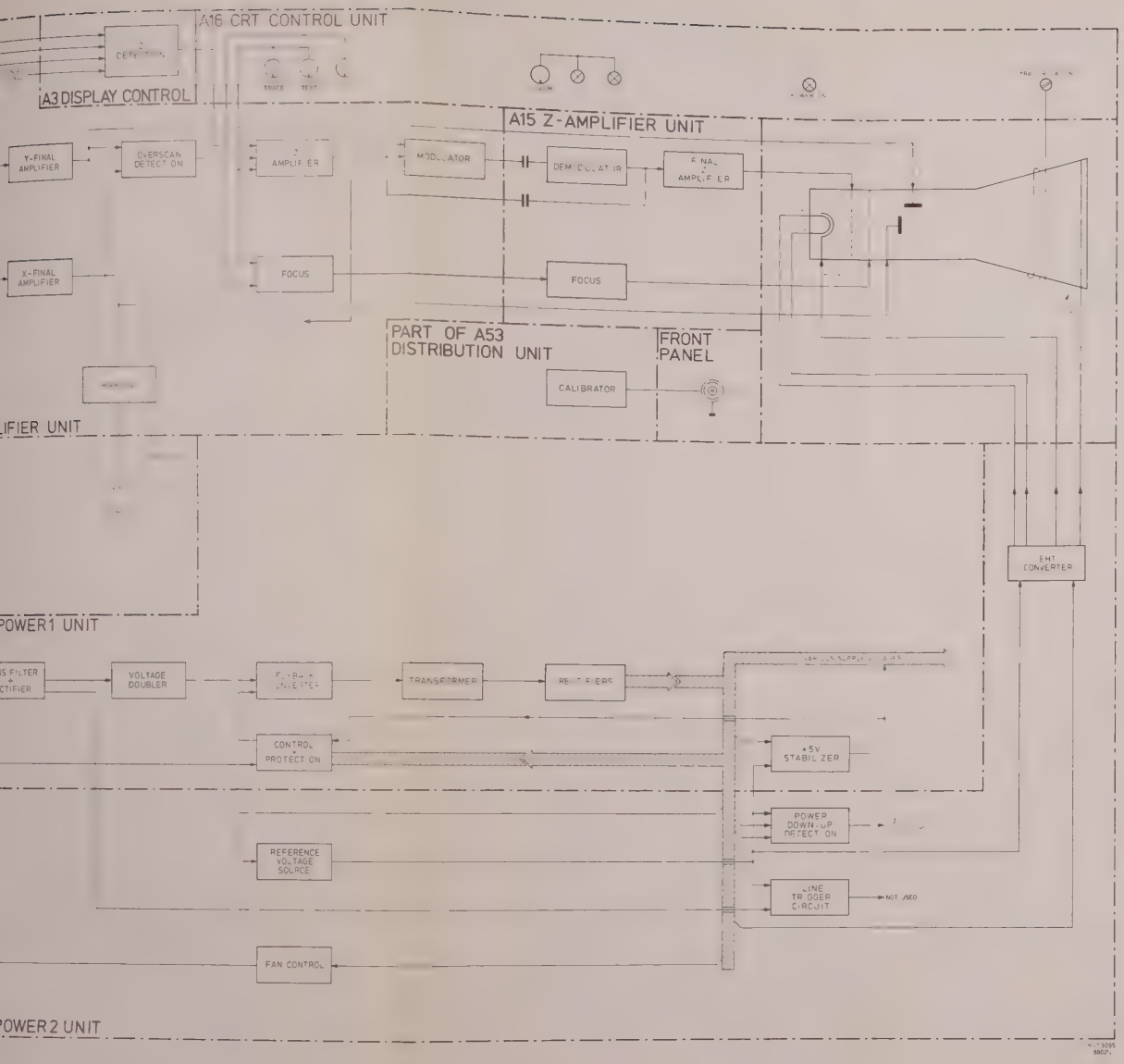


Figure 6.2 Detailed blockdiagram (part 2).

INTRODUCTION TO CIRCUIT DESCRIPTIONS 7

INTRODUCTION TO CIRCUIT DESCRIPTIONS

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7.1 General..... 7-1
7.2 Explanation of signal name set up..... 7-1
7.2.1 Signal names..... 7-1
7.2.2 Signal name list..... 7-2

7.0 INTRODUCTION TO CIRCUIT DESCRIPTIONS

7.1 GENERAL

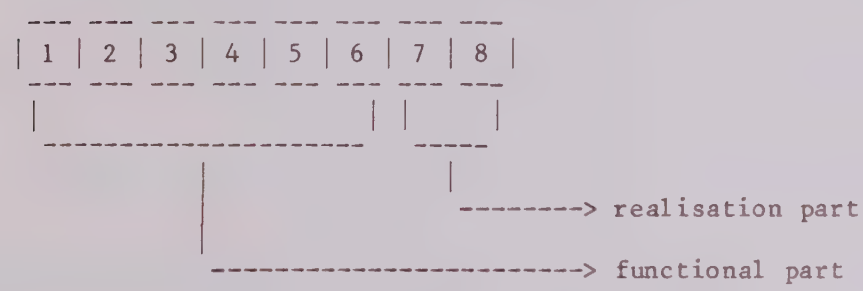
The functioning of the circuits is explained in chapter 8.0 "CIRCUIT DESCRIPTION" per unit in the sequence of the unit numbers (A ..). Every unit section contains the circuit description, the lay-out of the p.c.b., the circuit diagram(s) and a signal-name list, indicating the signal sources and signal flow.

7.2 EXPLANATION OF SIGNAL NAME SET UP

7.2.1 Signal names

Signal names consists of 2 parts:

- a functional part of maximal 6 characters
- a realisation part of 2 characters



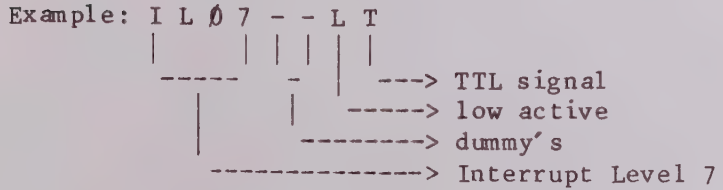
The realisation part is optional. If it is used then the functional parts should consist of 6 characters. If necessary dummy's (minus signs) are used in the functional part, to make it 6 characters long.

The first character of the realisation part has the following meaning:

H: active high signal
L: active low signal
X: irrelevant (e.g. counter outputs)

The second character of the realisation part is used to identify signal levels:

A: analogue
E: ECL -4,5V or -5,2V
T: TTL 5V or HCT
X: other levels



Sometimes the functional part can also be used for a serial number e.g. to indicate a buffered version of a signal.

Example: CHPT--Ø1

7.2.2 Signal name list

Each unit description in chapter 8.0 "CIRCUIT DESCRIPTIONS" contains a list with the signal names used in that unit given in alphabetical order.
Behind each name, a description is given and is mentioned on which unit the signal is generated.
Only if the signal is generated on the unit itself, the other units on which the signal is used (signal destination(s)) are mentioned, otherwise a minus sign is filled in.
If the signal flows over more units in sequence, the path is indicated.

Example: The battery voltage (BAVO) comes from unit A66 via A20, A19 and A12 to A6. On unit A66 is indicated: A20-A19-A12-A6.

Some signals may have more signal sources, because the sources have open collector output circuits, or 3-state output circuits.
In this case the sources are mentioned, separated with a plus (+) sign.
As signal source is always indicated, the unit where the signal is generated.

Example: On units A20, A19, A12 and A6, unit A66 is indicated as source.

A number of power supply lines and ground lines, which are generated on POWER 1 unit A19, are not mentioned on the signal name lists because they appear in almost every unit.
These signal names can be found on the signal name list of POWER 1 unit A19 itself, and are in the destination column indicated with "general".
Power supply lines, which are derived from the power supply lines mentioned above, are also not mentioned in the list.

The destinations of the data-bus and address-bus lines from the microprocessor system on MICROPROCESSOR unit A6 are also indicated with "general", because almost all units are involved. This is also done for the signals UPRD--LT (microprocessor read) and UPWR--LT (microprocessor write).

CIRCUIT DESCRIPTIONS 8

CIRCUIT DESCRIPTIONS

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8.6	A6	uP BOARD	8.6-1
8.7	A7	OPTION 1 (IEEE 488/RS232-C)	8.7-1
8.8	A8	DPU CONTROL	8.8-1
8.9	A9	DPU	8.9-1
8.10	A10	OPTION 2	8.10-1
8.11	A11	ADC + T&H	8.11-1
8.12	A12	MOTHER BOARD	8.12-1
8.13	A13	FRONT 1	8.13-1
8.14	A14	FRONT 2	8.14-1
8.15	A15	Z-AMPLIFIER	8.15-1
8.16	A16	CRT CONTROL	8.16-1
8.17	A17	SOFTKEY UNIT	8.17-1
8.18	A18	SMOOTH + DOTS	8.18-1
8.19	A19	POWER 1	8.19-1
8.20	A20	POWER 2	8.20-1
8.25	A25	MANAGEMENT UNIT	8.25-1
8.31	A31	TRIGGER INPUT UNIT	8.31-1
8.32	A32	THREE STAGE TRIGGER UNIT	8.32-1
8.34	A34	TRIGGER CONTROL UNIT	8.34-1
8.51	A51	TIME-BASE UNIT	8.51-1
8.52	A52	FAST RAMP UNIT	8.52-1
8.53	A53	DISTRIBUTION UNIT	8.53-1
8.54	A54	GATE UNIT	8.54-1
8.55	A55	VERTICAL SIGNAL UNIT	8.55-1
8.56	A56	TRIGGER PICK OFF UNIT	8.56-1
8.57	A57	INPUT UNIT	8.57-1
8.66	A66	REAR MODULE	8.66-1
8.69	A69	DELAY LINE UNIT	8.69-1

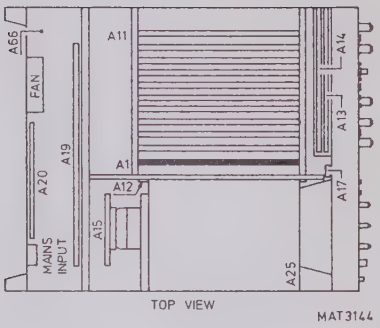
8.0 CIRCUIT DESCRIPTIONS

The functioning of the circuit is explained in this chapter. It is done per unit and in unitnumber (A..) sequence.

Every unit section contains a circuit description, the lay-out of the p.c.b., the circuit diagram(s) and a signal-name list.

See also chapter 7.0 "INTRODUCTION TO CIRCUIT DESCRIPTIONS".

UNIT A1 - FINAL AMPLIFIER UNIT



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8.1.1 General information

This unit basically comprises the vertical and horizontal final amplifiers, the overscan detection circuit, the Z-amplifier, the calibrator circuit and the analog plot interface.

8.1.2 Vertical final amplifier

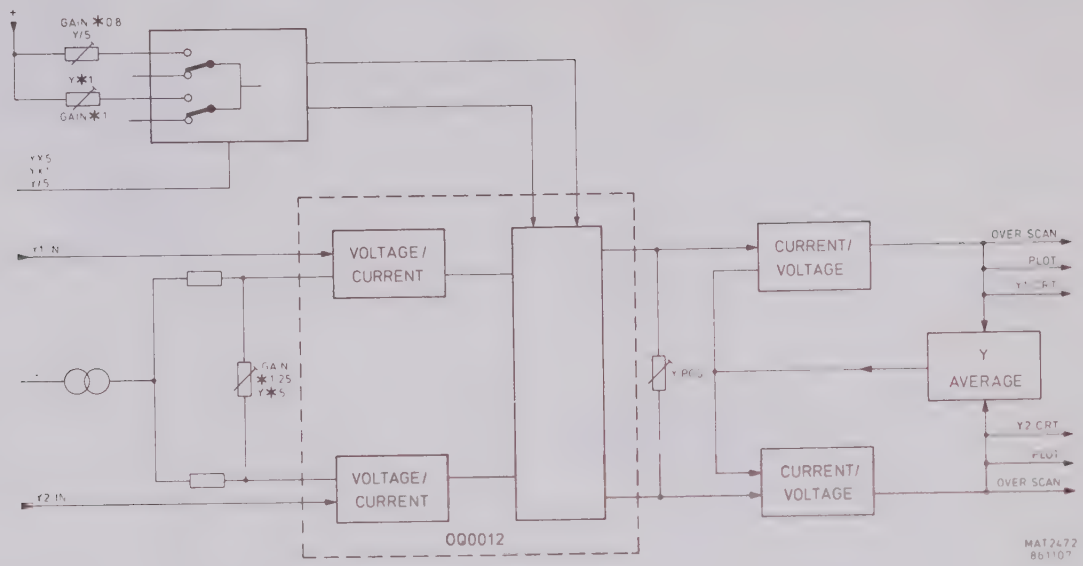


Figure 8.1.1 Blockdiagram Y-final amplifier.

The output signals Y1IN and Y2IN from the DISPLAY DAC UNIT A2 are applied to a voltage/current converter of which the x1,25 (Y*5-mode) gain can be adjusted by potentiometer R2531 in the emitter circuit of the input transistor of D2507.
Furthermore, the gain can be influenced for the Y*1 and the Y/5 mode.
Two sections of multiplexer D2501 can be switched by the signals ANEPY-HT (analog expand) and ANCPY-HT (analog compress) from DISPLAY CONTROL UNIT A3.
The switching is done according the following table:

MODE	ANCPY-HT	ANEPY-HT	analog expand factor (UNIT A1)	digital expand factor (UNIT A2)
Y/5	1	Ø	x0,8	/4
Y*1	Ø	Ø	x1	x1
Y*5	Ø	1	x1,25	x4

An additional circuit can be switched in for the x1 gain (adjustable with potentiometer R2513) and and additional circuit can be switched in for the x0,8 gain (adjustable with potentiometer R2516).
The selection depends on the user selection of the Y*5, Y*1 or the Y/5 mode.

Output points 12/13 and 14/15 of the MULTIPLIER D2506 are applied to current/voltage converters in the Y-OUTPUT stage of which the balance can be adjusted by potentiometer R2533.

The average value of the signals Y1 and Y2 is fed back to the input of the X-OUTPUT stage to keep the average value constant.

The signals X1 and X2 are applied to the vertical deflection plates of the C.R.T., to the OVERSCAN DETECTION circuit on unit A1 and also to the PLOT INTERFACE on this unit A1.

8.1.3 Horizontal final amplifier

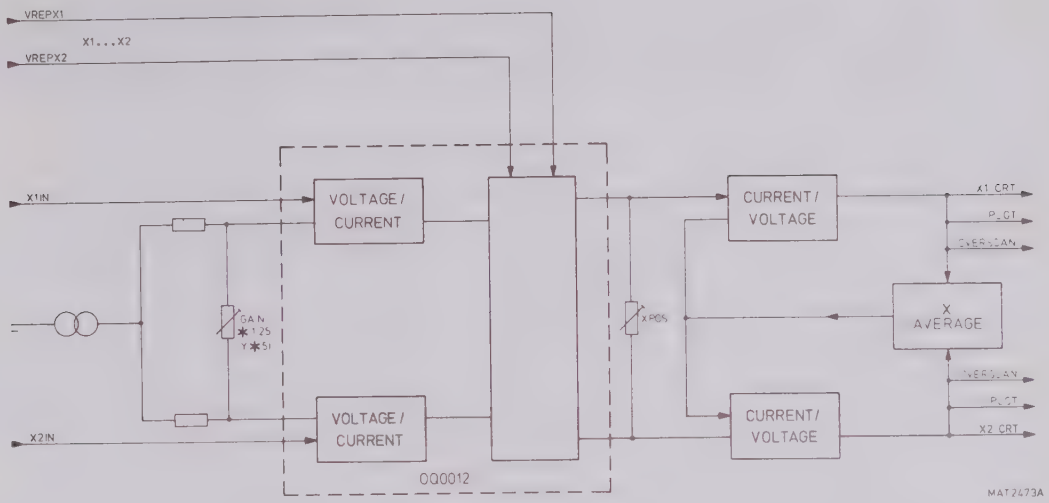


Figure 8.1.2 Blockdiagram X-final amplifier.

The output signals X1IN and X2IN from the DISPLAY DAC UNIT A2 are applied to a voltage/current converter of which the x1 gain can be adjusted by potentiometer R2566 in the emitter circuit of the input transistors of D2507.

Furthermore, the gain can be influenced by signals VREPX1 and VREPX2 which carry a variable X-EXPAND factor between x1/2 (EXPAND x1) and x1 (EXPAND x2). This factor, which is user selected, is multiplied in the stage D2507 to vary the X-gain.

Output points 12/13 and 14/15 of the MULTIPLIER D2507 are applied to current/voltage converters in the X-OUTPUT stage of which the balance can be adjusted by potentiometer R2571.

The average value of the signals X1 and X2 is fed back to the input of the X-OUTPUT stage to keep the average value constant.

The signals X1 and X2 are applied to the horizontal deflection plates of the C.R.T., to the OVERSCAN DETECTION circuit on unit A1 and also to the PLOT INTERFACE on this unit A1.

8.1.4 Trace/Text intensity

The levels ITTR from the TRACE INTENS frontpanel control and ITTX from the TEXT INTENS frontpanel control on C.R.T. CONTROL UNIT A16, are applied to one section of multiplexer D2501. This section, which is switched by the signal DPTR--HT (display trace), switches the trace intensity level to the Z-amplifier when traces have to be displayed and the text intensity level when texts have to be displayed.

8.1.5 Overscan detection

The output signals Y1, Y2, X1 and X2 from the vertical and horizontal final amplifiers are applied to an overscan detection circuit where they are compared with four overscan levels for the top, bottom, left and right sides of the trace area on the C.R.T. screen.

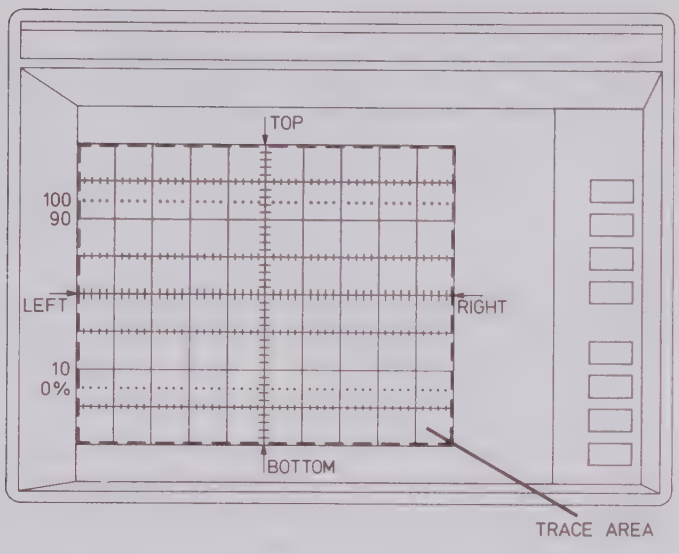


Figure 8.1.3 Overscan detection.

These levels can be adjusted by potentiometers R2658, R2659, R2678 and R2682 in such a way that during the display of traces, the traces can never be displayed outside the trace area on the C.R.T. screen.
In case of overscan a blanking signal is produced by the collector of transistor V2623 and this signal is applied to the Z-amplifier to blank the trace.
The overscan detection circuit can be disabled during text display and enabled during trace display by the signal DIOS--HT (disable overscan) via transistor V2611.

8.1.6 Z-amplifier

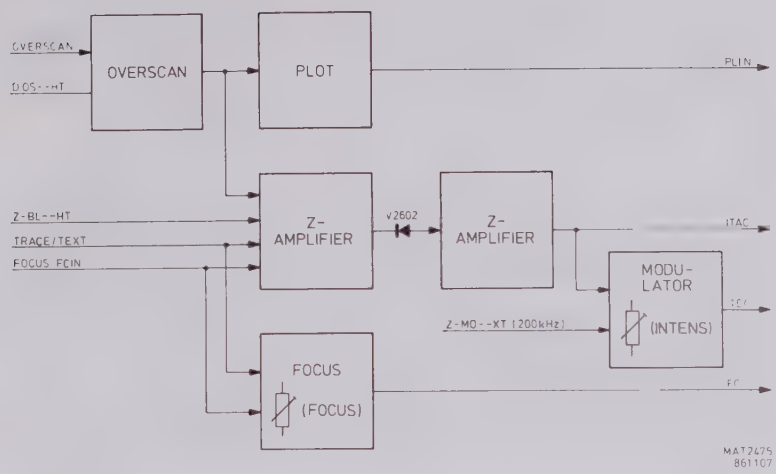


Figure 8.1.4 Blockdiagram Z-circuit.

INTENS

The Z-circuit is controlled by a number of different inputs:

- Overscan
- Z-blank signal
- TRACE or TEXT intensity control level
- FOCUS control level

The signals are applied to a Z-amplifier and the output of this amplifier is guided along two different signal path's. A high frequency component signal path (signal ITAC) and a low frequency component signal path (signal ITDC).
Signal ITAC is directly applied to Z-AMPLIFIER UNIT A15 and from there via a high voltage capacitor to the high voltage part of the circuit and to the intensity grid G1 of the C.R.T..

The low frequency component is applied to a modulation circuit, it can be influenced by a fine adjusting potentiometer R2637 and afterwards modulated with a frequency of 200 kHz from signal Z-MO--XT from the clock generator on the uP unit A6.
The resulting signal ITDC is applied to Z-AMPLIFIER unit A15 and via Z-circuit transferred via a high voltage capacitor to the high voltage part of the circuit. It is then demodulated, combined with the high frequency component and applied to the intensity grid G1 of the C.R.T..

FOCUS

The FOCUS circuit is influenced by the setting of the front panel FOCUS controls as well as the setting of the TRACE and TEXT intensity controls. The last is needed for the auto focus control when the intensity is changed with one of the frontpanel TRACE or TEXT intensity controls. There is also a fine adjustment potentiometer R2609.
The resulting signal FC is applied to the focus circuit on Z-AMPLIFIER UNIT A15 and from there to the focus grid G3 of the C.R.T..

8.1.7 Calibrator

This calibrator circuit is not used in this instrument.
The calibrator can be found on the Distribution unit A53 (see section 8.53).

8.1.8 Plot interface

The output signals Y1, Y2, X1 and X2 from the vertical and horizontal final amplifiers are applied to a plot interface where they are prepared to be plotted via the rear panel analog plot output socket.

The X-output gain can be adjusted with potentiometer R2728 and the Y-output gain with potentiometer R2738.
Sample and hold signal SAPL activates the interface for a plot action. Signals are only applied to the output socket when enabled by signal PLZEOT if a value is stored in the sample and hold circuit.

A pen lift circuit is activated via the PLIN signal (when an overscan is detected). The penlift flip flop can be reset by the PEN UP signal PU----LT.

The pen lift polarity can be influenced by signal PFPY via exclusive or circuit D2504.

8.1.9 Signal-name list

UNIT A1

Signal name	Description	Signal source	Signal destination(s)
ANCPY-HT	Analog compress Y	A3	-
ANEPY-HT	Analog expand Y	A3	-
DIOS--HT	Disable overscan	A3	-
DPTR--HT	Display trace	A3	-
FC	Focus	A1	A15
FCIN	Focus input	A16	-
ITAC	Intens a.c. component	A1	A15
ITDC	Intens d.c. component	A1	A15
ITTR	Intensity trace	A16	-
ITTX	Intensity text	A16	-
PENLIFT	Penlift	A1	A66
PLIN	Plot input	A1	A1
PFPY	Penlift polarity	A3	-
PLZEOT	Plot zero output	A3	-
PU----LT	Pen-up	A3	-
SAPL	Sample plot	A3	-
X1	X1 input for C.R.T.	A1	A15-C.R.T.
X2	X2 input for C.R.T.	A1	A15-C.R.T.
X1IN	X1 input final amplifier	A2	-
X2IN	X2 input final amlpifier	A2	-
X-PL	X plot	A1	A66
Y1	Y1 input for C.R.T.	A1	A15-C.R.T.
Y2	Y2 input for C.R.T.	A1	A15-C.R.T.
Y1IN	Y1 input final amplifier	A2	-
Y2IN	Y2 input final amplifier	A2	-
Y-PL	Y plot	A1	A66
VREPX1...X2	Variable expand X	A2	-
Z-BL--HT	Z-blanking	A3	-
Z-MO--XT	Z-modulation (200 kHz)	A6	-

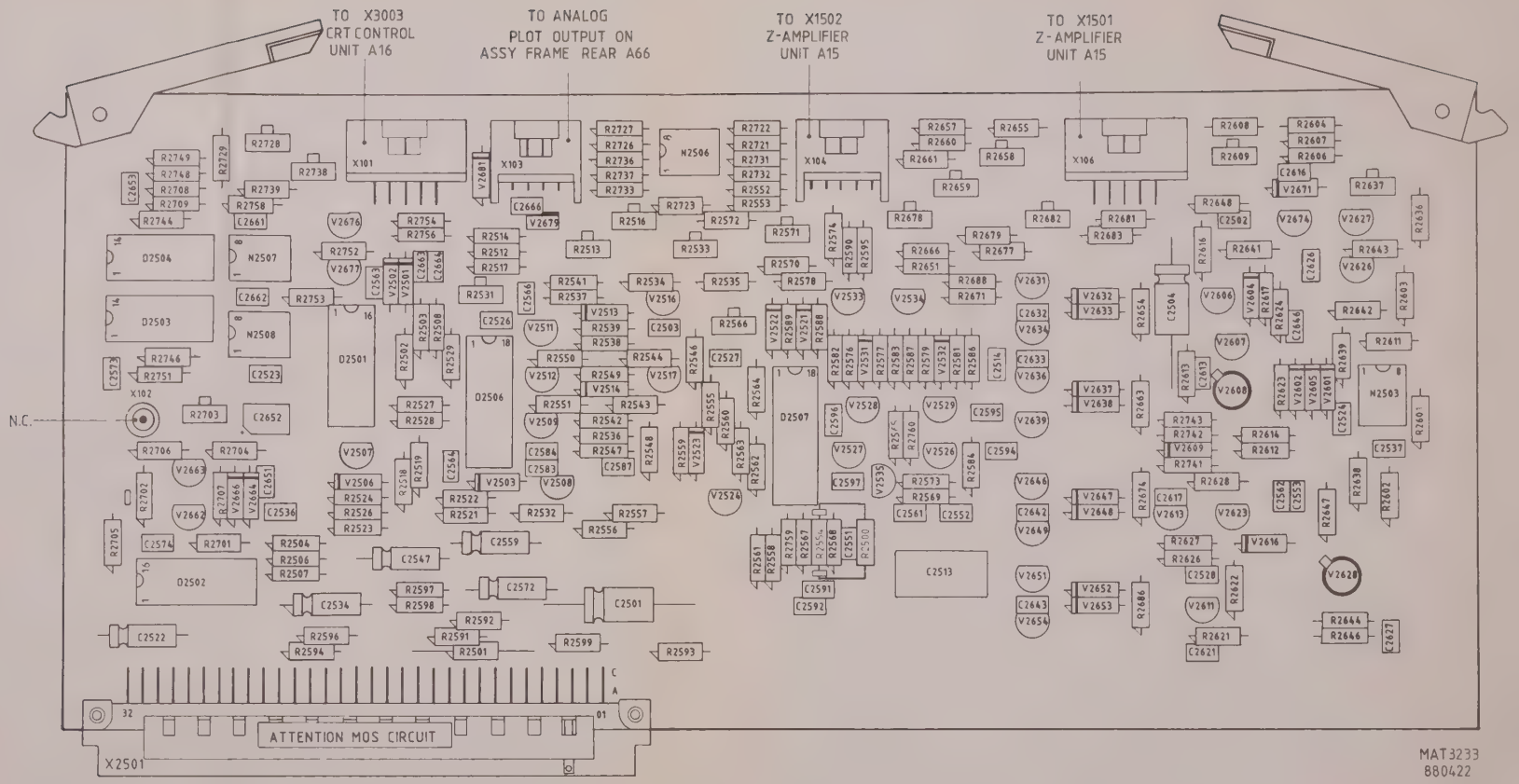


Figure 8.1.5 Unit A1 - FINAL AMPLIFIER UNIT - p.c.b. lay-out.

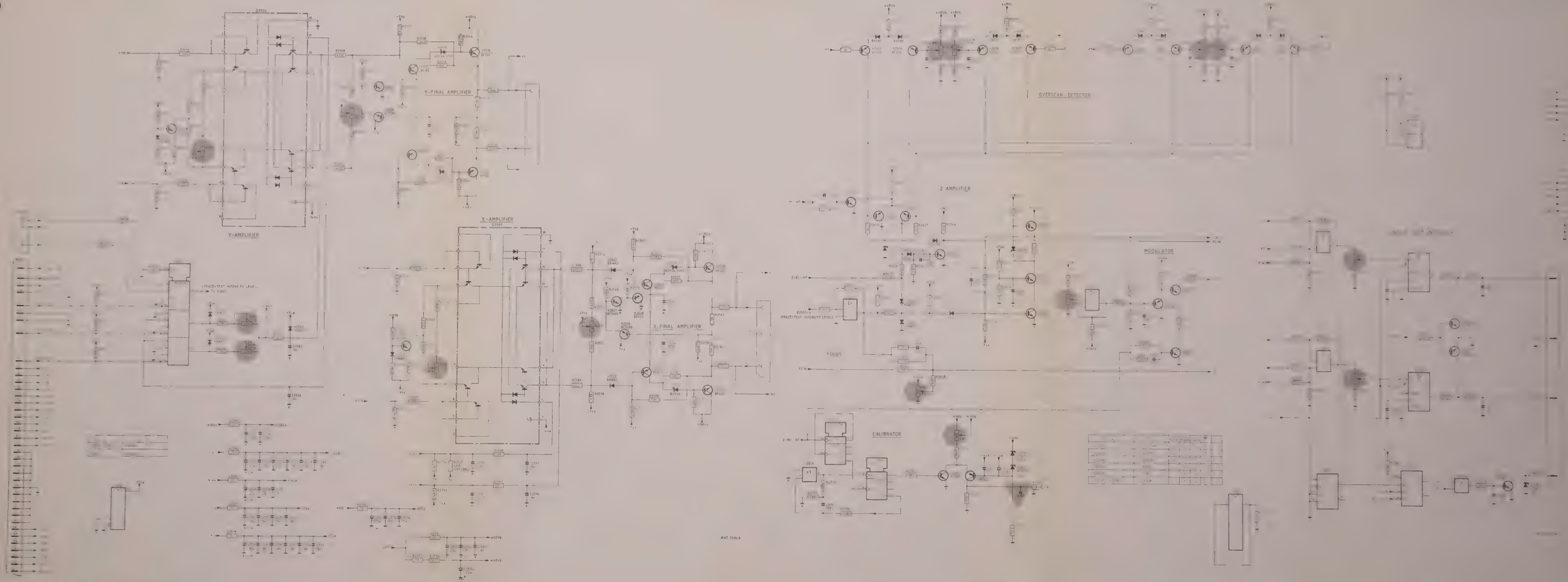
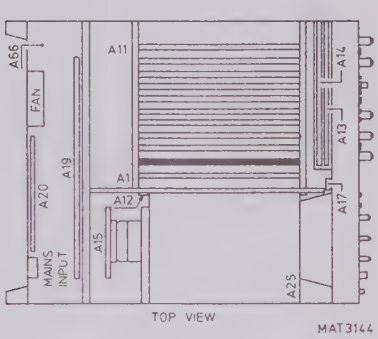


Figure 8.1.6 Unit A1 - FINAL AMPLIFIER UNIT - circuit diagram.

UNIT A2 - DISPLAY DAC UNIT



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8.2.4 X-Variable data path..... 8.2-11
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8.2.1 General information

This unit basically comprises the vertical and horizontal position adders and the vertical and horizontal digital to analog converters.

8.2.2 Vertical data path

The vertical trace data as well as all kinds of vertical text data on the ten output lines DCDBØØ...DCDBØ9 of the display control latch is applied to a combined invert/vertical-expand/latch circuit. This circuit consists of the two (not identical) field programmable logic sequencers (FPLS) D2301 and D2302 and the D-type flip flops D2309.
The control signal IVDCDB determines whether the data bits have to be inverted or not and the two control signals EPY-ØØ and EPY-Ø1 determine the vertical expand factor of the circuit.

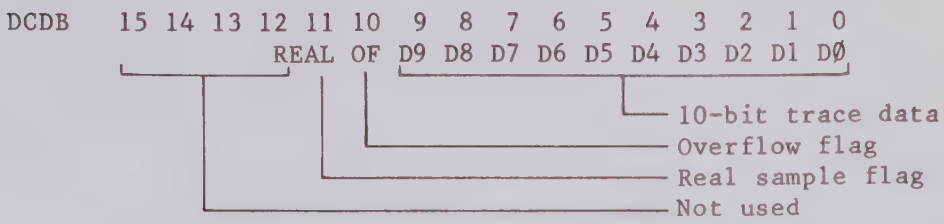
Vertical expand factor	Control signals		Digital expand factor (UNIT A2)	Analog expand factor (UNIT A1)
	EPY-Ø1	EPY-ØØ		
Y/5 (trace)	0	0	/4	/1,25
Y*1 (trace + MSC text)	0	1	x1	x1
line + softkey text	1	0	x4	x1
Y*5 (trace)	1	1	x4	x1,25

The combination of the digital expand factor on the display dac unit A2 and the analog expand factor on the final amplifier unit A1 results in the total required expand factor.
Digital expand is realized by the shifting of the bit pattern two bits to the right (/4) or two bits to the left (x4).
The resulting vertical data is then latched in the output latches of the FPLS circuits and in the four D-type flip flops by signal CKEPVE.

The data can be divided into five different kinds of data.

1) Trace data for X=t display:

Data format:



The trace data can be inverted, expanded by factors /5, x1 or x5 before it is applied as EPVEØØ...EPVE11 to the vertical position adder.

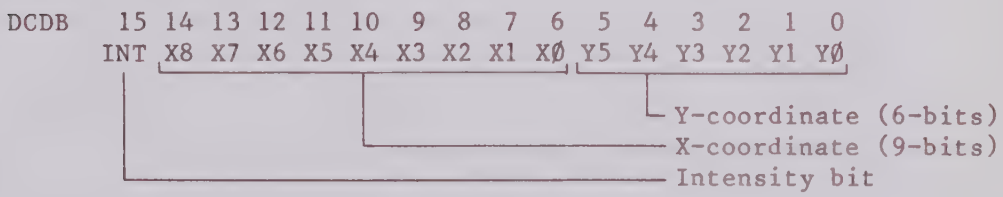
2) Trace data for AVSB display:

Data has the same format as for X=t display which is described before. However, only channel B is latched and applied to the vertical position adder.

3) Line text display:

Top area text (TAT)
Trace area text (TRAT)
Bottom area text (BAT)

Data format:



Only 10 bits DCDBØØ...DCDBØ9 of this bit pattern are applied to the circuit and only the Y-coordinate bits YØ...Y5 are of interest.
The data is not inverted but expanded by a factor of x4 by shifting the pattern two bits to the left and switching the lowest two bits to zero. Signal ENTXLNLT is active and the output bits EPVEØ8...EPVE11 of D2309 are switched to one.

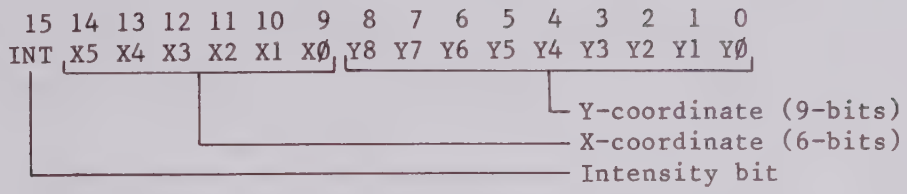
The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	1	1	1	1	Y5	Y4	Y3	Y2	Y1	YØ	Ø	Ø

This pattern is applied to the vertical position adder.

4) Softkey text display (SKT):

Data format:



Only 10 bits DCDBØØ...DCDBØ9 of this bit pattern are applied to the circuit and only the nine Y-coordinate bits YØ...Y8 are of interest.
The data is not inverted but expanded by a factor of *4 by shifting the pattern two bits to the left and switching the lowest two bits to zero.

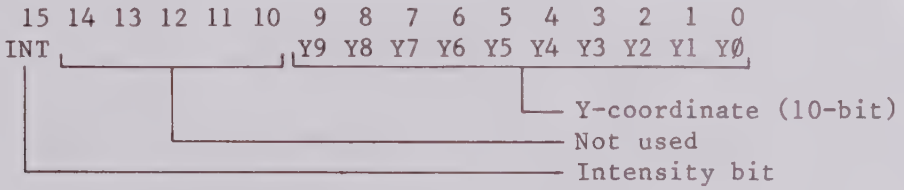
The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	Ø	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	YØ	Ø	Ø

This pattern is applied to the vertical position adder.

5) Miscellaneous text (MCS):

Data format Y-coordinates:



For miscellaneous text, two words, one carrying the Y-coordinate and the other one carrying the X-coordinate, are placed in the text memory for each dot to be displayed.
Only the 10 bits DCDBØØ...DCDBØ9 of the Y-coordinate pattern are applied to the circuit.
The data is not inverted and not expanded.

The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	Ø	Ø	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	YØ

This pattern is applied to the vertical position adder.

The output signal Z-OTØ1LT of the first FPLS circuit D2301 is applied to the second one and the output signal Z-OTØ2LT of the second FPLS circuit D2302 is applied to a reflection detection circuit.

The vertical position adder is a sixteen bit circuit which consists of D2319, D2321, D2324 and D2326. A sixteen bit vertical position information is latched in the vertical position latches D2314 and D2316 by signal WRVEPOLT and applied to the other adder input side. This vertical position information is calculated by the microprocessor and depends on the selected vertical expand factor, the use of the Y-POSITION control and the type of trace or text which has to be displayed.

The adder output bits VEDBØ9...VEDB11 are carrying information about reflection and are applied to a Z-detection circuit on unit A3. The following combinations result in light on the C.R.T. screen.

VEDB	11	1Ø	Ø9	Ø8
	0	0	0	1
	1	1	1	0

All other combinations result in NO light on the C.R.T. screen. This has no function for text display.

The other ten adder output bits VEDBØØ...VEDBØ9 which carry information in two-complement notation, are first converted by the code convert circuit D2338 into straight binary notation by inverting the highest bit VEDBØ9. These converted ten bits are then latched for a time of 750 ns (time between two dots) in a YDAC latch consisting of D2329 and D2331. This is done by the signal LEDA-1HT. It is then applied to the 10-bits vertical digital-to-analog converter YDAC N2301 which has two symmetrical output current lines.
A constant reference voltage +10VREF from differential amplifier N2304 is applied to the YDAC.
The symmetrical output currents of the YDAC are converted into voltage levels by a Hooper stage with low input impedance and low output impedance. This Hooper stage is formed by the transistors V2301 and V2302. The signals are fed then to sample and hold circuits with switches D2341, capacitors C2366 and C2367 and field effect transistors V2303 and V2303 for the deglitching of the YDAC output signals. This is necessary for dot-join display because the trace is constantly unblanked then.
As long as the YDAC outputs are not stable, the switches D2341 are opened by the signal LEDA-1LT and the previous levels are held (for about 125 ns) over the capacitors C2366 and C2367 and at the inputs of the FET transistors V2303 and V2303. After 125 ns the YDAC outputs are stable and the switches are closed. The capacitors can then be charged to the new YDAC output levels. In this way, the YDAC output glitches are suppressed.

For display of only discrete dots, the S/H output signals are applied via an output buffer of two emitter followers V2304 and V2307 with high input impedance and low output impedance as Y1IN and Y2IN to the inputs of the vertical final amplifier stage on unit A1.

For dot-join display an RC-filter with an RC-time of 750 ns (1 dot cycle) can be switched in.
With signal DJAC--HT active, capacitor C2373 will be switched in via switch D2341. In this case only the real samples (512) will be connected with each other with lines between the dots.

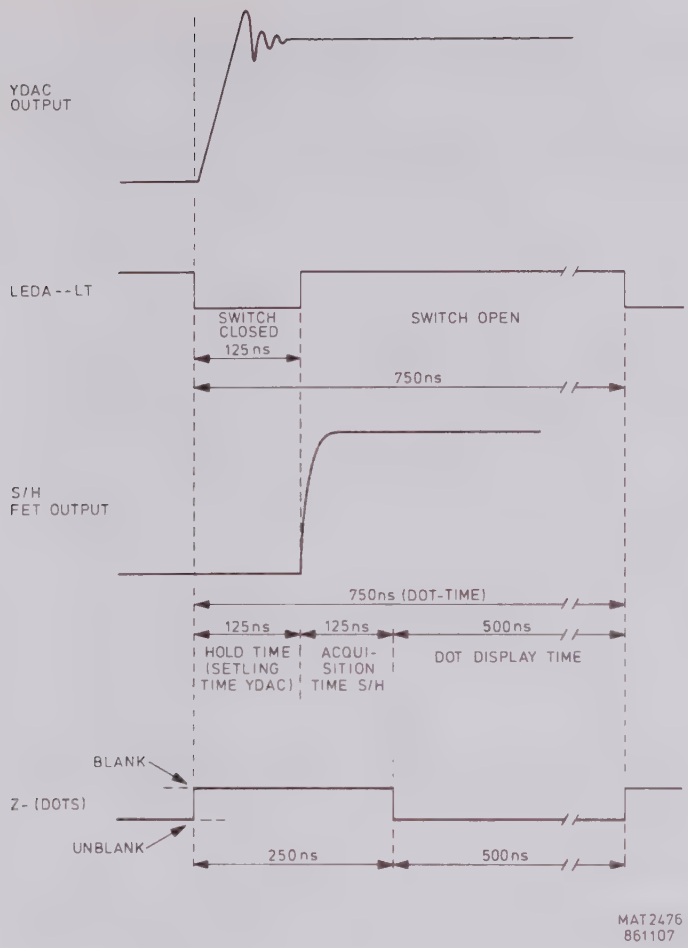


Fig. 8.2.1 Dot cycle

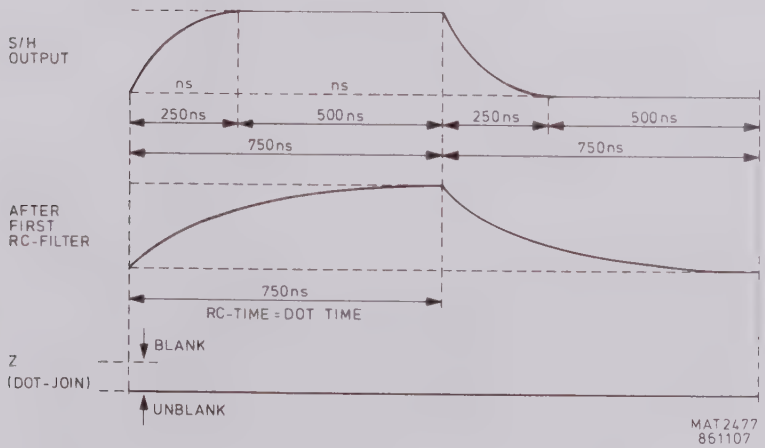


Fig. 8.2.2 Dot join cycle

8

For smooth display not only the dot-join filter is switched in, but also the smooth filter which gives a total RC-time of 7,5 us (10 dot cycles).
This second RC-filter is switched in when signal SM----LT is activated. Capacitor C2369 is switched in via switch D2342 and lines are displayed over ten dots.

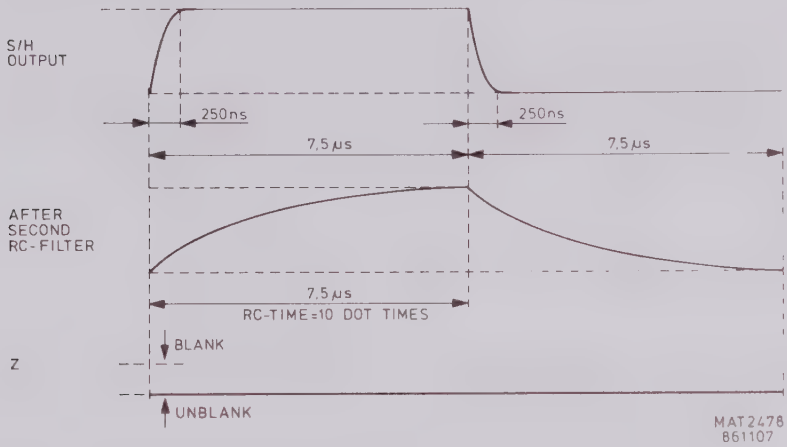


Fig. 8.2.3 Smooth cycle

NOTE: In this instrument the smooth circuit is not activated.

8.2.3 Horizontal data path

Horizontal data on the expand data bus lines EPDBØØ...EPDB111 can be divided into five kinds of data.

1) Address data for X=t display:

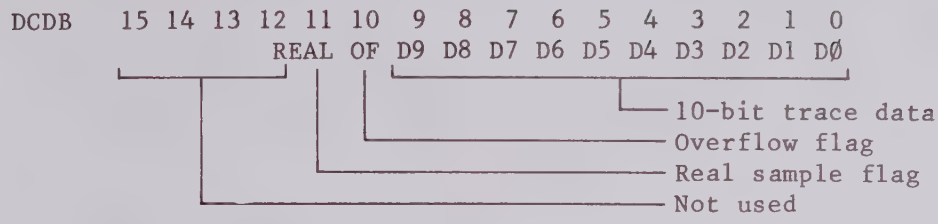
Data format:

DPAB	11	10	9	8	7	6	5	4	3	2	1	0
A	11	10	9	8	7	6	5	4	3	2	1	Ø

12-bit address data from the display address counter on unit A3.

The state of the display address counter is used for horizontal deflection during normal X=t display.
This data is applied to the expand data bus lines EPDBØØ...EPDB11 via the display address data buffer, which consists of D2121 on unit A3 and a part of D2122 on unit A3, when signal HOMO is active.

2) Trace data for AVSB display:



Vertical trace data bits DCDBØØ...DCDBØ9 of channel A for X-deflection in A versus B mode is applied to the expand data bus lines EPDBØØ...EPDB11 via the AVSB trace data buffer, which consists of D2303 and a part of D2304. This buffer is active when signal ENTRHOLT is activated.
The highest bit is inverted by the code convert circuit D2337 to convert the trace data from two-complement notation to straight binary notation. (For channel B this is done in the vertical channel path).
Via the AVSB trace data buffer the data is multiplied by a factor of four to adapt it to the higher horizontal resolution.

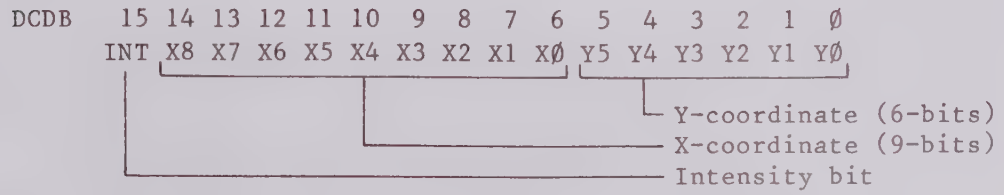
The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	0
	D9	D8	D7	D6	D5	D4	D3	D2	D1	DØ	Ø	Ø

This pattern is applied to the horizontal expand I circuit.

3) Line text display: Top area text (TAT)
Trace area text (TRAT)
Bottom area text (BAT)

Data format:



Only the 9 X-coordinate bits DCDBØ6...DCDB14 or XØ...X8 are of interest. These bits are applied to the expand data bus lines via the line text data buffer which consists of a part of D2304 on unit A2 and D2124 on unit A3. This buffer is active when signal ENTXLNLT is active. The data is via this line text data buffer expanded to twelve bits of which the lowest three bits are made zero.

The final bit pattern is:

EPDB	11	10	9	8	7	6	5	4	3	2	1	Ø
	X8	X7	X6	X5	X4	X3	X2	X1	XØ	Ø	Ø	Ø

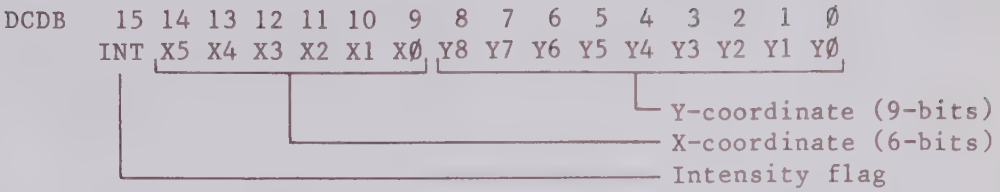
This pattern is applied to the horizontal expand I circuit.

In line text display mode, the X-variable is automatically set by the microprocessor to *1,5.

This results in 512 horizontal text dot positions over 15 divisions, so with a dot distance of 0,293 mm.

4) Softkey text display (SKT):

Data format:



Only the six X-coordinate bits DCDBØ9...DCDB14 or XØ...X5 are of interest. These bits are applied to the expand data bus lines via the softkey text data buffer which consists of D2133 on unit A3 and a part of D2122 on unit A3. This buffer is active when signal ENTXSKLT is active. The data is converted to twelve bits via this buffer. The highest three as well as the lowest three bits are made zero.

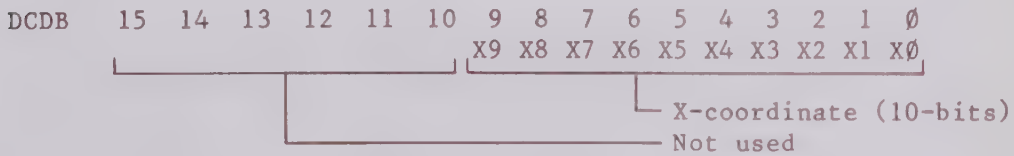
The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	Ø
	Ø	Ø	Ø	X5	X4	X3	X2	X1	XØ	Ø	Ø	Ø

In softkey text display-mode the X-variable is automatically set to *1,5 by the microprocessor.
This results in 512 horizontal text dot positions over 15 divisions, so with a dot distance of 0,293 mm.

5) Miscellaneous text (MSC):

Data format X-coordinates:



For miscellaneous text, two words, one carrying the Y-coordinate and the other one carrying the X-coordinate, are placed in the text memory for each dot to be displayed.
Only the 10 bits DCDBØØ...DCDBØ9 of the X-coordinate pattern are applied to the circuit. The data is not expanded and the X-variable is set to *1.

The final bit pattern is:

EPVE	11	10	9	8	7	6	5	4	3	2	1	Ø
	X9	X8	X7	X6	X5	X4	X3	X2	X1	XØ	Ø	Ø

The pattern is applied to the horizontal expand I circuit.

The expand databus is connected to the horizontal expand I circuit consisting of a number of multiplexers. The first group D2305, D2307 and D2308 is able to shift the input bit pattern one bit to the left or not. This means that an expand factor *1 is selected if signal EXP-ØØ is "Ø" and that an expand factor of *2 is selected if signal EXP-ØØ is "1". The second group D2311, D2312 and D2313 is able to shift its input bit pattern two bits to the left or not.

This means that an expand factor *1 is selected if signal EXP-Ø1 is "Ø" and that an expand factor of *4 is selected if signal EXP-Ø1 is "1".
The combination of these two groups results in a circuit of which the expand factor can be switched to *1, *2, *4 or *8 depending on the signals EXP-ØØ and EXP-Ø1.

The twelve lines EPHOØØ...EPHO11 of the expand horizontal data bus are applied to one input side of a sixteen bit horizontal adder circuit which consists of D2322, D2323, D2327 and D2328.
A sixteen bit horizontal position information is latched in the horizontal position latches D2317 and D2318 by signal WRHOPOLT and applied to the other adder input side.
This horizontal position information is calculated by the microprocessor and depends on the selected horizontal expand factor, the use of the X-POSITION control and the type of trace or text which has to be displayed.

The signals HODB13, HODB14 and HODB15 are applied to a reflection detection circuit.

The adder output bits HODBØØ...HODB12 are applied to a horizontal expand II circuit which consists of the multiplexers D2333, D2334 and D2336. This circuit can be switched for and expand factor *1, when signal EPX-Ø2 is "Ø" and to a factor *8, when signal EPX-Ø2 is "1".

*1 The address range is shifted three bits to the left resulting in 512 horizontal display positions over ten divisions

*8 Only the lowest 10 bits of the address range is used resulting in an horizontal expand factor of *8.

Data is latched in the multiplexers by signal LEDA--LT and DPRJ.

Ten bits of the horizontal expand II circuit output data are applied to the 10-bits horizontal digital to analog converter XDAC (N2303) which has two symmectrical output current lines. A constant reference voltage +10VREF from differential amplifier N2304 is applied to the XDAC. The symmetrical output currents of the XDAC are furthermore handled like already described under 8.2.2. for the vertical data path. Afterwards they are applied as X1IN and X2IN to the inputs of the horizontal final amplifier stage on unit A1.

8.2.4 X-variable data path

X-variable data which depends on the use of the X-EXPAND rotary controls, is calculated by the microprocessor and placed on the data bus lines DBØ8...DB15. It is then latched in the X-variable latch D2332 when signal WRHOVRLT is active.
It is then applied to an 8-bit X-variable digital to analog converter N2302. A constant reference voltage +10VREF from differential amplifier N2304 is applied to the DAC. The symmetrical output current lines VREPX1 and VREPX2 are applied to the horizontal final amplifier stage on unit A1.

8.2.5 Signal-name list

UNIT A2

Signal-name	Description	Signal source	Signal destination(s)
CKEPVE	Clock expand vertical	A3	-
DBØØ...15	Data bus ØØ...15	A6+option	-
DCDBØØ...Ø9	Display control data bus ØØ...Ø9	A4	-
DIOS--HT	Disable overscan	A3	-
DJAC--HT	Dot join active	A3	-
DPRJUP	Display reject up	A3	-
DPRJDW	Display reject down	A3	-
DPRJDWØ1	Display reject down	A2	A2
ENTRHOLT	Enable trace horizontal	A3	-
ENTXLNLT	Enable text line	A3	-
EPDBØØ...11	Expanded data bus ØØ...11	A2,A3	A2
EPHOØØ...13	Expanded horizontal bus ØØ...13	A2	A2
EPHO14	Expanded horizontal bus 14	A3	-
EPVEØØ...11	Expanded vertical bus ØØ...11	A2	A2
EPVEØ8LT	Expanded vertical bus Ø8	A2	A2
EPVEØ9LT	Expanded vertical bus Ø9	A2	A2
EPX-ØØ...Ø2	Expand X ØØ...Ø2	A3	-
EPY-ØØ...Ø1	Expand Y ØØ...Ø1	A3	-
EP12--LT	Expand 12	A3	-
IVDCDB	Invert display control address bus	A3	-
LEDA--LT	Latch enable DAC	A3	-
LEDA-1LT	Latch enable DAC	A2	A2
LEDA--HT	Latch enable DAC	A3	-
LEDA-1HT	Latch enable DAC	A2	A2
HODBØØ...15	Horizontal data bus ØØ...15	A2	A2
HOPOØØ...15	Horizontal position bus ØØ...15	A2	A2
SM----LT	Smooth	A3	-

Signal-name	Description	Signal source	Signal destination(s)
VEDBØØ...12	Vertical data bus ØØ...12	A2	A2
VEDBØ9LT	Vertical data bus Ø9	A2	A2
VEDBØ9...12	Vertical data bus Ø9...12	A2	A12-A3
VEPOØØ...15	Vertical position bus ØØ...15	A2	A2
VREPX1...X2	Variable expand X	A2	A12-A1
WRHOPOLT	Write horizontal position	A3	-
WRHOVRLT	Write horizontal variable	A3	-
WRVEPOLT	Write vertical position	A3	-
X1IN	X1 input final amplifier	A2	A12-A1
X2IN	X2 input final amplifier	A2	A12-A1
Y1IN	Y1 input final amplifier	A2	A12-A1
Y2IN	Y2 input final amplifier	A2	A12-A1
Z-OTØ1LT	Z-output Ø1	A2	A2
Z-OTØ2LT	Z-output Ø2	A2	A2
Z-OTØ3	Z-output Ø3	A2	A12-A3

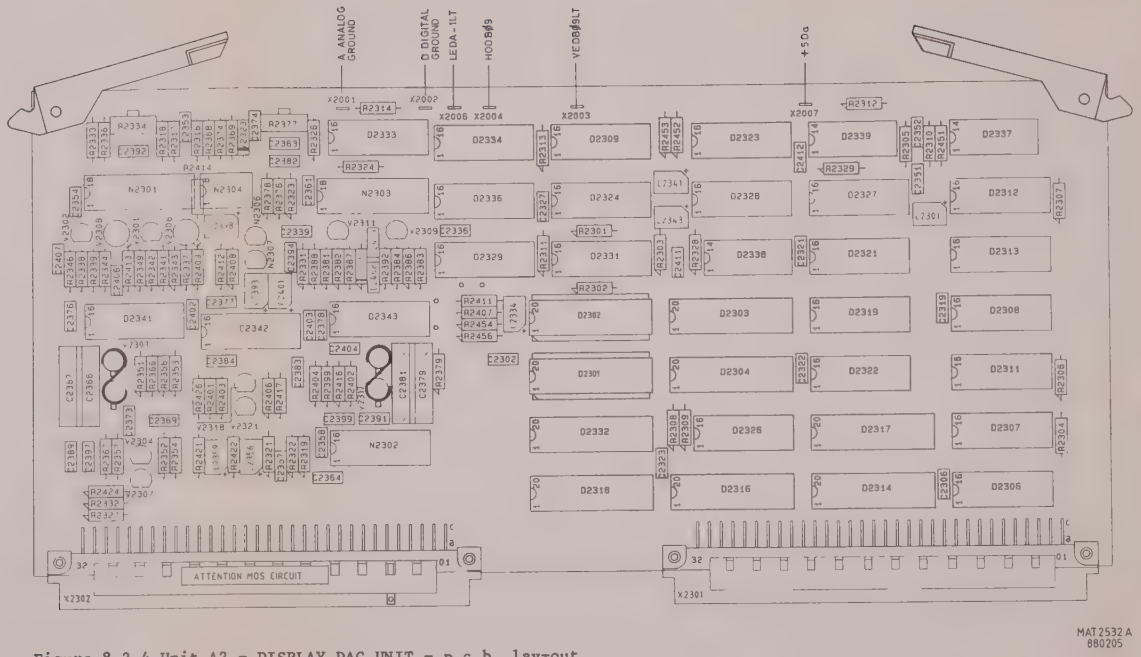


Figure 8.2.4 Unit A2 - DISPLAY DAC UNIT - p.c.b. lay-out.

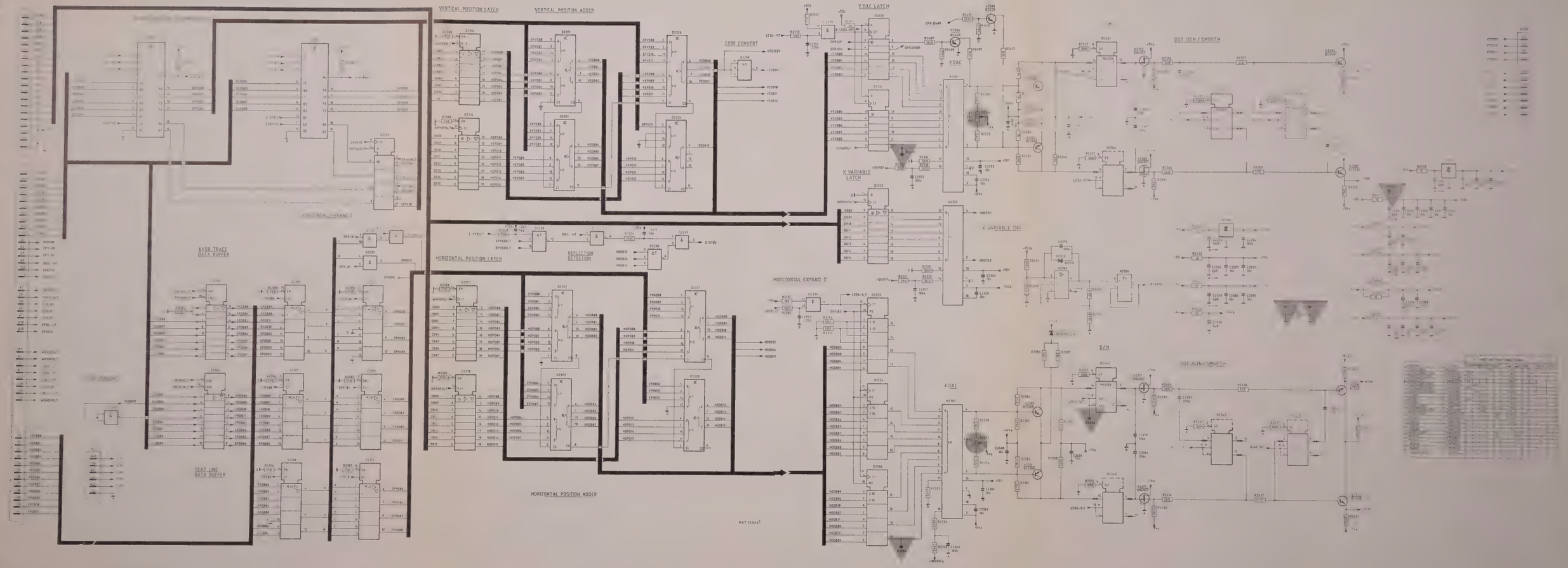
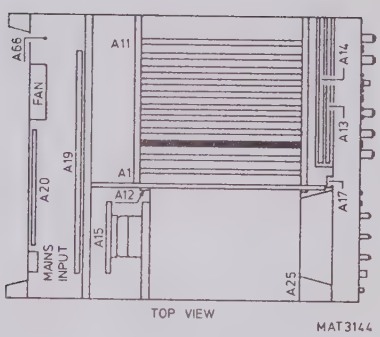


Figure 8.2.5 Unit A2 - DISPLAY DAC UNIT - circuit diagram.

UNIT A3 - DISPLAY CONTROL UNIT



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8.3.2 Display system and timing..... 8.3-2
8.3.3 Circuit descriptions..... 8.3-7
8.3.4 Signal-name list..... 8.3-12

8.3.1 General information

This unit contains the circuits needed to control the display circuits on units A2 and A4.

It contains the following circuits:

Data buffer
Preset register
Output ports for display parameters
Display address counter
Data buffers for:
- Display address data
- Softkey text data
- Line text data

Timing circuits:
- Synchronization flip flops
- Data acknowledge flip flop
- Start flip flop
- Smooth delay flip flop

Z + interrupt timer
Z - counter
Interrupt counter + interrupt flip flop
Restart counter
Address decoder
Z - detection circuit
Clock-fase generator
Memory select circuit

8.3.2 Display system and timing

8.3.2.1 Screen lay out

The screen lay out is as follows.

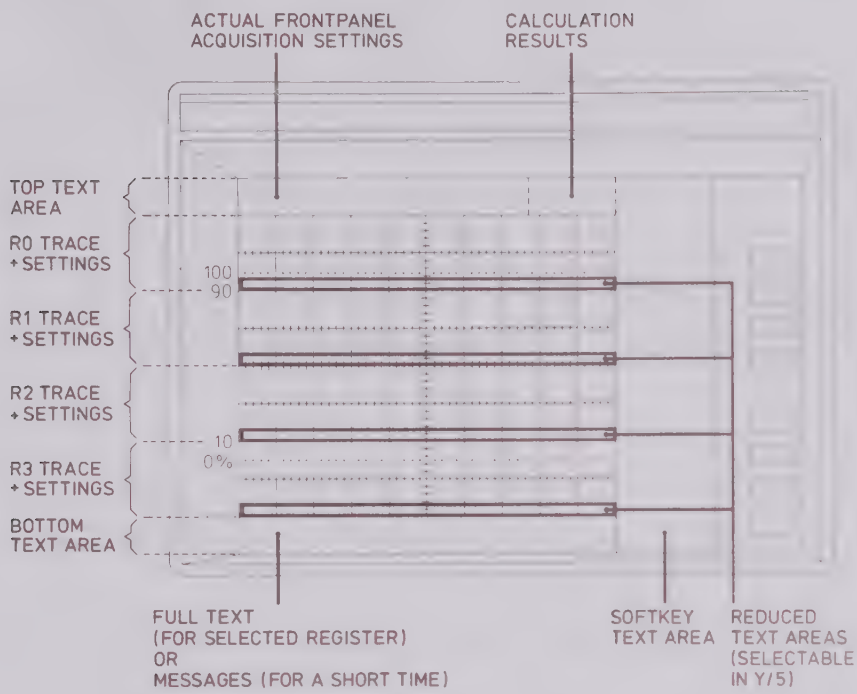


Figure 8.3.1 Screen lay out'.

8.3.2.2 Display cycle

During each complete display cycle of about 19 ms the complete contents of the trace memory as well as the text memory is displayed on the C.R.T. screen.

Each display cycle consists of the following display blocks in sequence:

RØ A and/or RØ B	}
R1 A and/or R1 B	} Contents of the
R2 A and/or R2 B	} trace memory
R3 A and/or R3 B	
TAT	Top text area
RAT RØ	Reduced area text RØ
RAT R1	Reduced area text R1
RAT R2	Reduced area text R2
RAT R3	Reduced area text R3
BAT	Bottom text area
SKT	Softkey area text
MSC	Miscellaneous text (like cursors and channel identification)
PLOT	One dot to plot

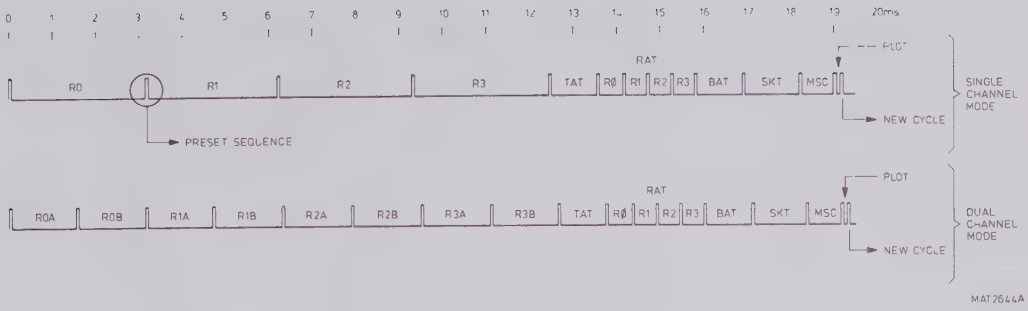


Figure 8.3.2 Display cycle.

8.3.2.3 Preset sequence

After the display of each display block an interrupt level signal ILØ5--LT is send to the microprocessor. The processor in turn starts a preset sequence of new preset values and new parameters for the display circuits. At the end of this preset sequence, signal WRDPSTLT is generated and the display of the next display cycle is started.

Presetting is done in the following sequence:

1 Read overflow bit from DBØØ

2 WRVEPOLT Write the vertical position data to the VERTICAL POSITION LATCH D2314 and D2316 on unit A2.

3 WRHOPOLT Write the horizontal position data to the HORIZONTAL POSITION LATCH D2317 and D2318 on unit A2.

4 WRPSDPLT Write the preset data for the display address counter to the PRESET REGISTER D2103 and D2104 on unit A3.

This is done together with the setting of the signals for the PLOT interface:

PLOT	0 = No sample in S&H
	1 = Sample in S&H
PU----LT	0 = Pen-up
	1 = Pen-down
PFPY	0 = Pen-up (high)
	1 = Pen-up (low)
PLZEOT	0 = Plot output active
	1 = Plot output not active

These four signals are only generated when a plot action has to be performed.

5 WRDPPALT Write the display parameters which are listed below, to the OUTPUT PORTS DISPLAY PARAMETERS D2106 and D2107 on unit A3.

DPMYØ2	DPMYØ1	DPMYØØ	DISPLAY BLOCK
0	0	0	RØ
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	Text TAT/RAT
1	0	1	Text BAT/SKT/MSC
1	1	0	--
1	1	1	--

DPMO--LT Display mode
0 = Dual channel
1 = Single channel

CHID Channel identity
0 = Channel A
1 = Channel B

HOMO Horizontal mode
0 = X=t
1 = AvsB (or text)

SM----LT Smooth
0 = Smooth
1 = No smooth

DIDJ Disable dot join
0 = No dots, dot joined
1 = Dots (or text)

IVDCDB Invert display control databus
0 = No invert
1 = Invert

SVR1 Save to R1
0 = No save
1 = Save

SVR2--LT Save to R2
0 = No save
1 = Save

SVR3 Save to R3
0 = No save
1 = Save

SAVE--LT Save
0 = Save
1 = No save

ENTXLNLT Enable text lines
0 = TAT, RAT, BAT
1 = Other text

ENTXSKLT Enable text softkey
0 = SKT
1 = Other text

Z-AC Z-active
0 = No light
1 = Light

6 WRHOVRLT Write data to the OUTPUT PORT DISPLAY PARAMETERS D2108 on unit A3 and to the X VARIABLE LATCH D2332 on unit A2.

This is done together with the following signals:

EPY-Ø1	EPY-ØØ	Y-EXPAND
0	0	* 1/4 - Trace
0	1	* 1 - Trace + MSC text
1	0	* 4 - Text (Other)
1	1	* 4 - Trace

EPX-Ø2	EPX-Ø1	EPX-ØØ	X-EXPAND
0	0	0	*1
0	0	1	*2
0	1	0	*4
0	1	1	*8
1	0	0	--
1	0	1	*16
1	1	0	*32
1	1	1	*64

TXLNSKLT Text line + softkey
0 = TAT, RAT, BAT, SKT
1 = Trace + MSC

DIOS--HT Disable overscan
0 = Overscan
1 = No overscan

7 Initialization of Z-counter Ø

8 Initialization of Z-counter 1

9 Initialization of Z-counter 2

10 Preset of LSB countvalue of Z-counter Ø

11 Preset of MSB countvalue of Z-counter Ø

12 Preset of LSB countvalue of Z-counter 2

13 Preset of MSB countvalue of Z-counter 2

14 Preset of LSB countvalue of Z-counter 3

15 Preset of MSB countvalue of Z-counter 3

16 Clear instruction (read)

17 WRDPSTLT Start display of the next display block after the setting of the parameters

8.3.2.4 Display timing

The display timing is arranged in such a way that one dot is displayed per 750 ns. Each period of 750 ns is divided into three fases of 250 ns each like shown in the following figure.

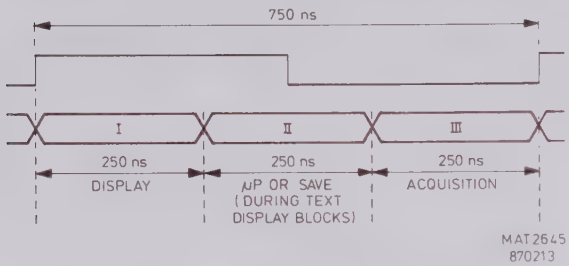


Figure 8.3.3 Display timing.

Fase I is for display actions, fase II for UP or SAVE actions and during fase III acquisition actions can be performed.

8.3.2.5 SAVE timing

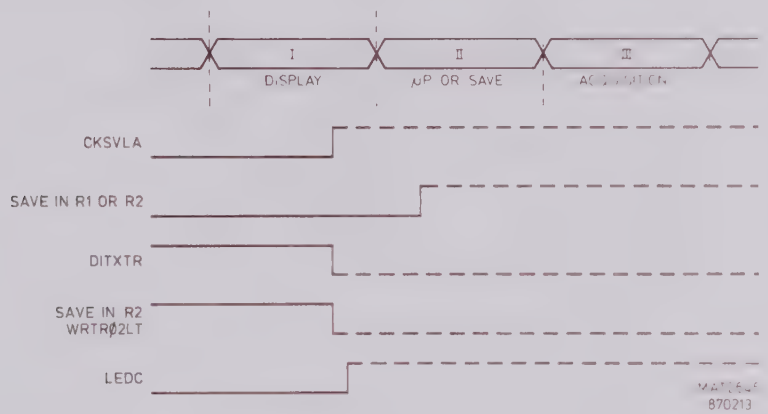


Figure 8.3.4 Save timing.

A save action from RØ to R1, R2 or R3 is done during the display of text blocks. It is done with the first 4096 addresses of the total of 8192 addresses which are generated by the display address counter. Each address is applied to register RØ, to the selected register and to the text memory.

The output data of RØ is latched in the SAVE latch during FASE I with signal CLKVLA.
If R2 is selected for a save action, this register is enabled directly to store the data value.
When this is done, the output of RØ is disabled and the output of the text memory is placed on the trace data bus via the TEXT/TRACE buffer via signal DITXTR. The text can be displayed then.

If R1 or R3 is selected, the output of the SAVE latch is placed on the trace data bus during FASE III, address line TRAB13 is switched to "1" to point to R1 or R3 and the relevant chip select signal is activated.

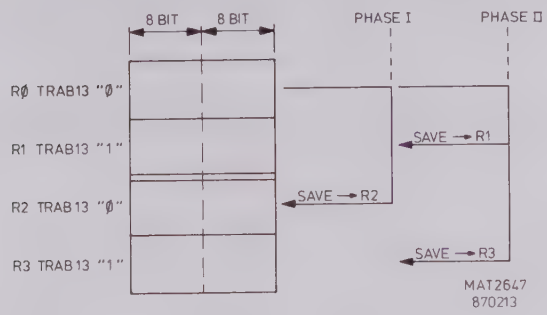


Figure 8.3.5 Save actions.

8.3.3 Circuit descriptions

8.3.2.1 Data buffer

Data from the microprocessor system on the data lines DBØØ...15, which is meant for the DISPLAY CONTROL unit A3, is applied to the internal display data bus lines DPDBØØ...15 of this unit. This data is transferred via the DATA BUFFER, which consists of D2101 and D2102 when the I/O select signal IOSLØ5LT is activated.

8.3.3.2 Preset register

Preset data from the microprocessor system can be latched in the PRESET REGISTER D2103 and D2104 (partly) when the write pulse WRPSDPLT is generated at the beginning of each new display block.
The data on the data lines PSDPØØ... PSDP11 is used to preset the DISPLAY ADDRESS COUNTER with a start value for the next display action. This value depends on the channel which is selected for display, the selected horizontal expand factor or the value which has to be plotted.

8.3.3.3 Output ports display parameters

A number of display parameters can be latched in the OUTPUT PORTS DISPLAY PARAMETERS D2104 (partly), D2106, D2107 and D2108 as described under section 8.3.2.

8.3.3.4 Display address counter

The DISPLAY ADDRESS COUNTER, consisting of the counters D2111, D2112 and D2113, generates the addresses of the TRACE MEMORY locations to be displayed.

The counter is normally (in single channel mode) presetted to its zero state before a display block starts and the counter counts through ist complete range during a display block.

In dual channel mode however, the counter needs to know whether channel A or channel B has to be displayed. The correct start address of the channel in the TRACE MEMORY has to be presetted by the microprocessor system. The counter counts then with a speed which is twice the speed in single channel mode.

The counter is always presetted by the value which is present in the PRESET REGISTER at the beginning of a display block. Presetting is done under the control of signal DIDPPS. Presetting is stopped at the start of a display block with signal STDP via flip flop D2114. Counting is started then under the control of signal DIDPCN.

The first output bit DPABØØ of the display counter is via multiplexer D2118 applied to the display address bus and influenced depending on the selection of single or dual channel mode.

Single channel mode: (HOMO = "0" and DPMO--LT = "1")

DPABØØ = DPABØØ

Dual channel mode: (HOMO = "0" and DPMO--LT = "0")

DPABØØ = CHID (Channel identification)

CHID = "0" means channel B (odd locations in memory)

CHID = "1" means channel A (even locations in memory)

In dual channel mode, the display counter clockpulse DPCNCK is switched to a speed which is twice the speed used in single channel mode.

The speed is:

1 1/3 MHz in single channel mode (derived from CK/6-ØHT)
2 2/3 MHz in dual channel mode (derived from CK/3)

8.3.3.5 Data buffers

There are buffers D2121 and D2122 (partly) for display addresses, D2122 (partly) and D2123 for softkey text and D2124 for line text.

8.3.3.6 Address decoder

An address decoder D2132 is able to decode a number of addresses which are generated by the microprocessor.
This results in a number of signals (see also the preset sequence under section 8.3.2) according to the following table.

IOSLØ5LT	UPWR--LT	ABØ4	ABØ3	ABØ2	ABØ1	Output signal
0	0	1	0	0	0	WRDPSTLT
0	0	1	0	0	1	--
0	0	1	0	1	0	--
0	0	1	0	1	1	WRVEPOLT
0	0	1	1	0	0	WRHOPOLT
0	0	1	1	0	1	WRPSDPLT
0	0	1	1	1	0	WRDPPALT
0	0	1	1	1	1	WRHOVRLT

A chip select signal CSZ-CNLT for the Z-counter is generated via D2129 if IOSLØ5LT is active and ABØ4 is logic "0".

The signal overflow status can be read by the microprocessor via data bit DBØØ (D2128-6), which is derived from signal DCDB10 via flip flop D2114. The overflow status (one or more bits in a display block) is read by the microprocessor after each display cycle.

8.3.3.7 Clock fase generator

A binary counter D2134 which can be resetted via the microprocessor reset signal UPRSOTLT counts the pulses from the 8 MHz microprocessor clocksignal DPCKØ8HT.
During each counter cycle, the counter is presetted to the value eleven when its fourth output bit is zero and a new clockpulse appears. The counter then continuous counting which results in the timing clock signals as shown in figure 8.3.6.

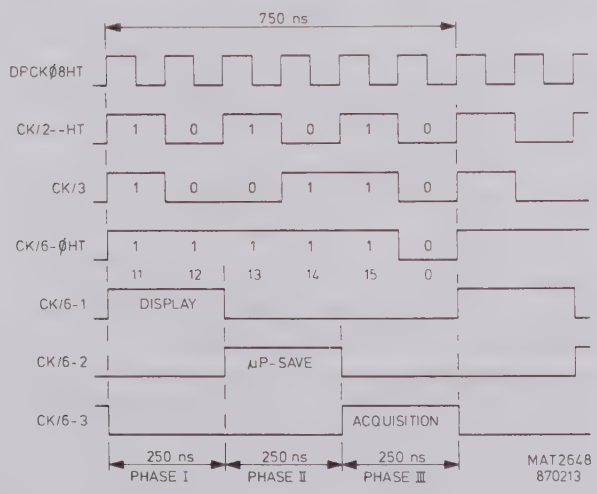


Figure 8.3.6 Clock signals.

8.3.3.8 Copy synchronization one-shot

The COPY SYNCHRONIZATION ONE-SHOT D2144 has no function in this instrument.

8.3.3.9 Memory select

The MEMORY SELECT circuit which mainly consists of the FPLA circuit D2151 generates a number of memory select, output enable and write enable signals.

8.3.3.10 Z-detection

The Z-DETECTION circuit which mainly consists of FPLS circuit D2142 generates one output signal Z-BL--HT which carries the blanking/unblanking information for the C.R.T. This signal is derived from a number of input conditions from a number of display circuits.

8.3.3.11 Z-timer

The Z-TIMER is for each block presetted with a value which is calculated by the microprocessor. The value depends on the total number of dots to be displayed during the actual display block. The counter starts counting down latch enable pulses LEDA--HT when enable display count signal ENDPCN is active. Until the end of the counting, when the zero state of the counter is reached, an output signal Z-DP is applied to the Z-DETECTION circuit. The C.R.T. trace can only be unblanked as long as the Z-TIMER is counting and signal Z-DP is generated.

8.3.3.12 Restart timer

This timer especially has a function when X-EXPAND is selected and is for each block presetted with a value which is calculated by the microprocessor. The value depends on the X-EXPAND factor and the total number of dots to be displayed during the actual display block.

If for example the X-EXPAND factor is *4, the display block will be displayed four times in order to reach a same trace intensity on the C.R.T. screen as there is without X-expansion.

After the first display action, when the zero state of the restart timer is reached, and restart display signal RDDP--LT is generated to start the second display action and so on. After display action four (in this example) the end of the complete display block is given by the ILØ5--LT output signal from the interrupt timer.

8.3.3.13 Interrupt timer + flip flop

This timer is for each display block presetted with a value which is calculated by the microprocessor. The value depends on the total number of dots to be displayed during the actual display block. The counter starts counting down latch enable pulses LEDA--HT when enable display count signal ENDPCN is active. At the end of the counting, when the zero state of the counter is reached, an output signal is applied to the interrupt flip flop D2133 and an interrupt signal ILØ5--LT for the microprocessor is generated to indicate the end of the actual display cycle.

8.3.3.14 Start + smooth delay flip flop

The START flip flop is blocked by signal IL05DPLT on input 11 as long as a display preset sequence is performed. At the end of such a sequence a display start signal WRDPSTLT is generated and the start flip flop D2127 produces a 3 us start signal STDP. This STDP signal is applied to the synchronization flip flop D2114 to start the display of a new block.

A new display action can also be started via a RTDP--LT output pulse from the restart-timer.

If SMOOTH is selected, an additional delay of 12 us is introduced by smooth delay flip flop D2127 and a smooth delay signal SMDL--LT is then applied to sychronization flip flop D2116. This is done at the end of a sweep to avoid connection of the last dot of a sweep with the first one of the next sweep.

NOTE: In this instrument the smooth circuit is not activated.

8.3.3.15 Plot one-shot

If a plot function is selected (signal PLOT active) the plot one-shot D2144 will generate a sample plot pulse SAPL for the analog plot interface on unit A1 at the beginning of the plot block. This is the last block of a display cycle.

In this way one dot per display cycle can be plotted. The minimum plot time is therefore 20 ms/dot. Slower plot speeds can be selected via the PLOT menu.

The microprocessor knows how many dots have to be plotted and which actual dot has to be plotted. The memory addres of the actual dot to be plotted, is presetted in the display address counter and the data which is stored in this addres location is applied to the plot interface on unit A1.

The penlift (pen up/pen down) can be controlled via the microprocessor generated signal PU----LT.

The polarity of the penlift is also generated by the microprocessor by generating signal PFPY.

If the Z-signal is blanked (during overscan for example) the pen is also lifted automatically.

If no plot function is selected, the plot outputs are short circuited via signal PLZEOT.

8.3.4 Signal-name list

UNIT A3

Signal-name	Description	Signal source	Signal destination(s)
ABØ1...15	Address bus Ø1...15	A6+Option	-
ANCPY-HT	Analog compress Y	A3	A12-A1
ANEPY-HT	Analog expand Y	A3	A12-A1
BUAB13...15	Buffered address lines 13...15	A3	A3
BUHISBLT	Buffered high strobe	A3	A3
BULOSBLT	Buffered low strobe	A3	A3
CHID	Channel indentification	A3	A3
CKEPVE	Clock expand vertical	A3	A12-A2
CKSVLA	Clock save latch	A3	A12-A4
CK/2--LT	Clock /2	A3	A3
CK/2--HT	Clock /2	A3	A3
CK/3	Clock /3	A3	A3
CK/6-ØLT	Clock /6-Ø	A3	A3
CK/6-ØHT	Clock /6-Ø	A3	A3
CK/6-1LT	Clock /6-1	A3	A3
CK/6-1HT	Clock /6-1	A3	A3
CK/6-2LT	Clock /6-2	A3	A3
CK/6-2HT	Clock /6-2	A3	A3
CLDPAB	Clock display address bus (CK/6-1HT)	A3	A12-A4
CLUPAB	Clock microprocessor bus (MMYSLØ2HT)	A3	A12-A4
CSTX--LT	Chip select text	A3	A12-A4
CSZ-CNLT	Chip select Z-counter	A3	A3
DAAK--LT	Data acknowledge	A3	A12-A4
DAAK--HT	Data acknowledge	A3	A12-A4
DAHISBLT	Data high strobe	A6+Option	-
DALOSBLT	Data low strobe	A6+Option	-
DATRAKLT	Data trace acknowledge	A3+A5+A6+A8 +Option	A12-A6, A12-Option
DBØØ...15	Data bus ØØ...15	A6+Option	-
DCDBØ9...15	Display control data bus Ø9...15	A4	-
DIDBTX	Disable data bus text-buffer	A3	A12-A4
DIDJ	Disable dot join	A3	A3
DIDPCN	Disable display counter	A3	A3
DIDPPS	Disable display preset	A3	A3
DIOS--HT	Disable overscan	A3	A12-A1, A12-A2
DISVLA	Disable save latch	A3	A4
DITXTR	Disable text trace buffer	A3	A12-A4
DJAC--HT	Dot join active	A3	A12-A2
DPABØØ...11	Display address bus ØØ...11	A3	A12-A4
DPCKØ8LT	Display clock 8 Mhz	A3	A3
DPCKØ8HT	Display clock 8 Mhz	A3	A3
DPCNCK	Display counter clock	A3	A3
DPDBØØ...15	Display data bus ØØ...15	A3	A3
DPMO--LT	Display mode	A3	A3

Signal-name	Description	Signal source	Signal destination(s)
DPMYRDHT	Display memory read	A3	A3
DPMYWRHT	Display memory write	A3	A3
DPMYØØ...Ø2	Display memory ØØ...Ø2	A3	A3
DPMYØ2LT	Display memory Ø2	A3	A3
DPRJUPLT	Display reject up	A3	A12-A2
DPRJDWLT	Display reject down	A3	A12-A2
DRTXTR	Direction text trace buffer	A3	A12-A4
DPTR--HT	Display trace (DPMYØ2LT)	A3	A12-A1
ENDPCN	Enable display counter	A3	A3
ENTRHOLT	Enable trace horizontal	A3	A12-A2
ENTRHOHT	Enable trace horizontal	A3	A3
ENTXLNLT	Enable text line	A3	A12-A2
ENTXSKLT	Enable text softkey	A3	A3
EPDBØØ...11	Expanded data bus	A2,A3	A12-A2
EPHO14	Expanded horizontal bus 14	A3	A12-A2
EPX-ØØ...Ø2	Expand X ØØ...Ø2	A3	A12-A2
EPY-ØØ...Ø1	Expand Y ØØ...Ø1	A3	A12-A2
EP12--LT	Expand 12	A3	A12-A2
HOMO	Horizontal mode	A3	A3
ILØ5--LT	Interrupt level Ø5	A3	A12-A6
ILØ5DPLT	Interrupt level Ø5 display	A3	A3
IOSLØ5LT	I/O select Ø5	A6	-
IVDCDB	Invert display control address bus	A3	A12-A2
LEDA--LT	Latch enable DAC	A3	A12-A2
LEDA--HT	Latch enable DAC	A3	A12-A2
LEDC	Latch enable display control	A3	A12-A4
MXCPAD (WRAQ--HT)	Multiplex copy address	A3	A12-A4
MYSLØ2LT	Memory select Ø2	A6+Option	-
MYSLØ2HT	Memory select Ø2 (CLUPAB)	A3	-
OETRØ1LT	Output enable trace Ø1	A3	A12-A4
OETRØ2LT	Output enable trace Ø2	A3	A12-A4
OETX--LT	Output enable text	A3	A12-A4
PFPY	Penlift polarity	A3	A12-A1
PLOT	Plot	A3	A3
PLZEOT	Plot zero output	A3	A12-A1
PSDPØØ...11	Present display bus ØØ...11	A3	A3
PU----LT	Pen-up signaal	A3	A12-A1
RDDM--LT	Read display memory	A3	A12-A4
RDDPDALT	Read display data	A3	A3
RSDAAKLT	Reset data acknowledge	A3	A3
RTDP--LT	Restart display	A3	A3
SAPL	Sample plot	A3	A12-A1
SAPL--LT	Sample plot	A3	A3
SARY	Sample ready	A4	-
SARYAKLT	Sample ready acknowledge (DITRDB) (WRAQ--RT)	A3	A12-A4

Signal-name	Description	Signal source	Signal destination(s)
SAVE--LT	Save	A3	A3
SLTR1LLT	Select trace 1L	A3	A12-A4
SLTR1HLT	Select trace 1H	A3	A12-A4
SLTR2LLT	Select trace 2L	A3	A12-A4
SLTR2HLT	Select trace 2H	A3	A12-A4
SM----LT	Smooth	A3	A12-A2
SMDL--LT	Smooth delay	A3	A3
STDP	Start display	A3	A3
SVR1	Save register R1	A3	A3
SVR2--LT	Save register R2	A3	A3
SVR3	Save register R3	A3	A3
SYDP	Synchronize display	A3	A12-A8
TRAB13	Trace address bus 13	A3	A12-A4
TXAB13	Text address bus 13	A3	A12-A4
TXLNSKLT	Text line softkey	A3	A3
UPCKØ8	Microprocessor clock 8 Mhz	A6	-
UPRD--LT	Microprocessor read	A6	-
UPRD--HT	Microprocessor read	A3	A3
UPRSOTLT	Microprocessor reset out	A6	-
UPWR--LT	Microprocessor write	A6	-
VEDBØ9...12	Vertical data bus Ø9...12	A2	-
WETRØ1LT	Write enable trace Ø1	A3	A4
WETRØ2LT	Write enable trace Ø2	A3	A12-A4
WETX--LT	Write enable text (WRØ2--LT)	A3	A12-A4
WRAQ--LT	Write acquisition	A3	A3
WRAQ--HT	Write acquisition (SARYAKLT)	A3	A3
WRDPPALT	Write display parameters	A3	A3
WRDPSTLT	Write display start	A3	A3
WRHOPOLT	Write horizontal position	A3	A12-A2
WRHOVRLT	Write horizontal variable	A3	A12-A2
WRPSDPLT	Write preset display	A3	A3
WRVEPOLT	Write vertical position	A3	A12-A2
WRØØ--LT	Write ØØ	A3	A3
WRØ1--LT	Write Ø1	A3	A3
WRØ2--LT	Write Ø2 (WETX--LT)	A3	A12-A4
Z-AC--LT	Z - active	A3	A3
Z-BL--HT	Z - blanking signal	A3	A12-A1
Z-DP	Z - display	A3	A3
Z-OTØ3	Z - output Ø3	A2	-

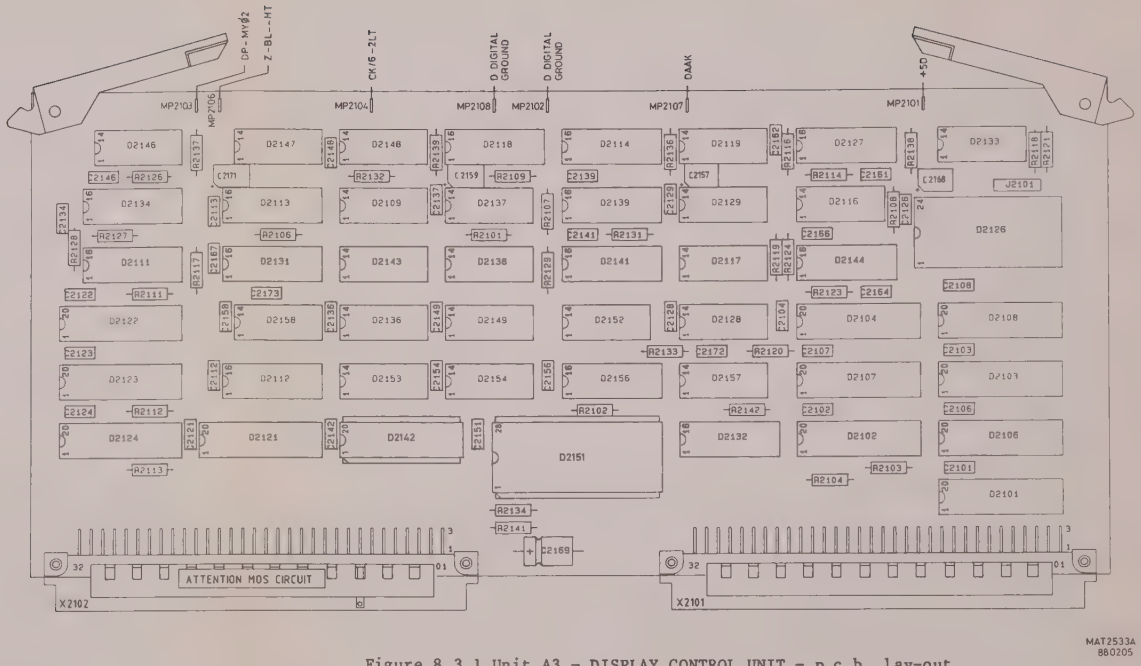


Figure 8.3.1 Unit A3 - DISPLAY CONTROL UNIT - p.c.b. lay-out.

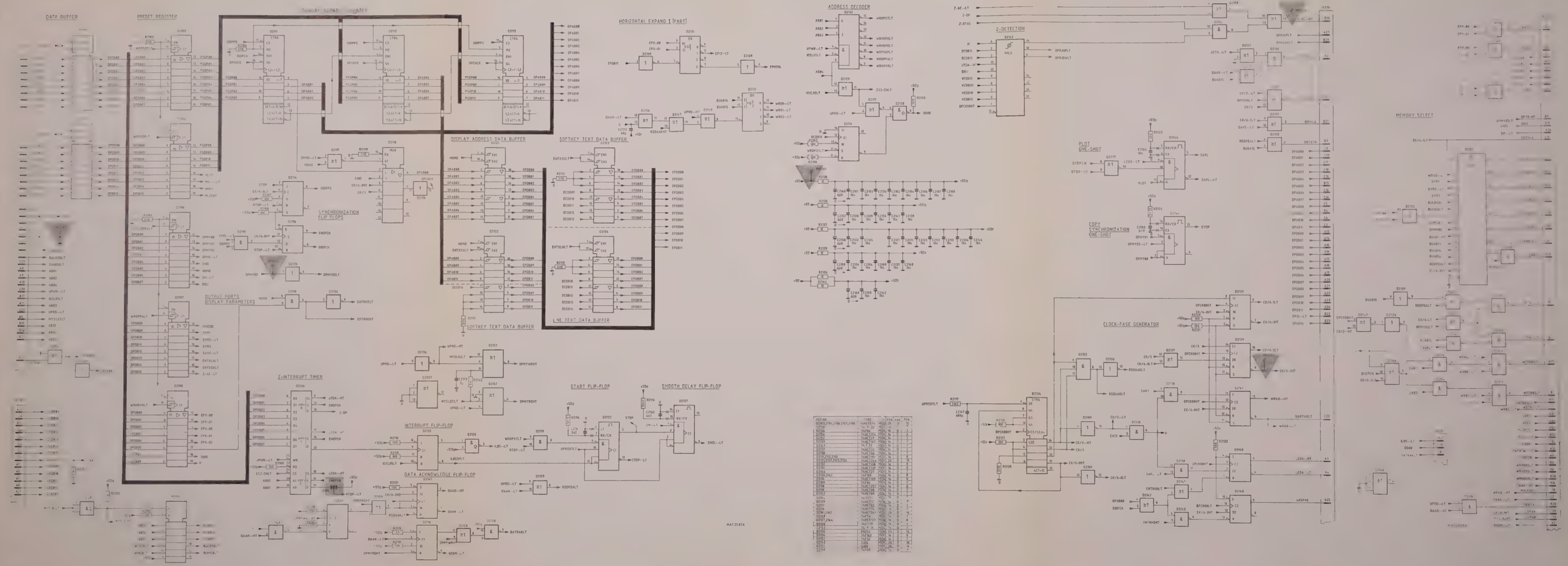
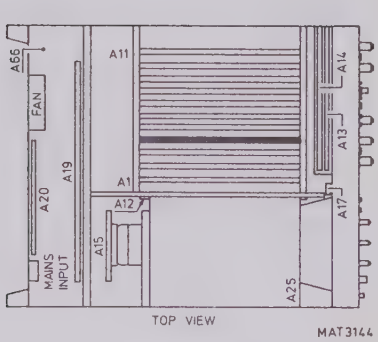


Figure 8.3.2 Unit A3 - DISPLAY CONTROL UNIT - circuit diagram.

UNIT A4 - DISPLAY MEMORY UNIT



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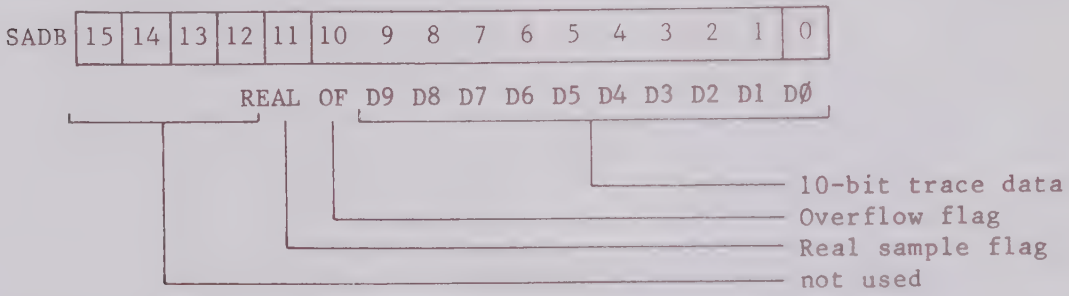
8.4.1 General information

This unit basically comprises the four random-access registers RØ, R1, R2 and R3 of the trace memory, the text memory, the copy address counter and their associated control circuits.

8.4.2 Copying trace data from the DPU into display register RØ

On receipt of a trigger pulse, a coupling is realized between the DPU (digital processing unit) and register RØ of the trace memory unit. The DPU places its 12-bit (two - complement) trace data on the sample data bus lines SADBØØ...SADB12. This bus is connected to the trace data latch consisting of D2001 and 2002. Each trace data word is clocked in the latch with signal latch enable display (LEDP). This is done in the rhythm of the acquisition system.

Trace data format:



Signal LEDP switches also a handshake flipflop D2017, resulting in an active SARY (sample ready) signal. When the trace data word is copied to register RØ, the SARYAKLT signal resets the handshake flip flop, which informs the DPU that the next trace data word can be sent to the trace data latch.
In this way the display unit is informed that new trace data is available on the output bus lines TRDBØØ ... TRDB15 of the trace data latch. This trace data bus is connected to the four display registers. New trace data however is always stored in register RØ. This is done in a rhythm which is determined by the acquisition system.
RAM's D2008 and D2009 form together the two 4kx16 registers RØ and R1 and D2011 and D2012 form together the two 4kx16 registers R2 and R3.

Addresses for register RØ needed during the copy cycle of trace data from the DPU into register RØ, are generated by a copy address counter which consists of D2018, D2019 and D2021.
The copy counter address bits CPABØØ ... CPAB11 are applied to the trace register RØ via address multiplexer II consisting of D2037, D2038 and D2039 as TRABØ1 ... TRAB12.
Address line TRAB13 us separately generated and is used for the switching between RØ and R1 or between R2 and R3.

The counter is first resetted to its zero state by signal RSDU--LT (reset DPU). After an active trigger the copy cycle is started and the register will be completely filled once with trace data from the acquisition system. The counter is counting (and thus producing addresses for register RØ. CNCPCN pulses (count pulses for the copy address counter) which are generated in the rhythm in which the acquisition system offers the new trace data. At the end of the copy cycle, the counter generates a signal TCCPCN (terminal count copy adress counter) and the cycle is stopped.

Register RØ is furthermore controlled by its chip select signals CSTR1LLT and CSTR1HLT which can only be active when the memory select down signal MYSLDWLT is not active and by the write enable signal WETRØ1LT.

8.4.3 Saving trace data from register RØ into one of the registers R1, R2 or R3.

The address information needed for register RØ and the selected register is generated by the display address counter. The address lines DPABØØ ... DPAB11 are applied to the registers RØ, R1, R2 and R3 via address multiplexer I consisting of D2031, D2033, D2032 and D2041 when cycle counter display address bus signal CLDPAB is active and via address multiplexer II consisting of D2037, D2038 and D2039 as TRABØ ... TRAB12 when multiplexed copy address signal MXCPAD is active.

Each trace data word on the register RØ trace data output lines TRDBØØ...TRDB15 is first saved in a save latch consisting of D2028 and D2029 with the clock save latch signal CKSVLA.
The saved word is then afterwards saved in the selected memory by using exactly the same display address. Address line TRAB13 is switched to point to the selected register which is activated via its chip select signal and write enable signal.
The output of the save latch is disabled by the disable save latch signal DISVLA. For the next word the microprocessor increases the address number and so on. After 4096 of these actions the save action is completed. The save latch is not used when data has to be saved in register R2 or R3. Save is then done directly from RØ to R2 and to R3.

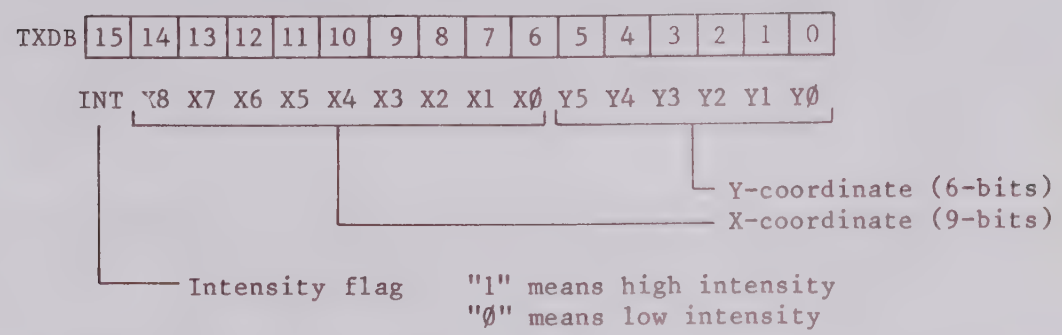
8.4.4 Storage of text in the text memory

All used kinds of texts are generated by the microprocessor system and stored when they are needed in a 8kx16 bit text memory consisting of D2014 and D2016.
The addresses needed for the storage of text in the text memory are generated by the microprocessor. The microprocessor address lines ABØ1 ... AB12 are applied to the text memory via address multiplexer I consisting of D2031, D2032, D2033 and D2041 as TXABØ1 ... TXAB12.

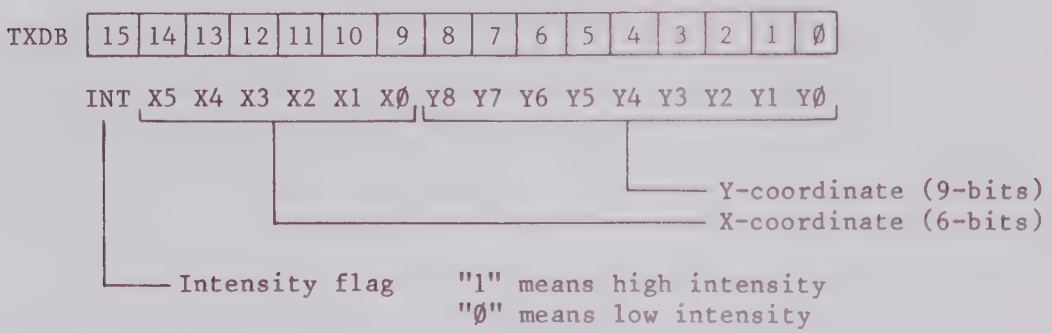
The text data consists of vertical and horizontal coordinates and an intensity flag. This data is generated by the microprocessor system. The data bits DBØØ ... DB15 are applied via a bidirectional latch consisting of D2003 and D2004 as TXDBØØ ... TXDB15 to the text memory.

The following text data formats exist:

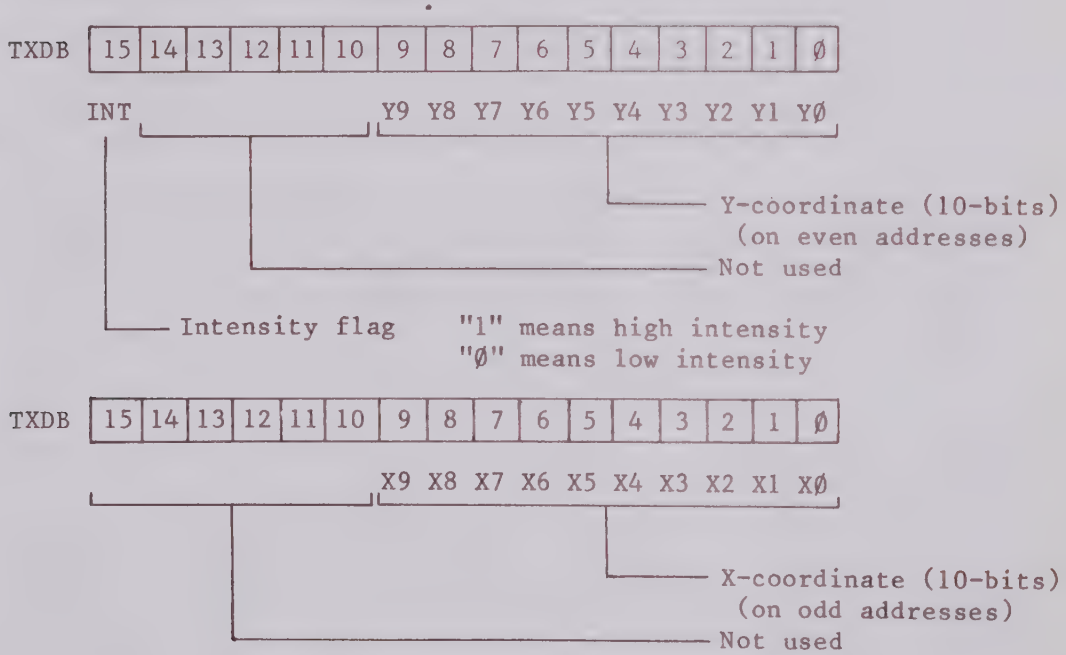
Top area text (TAT)
Trace area text (TRAT)
Bottom area text (BAT)



Softkey text (SKT)



Miscellaneous text (MSC)



For storage of miscellaneous texts, two words are stored, one for the Y-coordinate and the intensity flag and the other one for the X-coordinate.
If no text has to be displayed, a word of only one's will be stored in the text memory and the trace will be suppressed.

8.4.5 Reading trace data for display purposes

The display memory addresses which are needed during the display cycle for trace data are generated by a display address counter which is located on the display control unit A3.

The display counter output address bits DPABØØ ... DPAB11 are applied via address multiplexer I and address multiplexer II to the address inputs of the four display registers RØ, R1, R2 and R3.

Each register can be selected for display by the generation of its chip select signal, its output enable signal and the register select signal TRAB13.
The selected register places its output data word on the trace data bus lines TRDBØØ ... TRDB15. This data is applied to the display control latch by latch enable display control latch signal LEDC.
The output data bits DCDBØØ ... DCDB15 are applied then to the display DAC unit A2 for further handling.

8.4.6 Reading text data for display purposes

The text memory addresses which are needed during the display cycle for text data are generated by the display address counter. These display address counter address bits DPABØØ ... DPAB11 are applied via address multiplexer I to the address inputs of the text memory.
The text memory is selected by the generation of its chip select signal, its output enable signal and the register select signal TXAB13. The text output data word is placed on the text data bus lines TXDBØØ ... TXDB15 and via the text/trace buffer consisting of D2006 and D2007 applied to the display control latch.
The output data bits DCDBØØ ... DCDB15 are applied then to the display DAC unit A2 for further handling.

8.4.7 Data communication via options

Instruments which are equipped with option can communicate with the trace memory as well as the text memory via the following signal paths.

Trace memory:

Addresses are generated by the microprocessor and via address multiplexers I and II applied to the display memory.
Data communication is done via the microprocessor data bus, the bidirectional text/trace buffer and the trace data bus or vice versa.

Text memory:

Addresses are generated by the microprocessor and via address multiplexer I applied to the text memory.
Data communication is done via the microprocessor bus, the bidirectional data/text latch and the text data bus or vice versa.

8.4.8 Trigger address comparator

The TRIGGER ADDRESS COMPARATOR is part of the address generator on the DPU CONTROL (Unit A8).
It has no function in this instrument.

8.4.9 Signal name list

UNIT A4

Signal name	Description	Signal source	Signal destination(s)
ABØ1...12	Address bus Ø1...12	A6+option	-
CKSVLA	Clock save latch	A3	-
CLDPAB	Clock display adress bus	A3	-
CLUPAB	Clock microprocessor bus	A3	-
CNCPCN	Count copy address counter	A8	-
CPABØØ...11	Copy counter address bus ØØ...11	A4	A4
CSTR1LLT	Chip select trace 1L	A4	A4
CSTR1HLT	Chip select trace 1H	A4	A4
CSTR2LLT	Chip select trace 2L	A4	A4
CSTR2HLT	Chip select trace 2H	A4	A4
CSTX--LT	Chip select text	A3	-
DAAK--LT	Data acknowledge	A3	-
DAAK--HT	Data acknowledge	A3	-
DAVA	Data valid	A5	-
DBØØ...15	Data bus ØØ...15	A6+option	-
DCDBØØ...15	Display control data bus ØØ...15	A4	A12-A2,A12-A3
DIDBTX	Disable data bus text-buffer	A3	-
DIDCLA	Disable display control latch	A4	-
DISVLA	Disable save latch	A3	-
DITRDB	Disable trace data bus (SARYAKLT)	A3	-
DITXTR	Disable text trace buffer	A3	-
DPABØØ...11	Display address bus ØØ...11	A3	-
DRTXTR	Direction text trace buffer	A3	-
DUABØØ...11	DPU address bus ØØ...11	A8	-
ENCPSA	Enable copy sample	A4	A12-A8
LEDC	Latch enable display control	A3	-
LEDP	Latch enable display	A8	-
MXCPAD	Multiplex copy address	A3	-
MYSLDWLT	Memory select down	A6	-
MYSLØ2LT	Memory select Ø2	A6+Option	-

Signal-name	Description	Signal source	Signal destination(s)
OETRØ1LT	Output enable trace Ø1	A3	-
OETRØ2LT	Output enable trace Ø2	A3	-
OETX--LT	Output enable text	A3	-
OFDP	Overflow display	A9	-
OTCM	Output comparator	A4	A12-A8
RDDM--LT	Read display memory	A3	-
RLDP	Real sample display	A9	-
RSDU--LT	Reset DPU	A8	-
SADBØØ...Ø9	Sample data bus ØØ...Ø9	A9+A11	-
SARY	Sample ready	A4	A3
SARYAKLT	Sample ready acknowledge (DITRDB)	A3	-
SLTR1LLT	Select trace 1L	A3	-
SLTR1HLT	Select trace 1H	A3	-
SLTR2LLT	Select trace 2L	A3	-
SLTR2HLT	Select trace 2H	A3	-
TCCPCN	Terminal count copy address counter	A4	A12-A8
TRABØ1...12	Trace address bus Ø1...12	A4	A4
TRAB13	Trace address bus 13	A3	-
TRDBØØ...15	Trace data bus ØØ...15	A4	A4
TXABØ1...12	Text address bus ØØ...12	A4	A4
TXAB13	Text address bus 13	A3	-
TXDBØØ...15	Text data bus ØØ...15	A4	A4
UPCKØ8	Microprocessor clock 8 MHz	A6	-
WETRØ1LT	Write enable trace Ø1	A3	-
WETRØ2LT	Write enable trace Ø2	A3	-
WETX--LT	Write enable text	A3	-

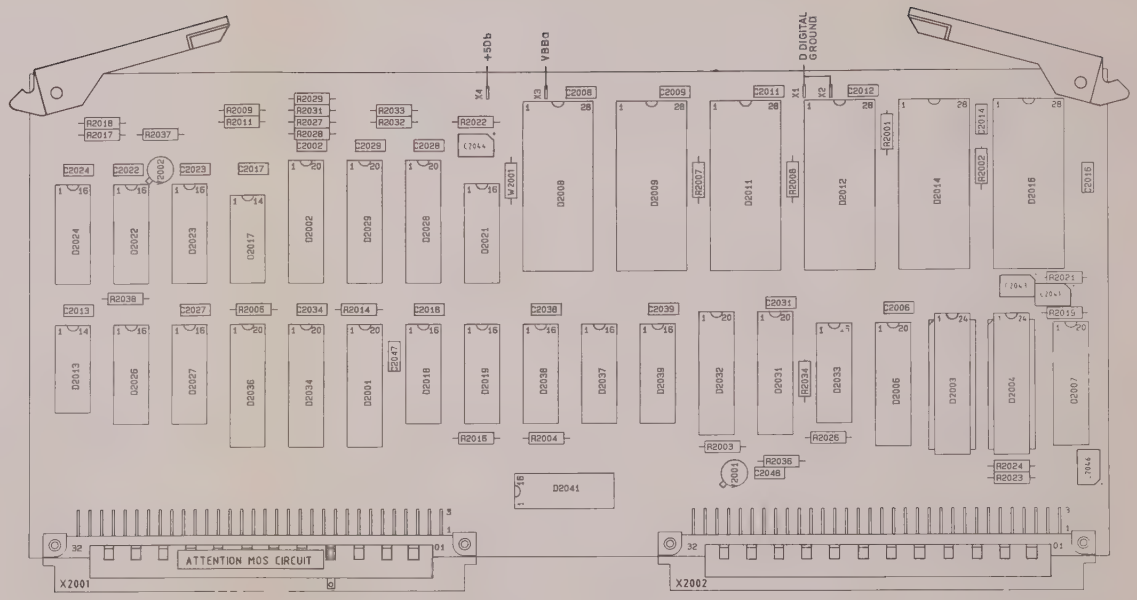


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Figure 8.4.1 Unit A4 - DISPLAY MEMORY UNIT - p.c.b. lay-out.

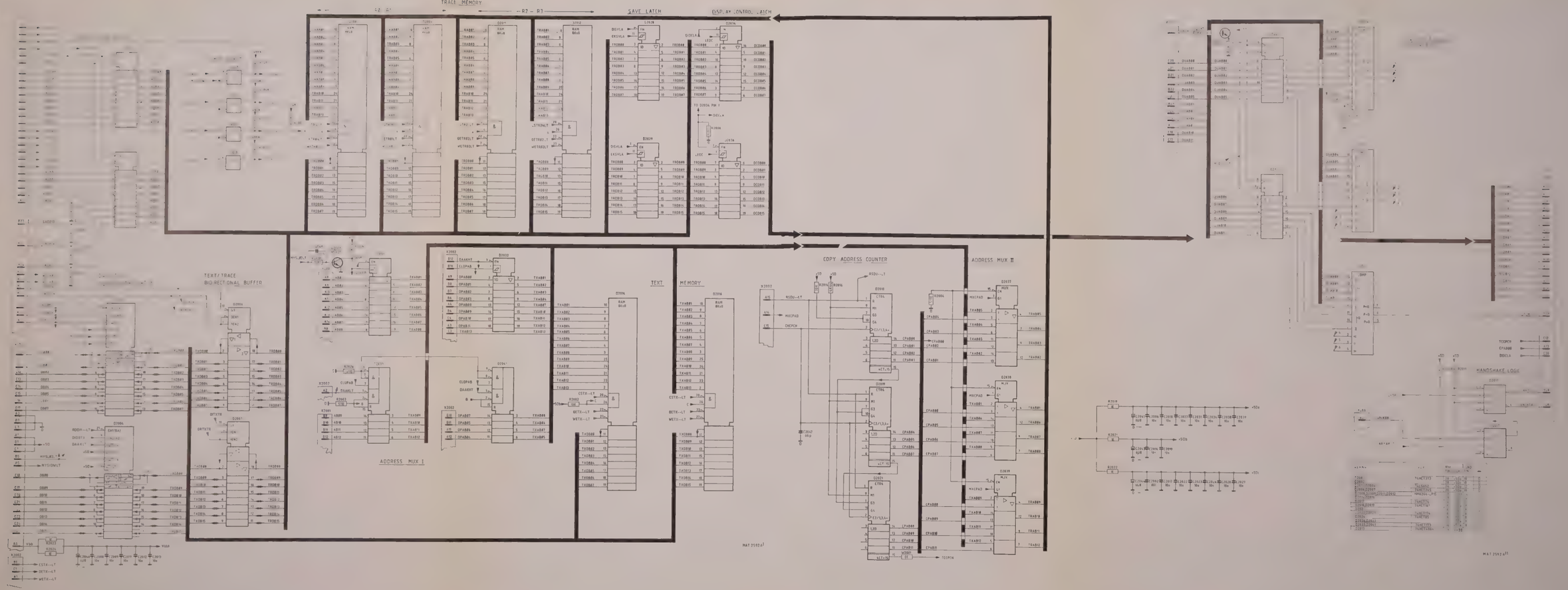
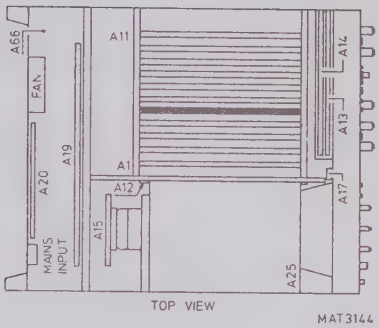


Figure 8.4.2 Unit A4 - DISPLAY MEMORY UNIT - circuit diagram.

UNIT A5 - GRAM UNIT



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8.5.2 Memory circuit..... 8.5-1
8.5.3 ACL circuit..... 8.5-2
8.5.4 Signal name list..... 8.5-4

8.5.1 General information

This unit basically consists of the microprocessor memory circuit (RAM) and the acquisition control logic (ACL).

8.5.2 Memory circuit

The microprocessor memory circuit consists of a RAM and some control logic.

The RAM consists of RAMØ (D1834 and D1836), which is backed up by the battery, and RAM1 (D1837 and D1838). All devices are 32 KByte types. If 8 KByte types are used for D1834 and D1836, then soldering joint J1801 should be changed over.

The ADDRESS REGISTER latches the data of the microprocessor address lines. It is clocked by CKAB--HT, which is active when addresses on the address bus are stable.

The BIDIRECTIONAL DATA buffer buffers the data lines to the microprocessor. It is enabled by CKAB--LT. The direction of data transfer is determined by RARD--LT.

The SELECT LOGIC generates the RAM select signals.
When the power goes down, MYSLDWLT goes low. Now D1833 separates SLØØLOLT and SLØØHILT from the select logic and so they go to VBBa level. The RAMs (only RAMØ) are deselected, their contents remain.

The remaining select logic generates delayed CKAB signals and DATRAKLT, when this unit is selected.
The delay of the CKAB signals (R1802 and C1892) ensures stable data on the address bus and the data bus when they are clocked in.
The delay of DATRAKLT (R1839 and C1893) ensures enough data setup time for the RAM.

8.5.3 ACL circuit

The ACL circuit consists of the following parts:

- ACL latch
- ACL reset logic
- Acquisition Control Logic (ACL)

The ACL latch is a shift register (D1814), which latches a number of ACL status signals, which come from the microprocessor via the MANAGEMENT unit A25.

The ACL RESET LOGIC generates reset signals for the ACL (RSACL and RSACL-LT) and the reset signal for the stair counter (RSSTCNLT) on the Time-base unit A51. The ACL is reset by the CLACL signal from the ACL LATCH, when a new setting of the instrument is made, or by the TRRY signal from the DPU Control unit A8. TRRY marks that the DPU is ready to accept a new sweep of samples.
The stair counter is reset by RSSTCNLT, when ILØ2--LT from the DPU CONTROL goes low (D1820). ILØ2--LT marks that the DPU has accepted a sweep of samples.

The ACQUISITION CONTROL LOGIC generates the required signals for the control of the capture of samples.
These signals are:

Name	Description	Destination
HDSA-1	Hold sample	Vertical signal unit A55
CNSTCNLT	Count stair counter	Time-base unit A51
STCV	Start conversion	ADC + T&H unit A11
CHPT	Channel pointer	DPU control unit A8
CHSW	Channel switch	Vertical signal unit A55
DAVA	Data valid	DPU control unit A8
TKSA	Take sample	DPU control unit A8
EODA	End of data	GRAM unit A5

The HDSA-1 signal generates THMOA and THMOB via the TRACK & HOLD CONTROL on the Vertical Signal Unit A55.
The time T1 consists of a short time made on this unit (determined by R1841 and C1861) and the HOLD DELAY times on unit A55.

In the timing diagram it is assumed that:

- Channels A and B are selected
- Multiple sampling is off
- The screen resolution is 512 dots

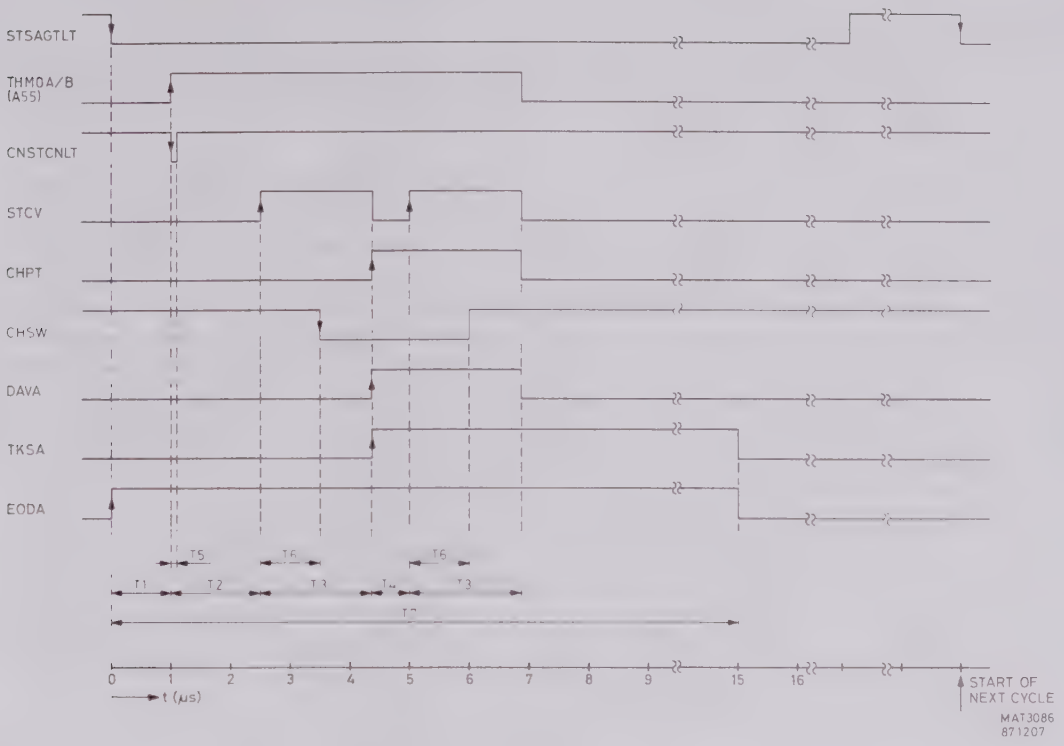


Figure 8.5.1 Timing diagram of acquisition control signals

On the falling edge of STSAGTLT, a sample is taken in the Gate unit A54. and amplified on the Vertical Signal unit A55. After a time (T1) the sample value is stable at the TRACK & HOLD on the Vertical Signal unit and THMOA and THMOB go high to hold the sample.

Next a count pulse (T5) for the STAIR COUNTER (CNSTCNLT) is generated to prepare the Time-base unit A51 for the next sample.

After a time (T2) the TRACK & HOLD is settled and STCV goes high to start conversion of the sample of channel B on the ADC unit A11.
After the conversion time (T3) the ADC needs some time to reset (T4) before the sample of channel B can be converted.
Because the ADC unit has also a TRACK & HOLD circuit. the CHANNEL SWITCH on the Vertical Signal unit may change over as soon as this T&H is in hold mode. This is timed out by T6.
The DAVA signal, which marks to the DPU that valid samples come from the ADC, is only active when the first sample of a sweep is taken, otherwise it is continuous low.
The TKSA signal is only active, when a sample from the ADC should be taken by the DPU. In dual channel mode it operates like given in the diagram above.
If channel A only is selected, it goes low at the falling edge of the second STCV pulse.
If channel B only is selected. it first goes high at the falling edge of the second STCV pulse.

The EODA signal marks the time (T7) in which the above mentioned signals may be active.
The repeat time of the STSAGTLT signal depends on the setting of the instrument and on the frequency of the input signal. The minimum repeat time is 35 us.

The ACL is built around a number of monostable multivibrators, which generate a pulse when they are actived. The above mentioned times T1...T7 are indicated the circuit diagrams. The remaining monostable multivibrators generate a small pulse on their activating edge.
The ADC and T & H unit A11 is clocked by the microprocessor clock. Therefore the generation of the STCV signal is synchronised by UPCK16. If Multiple Sampling is selected, e.g. 4, then every fourth sample should be taken by the DPU and next the stair counter should be incremented. This multiple sampling factor is counted up by two 3-bit counters (D1810). Via multiplexer D1811 the corrected counter line is selected to generate TKSA and CNSTCNLT.
The generation of TKSA is influenced by the signals A, B and DUAL, which depend on the selected vertical channels.
In lower resolution modes, the stair counter should be incremented 2, 4 or 8 times, depending on the selected resolution. This is counted down by counter D1813, which gets its pulses from IC D1812, which operates as a pulse generator.

8.5.4 Signal name list

UNIT A5

Signal name	Description	Signal source	Signal destination(s)
A	Channel A mode	A5	A5
ABØ1...16	Address bus Ø1...16	A6 + Option	-
AB19	Address bus 19	A6	-
B	Channel B mode	A5	A5
CHPT	Channel pointer	A5	A5, A12-A8, A12-A25
CHPT--LT	Channel pointer	A5	A5
CHSW	Channel switch	A5	A12-A25
CKAB--HT	Clock address bus	A5	A5
CKAB--LT	Clock address bus	A5	A5
CLACL	Clear acquisition control logic	A5	A5
CNSTCNLT	Count stair counter	A5	A12-A25-A53-A51
DAHISBLT	Data high strobe	A6 + Option	-
DALOSBLT	Data low strobe	A6 + Option	-
DATRAKLT	Data transfer acknowledge	A3+A5+A6+A8 + Option	A12-A6, A12-Option
DAVA	Data valid	A5	A5, A12-A4, A12-A8
DBØØ...15	Data bus ØØ...15	A6 + Option	-
DUAL	A and B mode	A5	A5

Signal name	Description	Signal source	Signal destination(s)
ENDBBFLT	Enable data bus buffer	A5	A5
EODA	End of data	A5	A5
FBRY	Feedback ready	A8	-
HDSA	Hold sample	A5	A5
HDSA-1	Hold sample 1	A5	A55
ILØ2--LT	Interrupt level Ø2	A8	-
IOSLØ8LT	I/O Select Ø8	A6	-
LEACL	Latch enable acquisition control logic	A25	-
MSCØ...2	Multiple sampling control Ø...2	A5	A5
MYSLDWLT	Memory select down	A6	-
MYSLØ1LT	Memory select Ø1	A6	-
RAABØ1...16	RAM address bus Ø1...16	A5	A5
RAAB19	RAM address bus 19	A5	A5
RADBØØ...15	RAM data bus ØØ...15	A5	A5
RARD--LT	RAM read	A5	A5
RAWR--LT	RAM write	A5	A5
RSACL	Reset acquisition control logic	A5	A5
RSACL--LT	Reset acquisition control logic	A5	A5
RSCØ...2	Resolution control Ø...2	A5	A5
RSSTCNLT	Reset stair counter	A5	A12-A25-A53-A51
SADBØØ...11	Sample data bus	A9+A11	-
SECK1	Serial clock 1	A25	-
SEDA1	Serial data 1	A25	-
SLØØHILT	Select ram ØØ high byte	A5	A5
SLØØLOLT	Select ram ØØ low byte	A5	A5
SLØ1HILT	Select ram Ø1 high byte	A5	A5
SLØ1LOLT	Select ram Ø1 low byte	A5	A5
STCV	Start conversion	A5	A12-A11
STSAGTLT	Start sampling gate	A51	-
TKSA	Take sample	A5	A12-A8
TRRY	Transfer ready	A8	-
UPCK16	Microprocessor clock 16 MHz	A6	-
UPRD--LT	Microprocessor read	A6	-
UPRSOTLT	Microprocessor reset out	A6	-
UPWR--LT	Microprocessor write	A6	-
VBB	Voltage battery backup	A6	-
VBBa	Voltage battery backup a	A5	A5

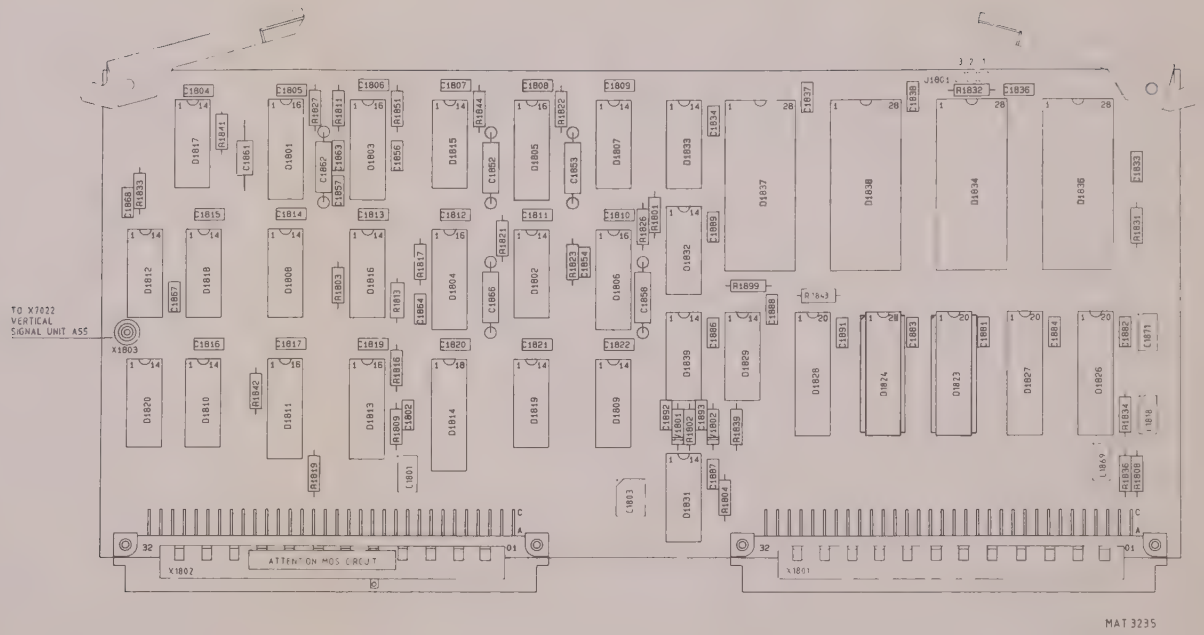
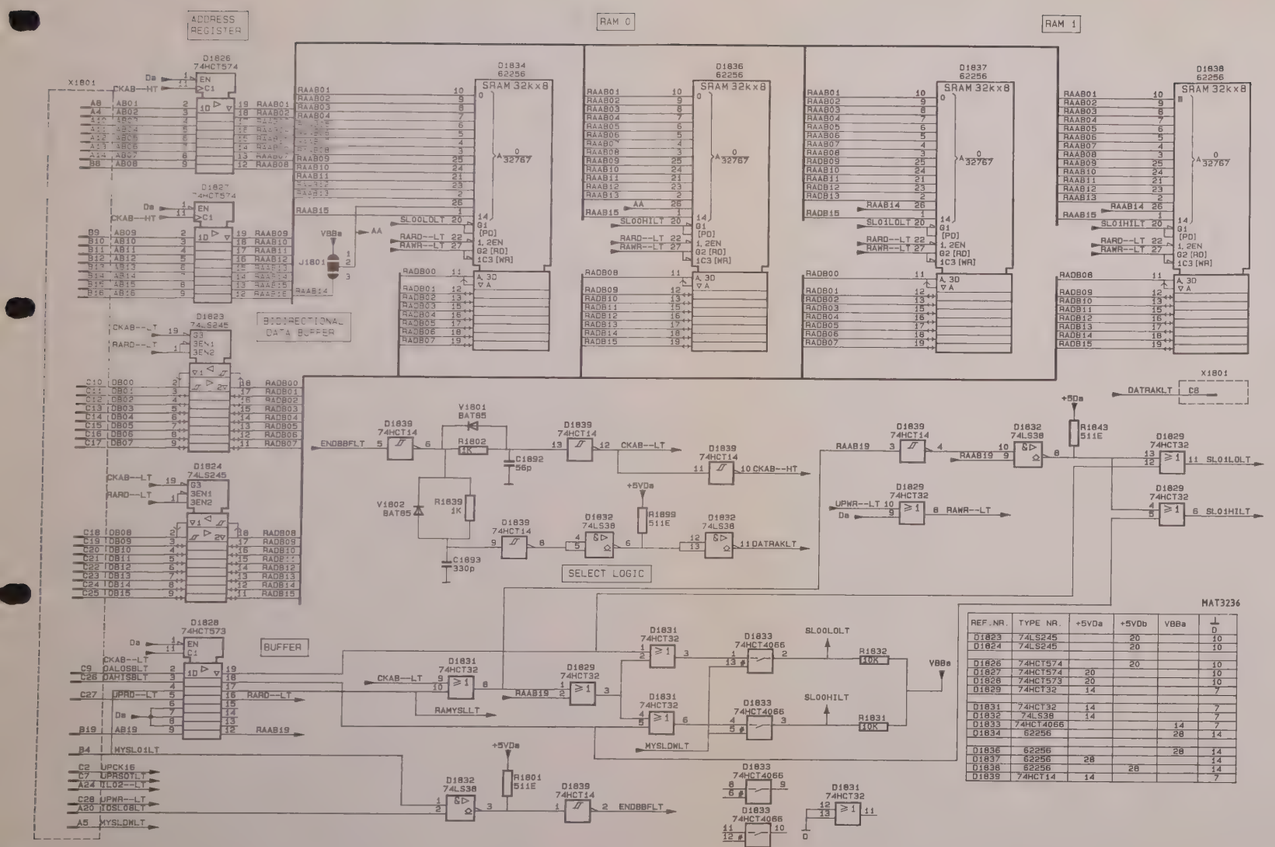
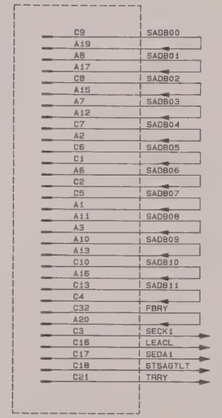
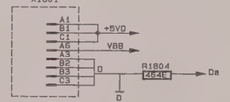


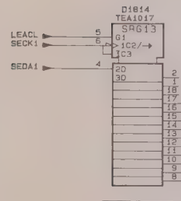
Figure 8.5.2 Unit A5 - GRAM UNIT - p.c.b. lay-out.

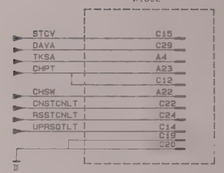


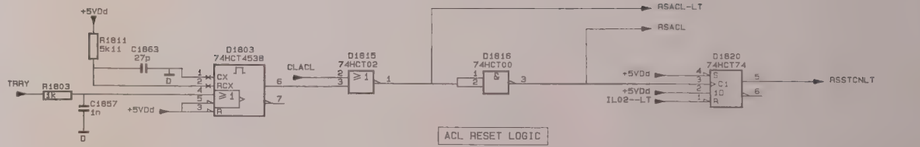
REF.NR.	TYPE NR.	+5Vd	+5VDb	VBBa	⊥
D1823	74LS245		20		10
D1824	74LS245		20		10
D1826	74HCT574		20		10
D1827	74HCT574	20			10
D1828	74HCT573	20			10
D1829	74HCT32	14			7
D1831	74HCT32	14			7
D1832	74LS38	14			7
D1833	74HCT4066			14	7
D1834	62256			28	14
D1836	62256			28	14
D1837	62256	28			14
D1838	62256		28		14
D1839	74HCT14	14			7











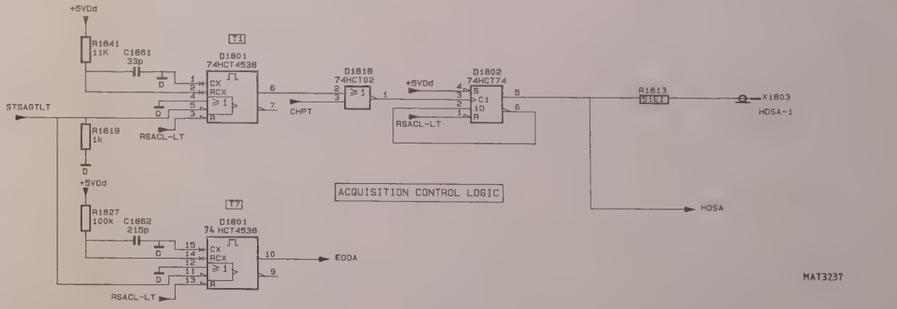
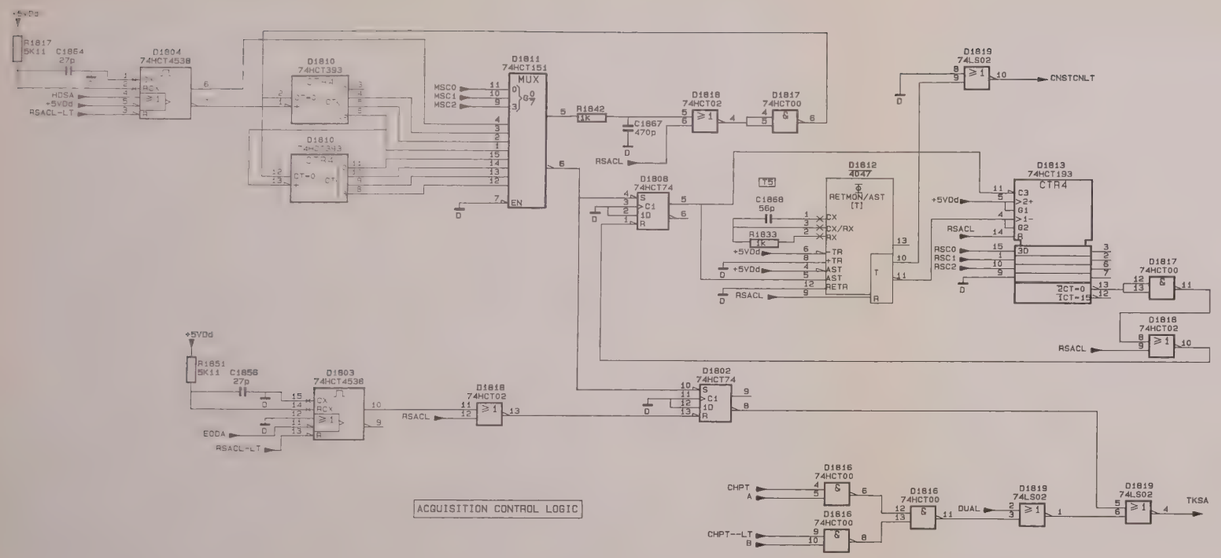
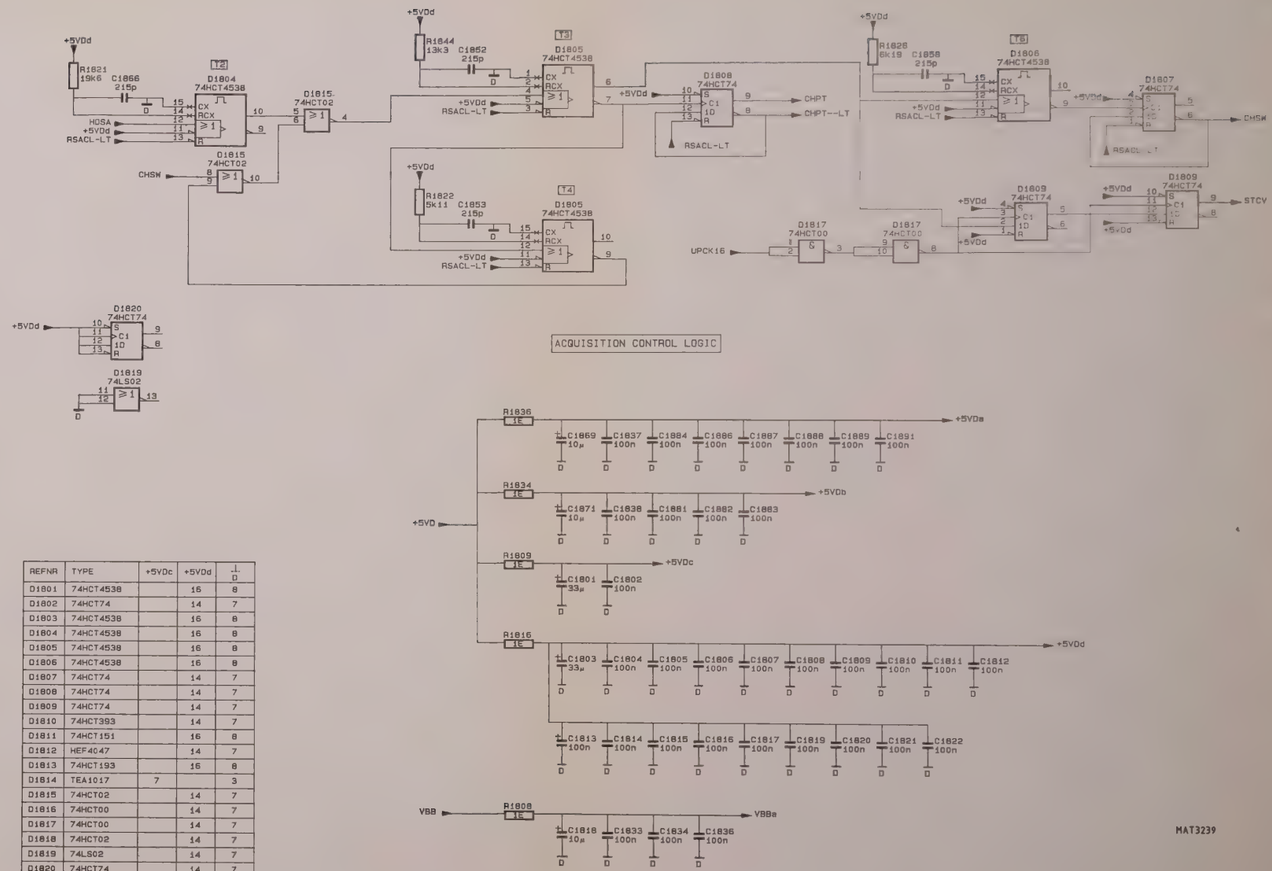


Figure 8.5.3 Unit A5 - GRAM UNIT - circuit diagram.

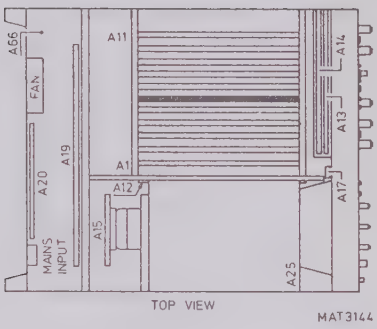




REFNR	TYPE	+5VDc	+5VDd	⊥ D
D1801	74HCT4538		16	8
D1802	74HCT74		14	7
D1803	74HCT4538		16	8
D1804	74HCT4538		16	8
D1805	74HCT4538		16	8
D1806	74HCT4538		16	8
D1807	74HCT74		14	7
D1808	74HCT74		14	7
D1809	74HCT74		14	7
D1810	74HCT393		14	7
D1811	74HCT151		16	8
D1812	HEF4047		14	7
D1813	74HCT193		16	8
D1814	TEA1017	7		3
D1815	74HCT02		14	7
D1816	74HCT00		14	7
D1817	74HCT00		14	7
D1818	74HCT02		14	7
D1819	74LS02		14	7
D1820	74HCT74		14	7

Figure 8.5.4 Unit A5 - GRAM UNIT - circuit diagram.

UNIT A6 - UP UNIT



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8.6.1 General information

This unit mainly consists of a powerfull 68000 microprocessor configuration with EPROM, address decoders, I/O buffers and a clock generator. The microprocessor runs at a clock frequency of 8 MHz.
A bus arbiter has been provided to allow a multiprocessor system, which is used when options are installed in the instrument. The microprocessor has an asynchronous bus structure with a 24 bit address bus and a 16 bit data bus.
Asynchronous means that the microprocessor waits for a "data acknowledge" signal from selected I/O circuitry, before continuing. This enables the microprocessor to handle different access times in I/O circuitry.

8.6.2 Memory map

Only a part of the complete address range is used, according to the following memory map which also gives the memory select signals.

Address (Hex)		
ØØØØØØ Ø3FFFF	ROMØ	Unit A6
Ø4ØØØØ Ø7FFFF	ROM1	
Ø8ØØØØ ØBFFFF	Not used	
ØCØØØØ ØFFFFF	uP I/O	
	Not used	Outside unit A6
CØØØØØ CFFFFF	I/O	I/O Select
DØØØØØ D1FFFF	RAMØ	MYSLØ1LT Unit A5
	Not used	
D2ØØØØ D3FFFF	Display RAM	MYSLØ2LT Unit A4 + unit A3
D4ØØØØ D5FFFF	DPU RAM + I/O	MYSLØ3LT Unit A8
D6ØØØØ D7FFFF	OPTION 2	MYSLØ4LT
D8ØØØØ D9FFFF	RAM1	MYSLØ1LT Unit A5
DAØØØØ FFFFFF	Not used	

A number of I/O select signals select address ranges in the I/O part of the memory map, according to the following table:

Select signal	Selected address range	Used for
IOSLØ3LT	C00000-C1FFFFF	Option
IOSLØ4LT	C20000-C3FFFFF	Front units A13 + A14
IOSLØ5LT	C40000-C5FFFFF	Display unit A3
IOSLØ6LT	C60000-C7FFFFF	Not used
IOSLØ7LT	C80000-C9FFFFF	Management unit A25
IOSLØ8LT	CA0000-CBFFFFF	A.C.L. part unit A5
IOSLØ9LT	CC0000-CDFFFFF	Not used
IOSL1ØLT	CE0000-CFFFFFF	Option

The data acknowledge signal for the microprocessor is generated on this unit (A6) when an I/O select signal is active.When a memory select signal is active the data acknowledge signal is generated on the selected unit via a wired or open collector circuit (DATRAKLT).

8.6.3 Interrupts

Peripheral circuits can generate an interrupt to the microprocessor to ask for special actions. Each interrupt has a priority level according to the table below. The higher the interrupt number is, the higher it´s priority level is. Interrupts with a priority level which is lower than or equal to the priority level of the currently being handled interrupt are inhibited, until the higher priority level interrupt is handled.

Interrupt signal	Comes from
ILØ1--LT	Microprocessor unit A6
ILØ2--LT	DPU unit A9
ILØ3--LT	Front unit A14
ILØ4--LT	Option
ILØ5--LT	Display unit A3
ILØ6--LT	Not used
ILØ7--LT	Power 2 unit A20

The functions of the interrupts are:

ILØ1--LT	Comes every 40 ms. It starts a scan of the front panel keys and updates the status of the pilot lamps.
ILØ2--LT	Marks the end of a DPU program or that the DPU has started to transfer data to the display register RØ.
ILØ3--LT	Marks that one of the rotaries on the front panel has been turned.
ILØ4--LT	Is reserved for use by an option.
ILØ5--LT	Marks the end of a display cycle.
ILØ6--LT	Not used.
ILØ7--LT	Marks that the power goes down.

8.6.4 Circuit description

The MICROPROCESSOR (D1717) is connected via the microprocessor data bus to the BIDIRECTIONAL DATA BUS BUFFER and to ROMØ and ROM1.
ROMØ and ROM1 consists each of two 128K x 8 ROMS, together forming two 128K x 16 ROMs.
If software releases with 64K x 8 ROMS are used, then the soldering joints J1701 and J1702 should be changed over.
The ROMs are addressed via the microprocessor address bus. This bus is buffered to the other units by the ADDRESS BUS BUFFER.
The circuit consisting of D1737, D1741 and D1747 generate the memory select signals and some strobe signals.
The circuit consisting of D1744 and D1746 generate the I/O select signals. Via D1743 and D1714 DATRAKLT goes down with a short delay as one of the I/O select signals goes down.
DATRAKLT can also be pulled down by circuits on other units via pin C8 on connector X1701 and the service switch X1707. This switch can be changed over to generate a data transfer acknowledge by the SLBUENLT signal, which is used by the diagnostic software (see chapter 11.4.4).
The circuit around D1741 generates ROM select signals and some other control signals.
The 3 function control signals are applied to a gate in D1737, which detects the interrupt acknowledge status of the microprocessor, when all function code signals are high. This is used to generate VAPEADLT and memory select control signals.
The monostable multivibrator D1709 keeps the bus busy signal a while active, after the microprocessor has accessed the display RAM. This prevents other microprocessors on options to take over the bus, when the microprocessor has transferred data to the display memory, to assure enough time for the display memory control logic to write the data in the display memory (unit A4).

The BUS ARBITER

The BUS ARBITER consists of a dedicated IC (D1731) and associated logic.
It´s main function is to assign control of the microprocessor busses to the microprocessor that claims the control.
When no options are installed in the instrument there is only one microprocessor, so the bus arbiter has no real arbiter function.
If UPAB23 at D1734 pin 13 goes high, then RQCL to the BUS ARBITER goes high. Now the BUS ARBITER circuit makes ABBUENLT and SLBUENLT low, which enables all buffers to the CCU-bus. This enables the microprocessor to access memory and I/O ports on other units via the CCU-bus.
The BUS ARBITER circuit is reset by the microprocessor reset signal (UPRSOTLT) from the RESET/HALT logic.
The capacitors C1754...C1761 and resistor network R1726 give delay times, which time the taking over of the microprocessor busses by another microprocessor.

The associated logic generates a number of control signals for the arbiter function as well as for normal microprocessor functions. The shift register D1748 generates the CLWR--LT signal that lies with its edges between the edges of one of the memory select signals. So first the memory select signal goes down, next the CLWR--LT pulse and UPWR--LT pulse at D1721 come and finally the memory select signal goes high.

The CLOCK GENERATOR consists of a compact integrated crystal oscillator of 16 MHz (G1701) and a number of divider stages. The table below gives the frequency of the generated signals.

Name	Frequency
UPCK16	16 MHz
UPCKØ8	8 MHz
UPCK	8 MHz
Z-MO-XT	200 kHz
TIC	25 Hz

By changing over soldering joint J1707 all frequencies are divided by 2. This can be used to detect access time problems.

The INTERRUPT PRIORITY LEVEL ENCODER (D1708) encodes 7 offered interrupt levels to a 3 bit binary code (IPLØ...2), which is applied to the microprocessor. A reaction of the microprocessor on ILØ1--LT might be postponed a while, because interrupts with a higher priority are present. Now flipflop D1704 keeps ILØ1--LT low, when TIC goes high after 20 ms. When the interrupt is acknowledged the flipflop is reset by TCRS--LT.
Gate D1739 is a buffer between the HCT logic on unit A3 and the LS TTL logic of D1708.
ILØ7--LT (power down) is also routed to the reset/halt logic, to halt the microprocessor.

The WATCHDOG consists of a retriggerable monostable multivibrator (D1709), an oscillator (D1712) and the reset/halt logic.
When the microprocessor program runs normally, the multivibrator is retriggered within every 2 seconds by WD----LT. This keeps pin 12 of D2709 low. Via D1712 UPRSOTLT and UPHA--LT stay high.
When another microprocessor has taken over control over the system, WD----LT is generated by this microprocessor.
If the WD----LT signal does not come within 2 seconds (e.g. due to an abnormal program sequence) pin 12 of D1709 goes high. Now the microprocessor is halted by UPHA--LT and the hardware is reset by UPRSOTLT.
The gate of D1712 pins 1, 2 and 3 forms an oscillator, so after about 2 seconds UPHA--LT and UPRSOTLT become inactive. The microprocessor will restart, generate the WD----LT signal and so on.
If for some reason the microprocessor should not restart correctly the oscillator of D1712 gives a halt plus reset after 2 seconds and after another 2 seconds the microprocessor can restart again. The strap X1708 allows disabling of the watchdog, which is used for the diagnostic software (see section 11.4).
A start of the microprocessor and a restart caused by the watchdog initiates the power up routine (see section 11.4).
If the power goes down ILØ7--LT halts the microprocessor via pin 5 of D1712. Capacitor C1753 keeps ILØ7--LT long enough low at power up, to be sure that all supply voltages are present when the microprocessor starts.
The signal ILØ7--LT is also connected to testpoint X1713, which is located next to ground testpoint X1714.
By interconnecting these testpoints the microprocessor can be restarted.

The INPUT PORT enables the microprocessor to read the status of 3 service switches and the status of the battery.
Service switch X1703 is read by the microprocessor to detect in which type of instrument it is placed, to start up the appropriate software. In this instrument the switch should be open (see figure 8.6.1).
Service switches X1704 and X1706 have functions for the diagnostic software (see section 11.4.4).

Via the OUTPUT PORT, the microprocessor generates the watchdog signal WD----LT with the open collector gate D1714. The battery test circuit is also controlled via the output port.

The BATTERY TEST circuit loads the battery via V1702 and R1712 with a specified current, when the condition of the battery has to be tested after a (re)start of the microprocessor. The COMPARATOR compares the battery voltage with a reference voltage from V1701. When the battery voltage is too low, BAST goes high, which is read by the microprocessor via the input port.

The SUPPLY VOLTAGE SWITCH switches +5D off, when this voltage is too low.
When the power is on, +5D supplies the memories via V1712. V1707 prevents that the batteries are charged by +5D.
When +5D goes too low as the instrument is switched off, V1711 and V1712 block.
Now the memories are supplied by the battery via V1707. The blocking diode V1712 prevents that the battery supplies back to +5D.
V1708 will also block, MYSLDWLT will go down, which will deselect the memories. Their contents will remain.

8.6.5 Signal name list

UNIT A6

Signal name	Description	Signal source	Signal destination(s)
ABØ1...2Ø	Address bus Ø1...2Ø	A6+Option	General
ABBUENLT	Address bus enable	A6	A6
BAST	Battery status	A6	A6
BATS	Battery test	A6	A6
BAVO	Battery voltage	A66	-
BSBU--LT	Bus busy	A6+Option	A6,Option
BSGROTHT	Bus grant output	A6	Option (1)
BSRQ--LT	Bus request	A6+Option	A6,Option
CLWR--LT	Clocked write	A6	A6
DAAK--LT	Data acknowledge	A6	A6
DAAKBSLT	Data acknowledge bus	A6	A6
DAHISBLT	Data high strobe	A6+Option	A12-A3,A12-A5
DALOSBLT	Data low strobe	A6+Option	A12-A3,A12-A5
DASB--HT	Data strobe	A6	A6
DATRAKLT	Data transfer acknowledge	A3+A5+A6+A8 +Option	A6,Option
DBØØ...15	Data bus ØØ...15	A6+Option	General
ENAD--LT	Enable address	A6	A6
FCØ...2	Function code Ø...2	A6	A6
ILØ1--LT	Interrupt level Ø1	A6	A6
ILØ2--LT	Interrupt level Ø2	A8	-
ILØ3--LT	Interrupt level Ø3	A14	-
ILØ4--LT	Interrupt level Ø4	Option	-
ILØ5--LT	Interrupt level Ø5	A3	-
ILØ6--LT	Interrupt level Ø6	A25	-
ILØ7--LT	Interrupt level Ø7	A20	-
IPLØ...2	Interrupt priority level Ø...2	A6	A6
IOSLØ3LT	I/O Select Ø3	A6	A12-Option
IOSLØ4LT	I/O Select Ø4	A6	A12-A14
IOSLØ5LT	I/O Select Ø5	A6	A12-A3
IOSLØ6LT	I/O Select Ø6	A6	A12-A25-A26
IOSLØ7LT	I/O Select Ø7	A6	A12-A25
IOSLØ8LT	I/O Select Ø8	A6	A12-A5
IOSLØ9LT	I/O Select Ø9	A6	A12-Option
IOSL1ØLT	I/O Select 1Ø	A6	A12-Option
LODASBLT	Lower data strobe	A6	A6
MASL--LT	Master selected	A6+Option	A6,Option
MYSLØ1LT	Memory select Ø1	A6+Option	A12-A5
MYSLØ2LT	Memory select Ø2	A6+Option	A12-A3,A12-A4
MYSLØ3LT	Memory select Ø3	A6	A12-A8
MYSLØ4LT	Memory select Ø4	A6	A12-Option
MYSLALHT	Memory select all	A6	A6
MYSLALLT	Memory select all	A6	A6
MYSLDWLT	Memory select down	A6	A12-A4,A12-A5,A12-Option
RDRO	Read ROM	A6	A6
RDSB--LT	Read strobe	A6	A6

(1) Becomes BSGRINHT on option.

Signal name	Description	Signal source	Signal destination(s)
RQCL	Request clock	A6	A6
SLBUENLT	Select bus enable	A6	A6
SLRO$\emptyset$	Select ROM $\emptyset$	A6	A6
SLRO1	Select ROM 1	A6	A6
TCRS--LT	TIC reset	A6	A6
TIC	Timer interrupt clock	A6	A6
TSLMA-LT	Timing slave to master	A6	A6
UPAB$\emptyset$1...23	Microprocessor address bus $\emptyset$1...23	A6	A6
UPADSBHT	Microprocessor address strobe	A6	A6
UPADSBLT	Microprocessor address strobe	A6	A6
UPCK	Microprocessor clock	A6	A6
UPCK$\emptyset$8	Microprocessor clock 8 MHz	A6	A12-A4,A12-A8,A12-Option A12-A3,A12-A9
UPCK16	Microprocessor clock 16 MHz	A6	A12-A5 A12-A8 A12-A11
UPDASBLT	Upper data strobe	A6	A6
UPDB$\emptyset\emptyset$...15	Microprocessor data bus $\emptyset\emptyset$...15	A6	A6
UPHA--LT	Microprocessor halt	A6	A6
UPIN--HT	Microprocessor input port	A6	A6
UPOT--HT	Microprocessor output port	A6	A6
UPRD--LT	Microprocessor read	A6	General
UPRDWR	Microprocessor read/write	A6	General
UPRSOTLT	Microprocessor reset out	A6	A12-A3,A12-Option,A12-A5-A12-A25
UPWR--LT	Microprocessor write	A6	General
VAPEADLT	Valid peripheral address	A6	A6
VAPESLLT	Valid peripheral select	A6	A6
VBB	Voltage battery backup	A6	A12-A5,A12-Option
WD----LT	Watch dog	A6+Option	A6
WRSB--LT	Write strobe	A6	A6
Z-MO--XT	Z-modulation	A6	A12-A1

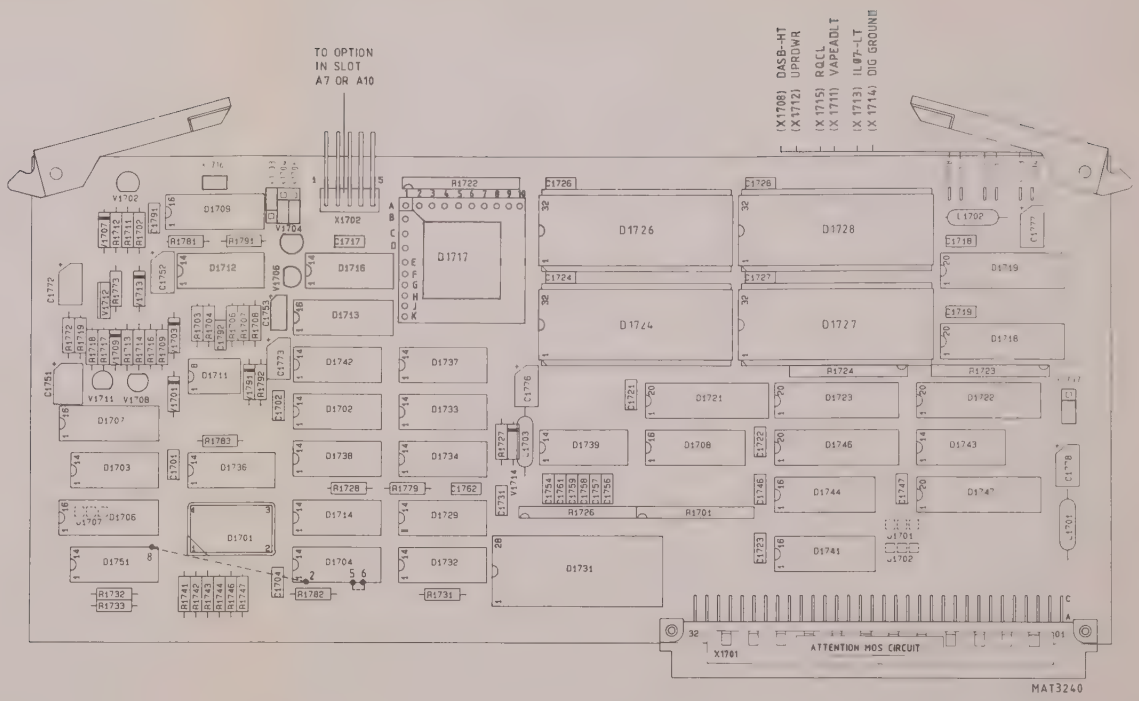


Figure 8.6.1 Unit A6 - UP UNIT - p.c.b. lay-out.

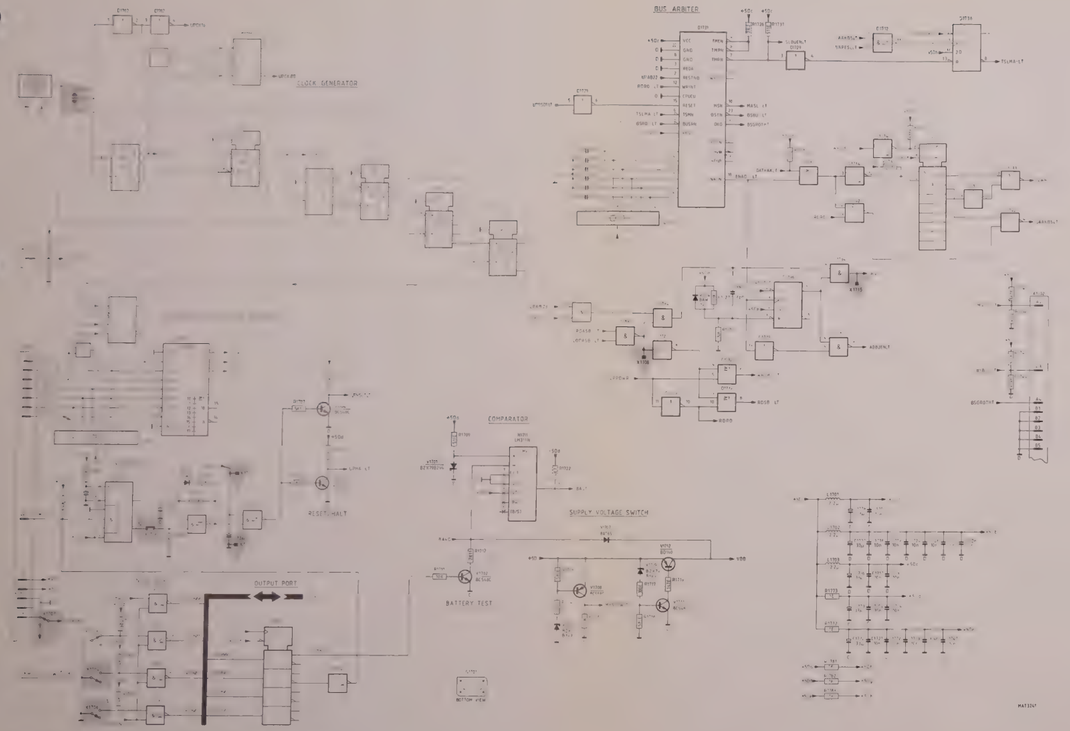


Figure 8.6.2 Unit A6 - UP UNIT - circuit diagram.

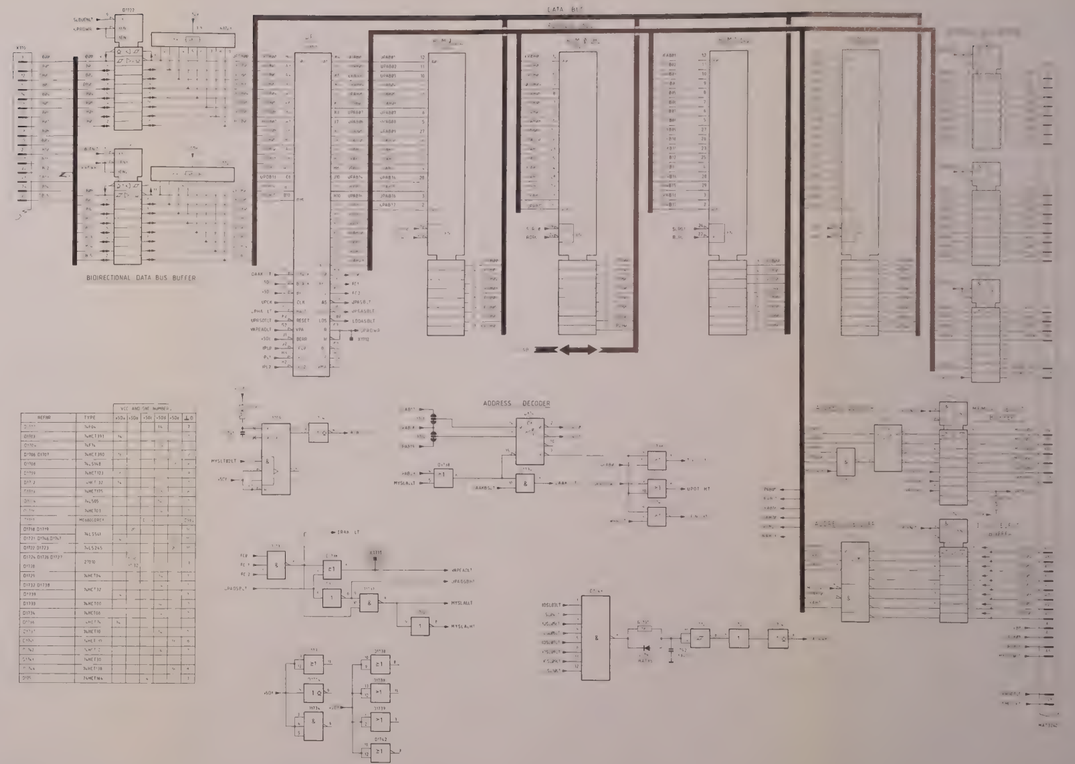
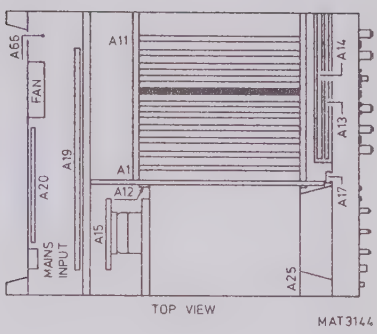


Figure 8.6.3 Unit A6 - UP UNIT - circuit diagram.

UNIT A7 - OPTION 1



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8.7.1 General information

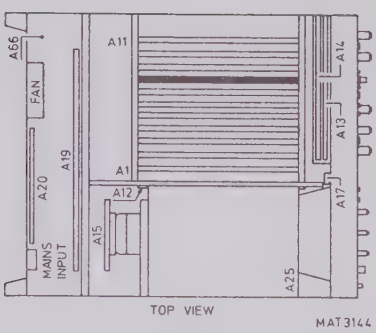
This OPTION 1 slot is reserved for an optional printed circuit board.

Normally the Interface board is installed in this slot.

A second slot (OPTION 2) is also available in this instrument (see section 8.10.1).

NOTE: The first option to be installed in this instrument must always be placed in the OPTION 1 slot. The OPTION 2 slot may only be used if an option is installed already in the OPTION 1 slot.

UNIT A8 - DPU CONTROL UNIT



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8.8.1 General information

The DPU CONTROL forms together with the DPU (Data Processing Unit) a fast Data Processor with an instruction cycle time of 125 ns.
The main function of the Data Processor is to accept sample data from the ADC, to perform calculations on it, to load the data in register RØ of the Display unit and to feed back sample data to the feedback DACs on the Management unit (see figure 8.8.1).

Other functions are:

- add samples of both channels in ADD mode
- invert samples of one or both channels
- linear interpolation
- flag handling (e.g. overflow)
- average calculations
- turning off feedback in eye pattern mode.

To perform these functions there are lines to the Acquisition Control Logic on unit A5, the ADC on unit A11, the Display Memory + Control on units A3 and A4 and the Feedback DACs on the Management unit A25.
The Data Processor gets its programs from the microprocessor.
When a program is finished or other DPU actions have to be reported, an interrupt to the microprocessor (ILØ2--LT) is generated.
Normally it is rather difficult to check the proper operation of the Data Processor. Therefore it is recommended to use the "DPU test", which is in the diagnostic software (see chapter 11).

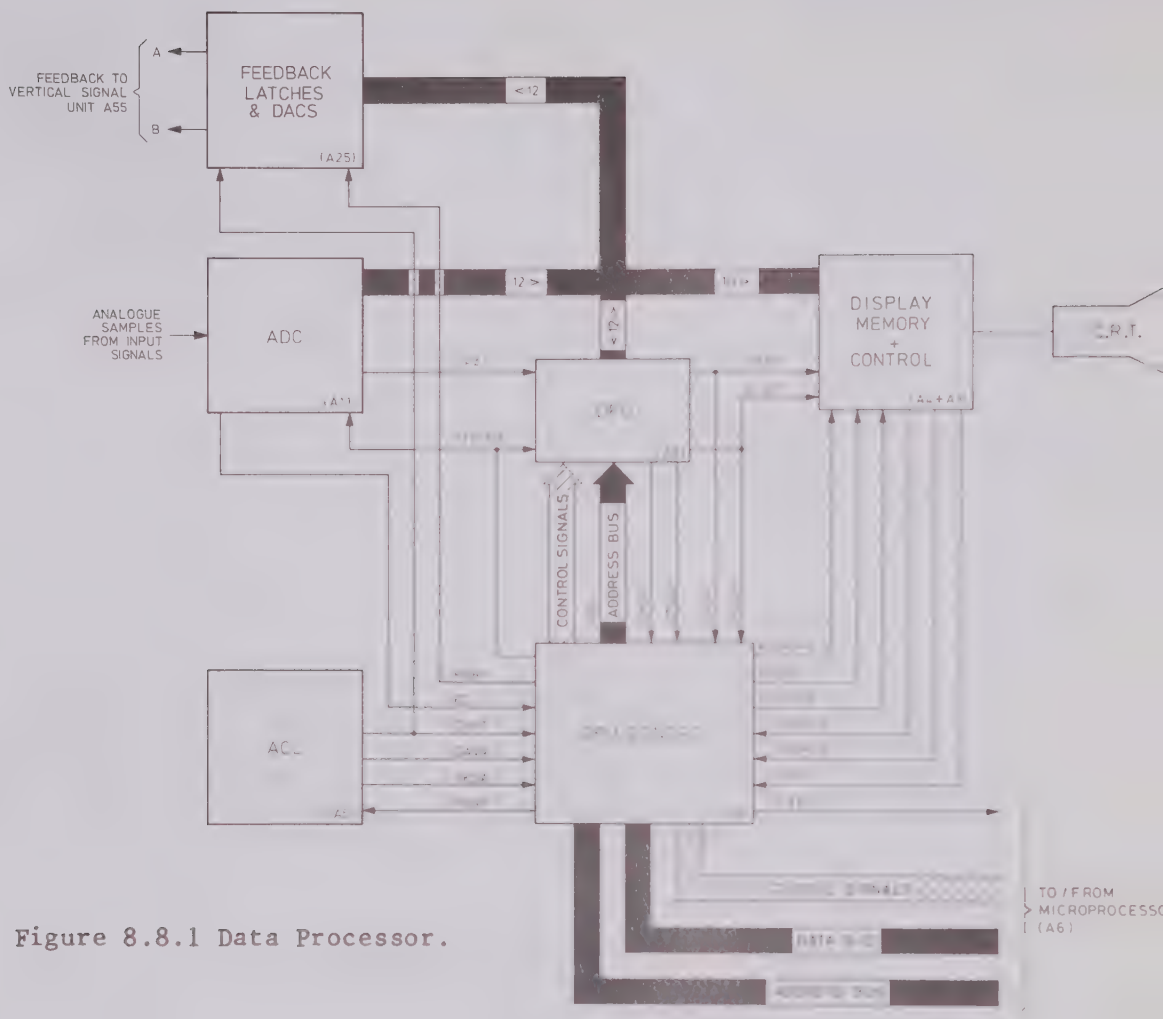

Figure 8.8.1 Data Processor.

8.8.2 Circuit description

The DPU (unit A9) performs the calculations on the sample data. To be able to do this, it receives a number of control signals and addresses from the DPU CONTROL.
These are derived from program words that are stored in the control memory.
The format of these 32 bit program words is defined as follows:

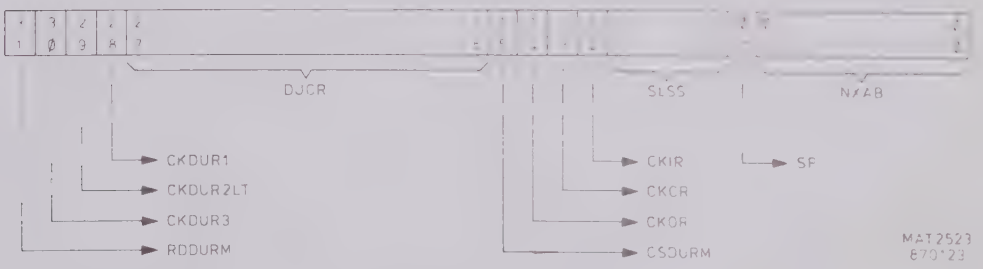

Figure 8.8.2 Program word format.

bits ØØ...Ø6	are the 7 less significant bits of the address of the next instruction
bit Ø7	marks the end of a program
bits Ø8...11	selects statusbit in case of a conditional jump
bit 12	if set bits 16...27 are data for the instruction register
bit 13	if set bits 16...27 are data for the control register
bit 14	if set bits 16...27 are data for the offset jump register
bit 15	if set it generates the signal CSDURM for the DPU
bits 16...27	data for the instruction register or control register or offset jump register, depending on the status of bits 12...14
bits 28...31	if set they generate respectively the signals CKDUR1, CKDUR2LT, CKDUR3 and RDDURM for the DPU.

The control memory may contain one or more programs with a maximum length of 128 words (7 address bits).
The program which is selected depends on the 4 most significant address lines (bits Ø8...11).
The DPU CONTROL consists of the following parts:

- address decoder
- mode register
- start/stop logic
- status multiplexer
- address multiplexer
- control memory
- buffer
- pipeline register
- instruction register
- control register
- address generator

The ADDRESS DECODER, which mainly consists of IC D1401, decodes some address lines from the microprocessor to the select signals SLOTØ...6. Because the logic on this unit is fast enough, the DATRAKLT signal can go low immediately when MYSLØ3LT goes low.
IC D1424 generates a clock signal for the mode register when SLOT2 goes low and the SLAB signal when UPSL goes high.
Furtheron this part contains some buffers for clock signals.

The MODE REGISTER (D1418) is an 8 bit latch that latches data from the microprocessor for the control of the start/stop logic.

The START/STOP LOGIC mainly consists of FPLS D1452 (Field Programmable Logic Sequencer). It generates a number of control signals depending on the status of its input signals.
Three outputs and the output of the status multiplexer are latched by IC D1458. The four outputs determine via the address multiplexer the four most significant address bits of the next instruction. If output pin 16 or pin 17 of D1457 goes low ILØ2--LT is generated via D1404. The microprocessor reads then via D1423 the status of both outputs. The going low of pin 17 marks that the DPU has finished its program.

The STATUS MULTIPLEXER consists of two 1 of 8 multiplexers (D1402 and D1403), which form together a 1 of 16 multiplexer.
The status signal that is selected is determined by the SLSSØØ...Ø3 signals from the pipeline register b.

The ADDRESS MULTIPLEXER (D1409, D1411 and D1412) is a 12 bit multiplexer of which 11 bits are used.
When a DPU program is executed SLAB is low. NXABØØ...NXØ6 and four output signals of D1458 are selected. The address of the next word in the control memory is determined by the 7 less significant bits of the current word and the signals SS1, IS, CLØ and CL1.
When a DPU program is loaded in the control memory by the microprocessor, SLAB is high. The address where the word is loaded is determined by the address selected by the microprocessor.

The CONTROL MEMORY is a 2048 x 32 ram. It is built with four 2048 x 8 ram's (D1426...1429). SLOTØ is the write signal for the lower 16 bits of a word, SLOT1 is the write signal for the higher 16 bits of a word.
When a DPU program is executed both are high, which results in the read status of the ram. The data on the DUIR bus are determined by the address on the IRAB.

The buffer is a 32 bit buffer (D1413, D1414, D1416 and D1417) between the microprocessor data bus and the DUIR bus. It seperates data on both buses when a DPU program is executed.
When a DPU program is loaded, data from the microprocessor are transferred to the control memory by the SLOTØ and SLOT1 signals, which also control the control memory.

The PIPELINE register is a 32 bit register (D1431...1434), which holds the current instruction, while the next instruction is fetched from the control memory. It is clocked by CKPL, which is generated by the start/stop logic.
At the outputs of the register the definition of the program word can be recognized.

The INSTRUCTION REGISTER (D1441 + D1442) is a 12 bit latch, that latches 12 signals for the DPU. It is clocked by CKIR, which is derived from bit 12 of the program word via D1459.

The CONTROL REGISTER (D1438 + D1439) is a 12 bit latch, that latches 12 signals, which are mainly used on this unit. It is clocked by CKCR, which is derived from bit 13 of the program word.

The ADDRESS GENERATOR generates addresses for the pretrigger ram, the average ram and the flag ram on the DPU.
It consists of the following parts:

- buffer
- offset jump register
- address register
- adder
- pretrigger counter
- multiplexer
- trigger address comparator

The BUFFER is a 12 bit buffer (D1421 + D1422), which latches data from the microprocessor. It is clocked by SLOT4.
When OTDIPR is low the data are put on the DPU address bus (DUABØØ...11).DUABØØ is also led to the status multiplexer.

The OFFSET JUMP REGISTER (D1436, D1419 + D1437) consists of two parts. If OTENDT is low, D1436 and D1437 latch DUCRØØ...11, which is the offset jump. D1436 and D1437 are clocked by CKOR, which is derived from bit 14 of the program word. The output signals are applied to the adder.
If OTENDT is high DBØ8...DB15 are latched by D1419 on SLOT2. D1437 is reset.
The output signals of D1419 and D1437 are applied to the adder.
Due to the inverter D1406 either the outputs of D1436 or D1419 are enabled.

The ADDRESS REGISTER (D1443 + D1444) is a 12 bit latch, which latches data from the DPU address bus. It is clocked by CKAD. It can be reset by RSAD--LT.

The ADDER is a 12 bit adder, which adds data from the offset jump register and the address register. The carry signal (CYAA) is led to the status multiplexer.

The preset value is loaded from the DPU address bus by LDPRCNLT. The counter value is applied to the pretrigger address bus (PRABØØ...11). When all counter bits are "1" TCPRCN is generated by D1404. It is led to the status multiplexer.

The MULTIPLEXER (D1449, D1451 and D1452) selects data from the adder or from the pretrigger counter. The data are applied to the DPU address bus.
When SLPRAB is low, the data from the adder are selected, otherwise data from the pretrigger is selected.
Because OTDIPR and OTDIMX are in antiphase (D1406 pin 3 and 4) either the buffer or the multiplexer writes data to the DPU address bus.

8.8.3 Signal name list

UNIT A8

Signal name	Description	Signal source	Signal destination(s)
ABØ2...12	Address bus Ø2...12	A6+Option	-
CHPT	Channel pointer	A5	-
CKAD	Clock address register	A8	A8
CKCL	Clock cycle counter	A8	A8
CKCR	Clock control register	A8	A8
CKDUR1	Clock DPU register I	A8	A12-A9
CKDUR2LT	Clock DPU register II	A8	A12-A9
CKDUR3	Clock DPU register III	A8	A12-A9
CKDUØ8LT	Clock DPU 8 MHz	A8	A8
CKDU16LT	Clock DPU 16 MHz	A8	A8
CKF	Clock flags	A8	A12-A9
CKIR	Clock instruction register	A8	A8
CKOR	Clock offset jump register	A8	A8
CKPL	Clock pipeline register	A8	A8
CLØ...1	Cycle Ø...1	A8	A8
CNCPCN	Count copy address counter	A8	A12-A4
CO	Complement	A8	A12-A9
CSDURM	Chip select DPU ram	A8	A12-A9
CYAA	Carry address adder	A8	A8
CYOT	Carry out	A9	-
DATRAKLT	Data transfer acknowledge	A8+A3+A5+ A6+Option	A12-A6, A12-Option
DAVA--03	Data valid	A5	-
DBØØ...15	Data bus ØØ...15	A6+Option	-
DUABØØ...11	DPU address bus ØØ...11	A8	A12-A9, A12-A4
DUCRØØ...11	DPU control register ØØ...11	A8	A8
DUIRØØ...31	DPU instruction register ØØ...31	A8	A8
EC	End of conversion	A11	-
ENCP	Enable copy	A8	A8
ENCPSA	Enable copy sample	A4	-
ENOFD	Enable overflow detection	A8	A12-A9
ENPRCN	Enable pretrigger counter	A8	A8
FBRY	Feedback ready	A8	A12-A9, A12-A5-A12-A25
ILØ2--LT	Interrupt level Ø2	A8	A12-A6, A12-A5
IRABØØ...1Ø	Instruction register address bus ØØ...1Ø	A8	A8
IS	Initialisation	A8	A8
LDPRCNLT	Load pretrigger counter	A8	A8
LEDP	Latch enable display	A8	A12-A4
MYSLØ3LT	Memory select Ø3	A6	-

Signal name	Description	Signal source	Signal destination(s)
NXABØØ...Ø6	Next address bus ØØ...Ø6	A8	A8
OEDUØØ	Output enable DPU ØØ	A8	A12-A9
OEDUØ1	Output enable DPU Ø1	A8	A12-A9
OFDP	Overflow display	A9	-
OTCM	Output comparator	A4	-
OTDIAD	Output disable ADC	A8	A12-A9, A12-A11
OTDIMX	Output disable multiplexer	A8	A8
OTDIPR	Output disable pretrigger	A8	A8
OTENDT	Output enable delta-t	A8	A8
OTLD	Output limit detection	A9	-
PRABØØ...11	Pre-trigger address bus ØØ...11	A8	A8
RDDURM	Read DPU ram	A8	A12-A9
RLDP	Read sample display	A9	-
RSAD--LT	Reset address register	A8	A8
RSDU--LT	Reset DPU	A8	A12-A4
RSDUR--LT	Reset DPU registers	A8	A12-A9, A12-A4
SFSRØØ	Select function shift register ØØ	A8	A12-A9
SFSRØ1	Select function shift register Ø1	A8	A12-A9
SLAB	Select microprocessor address bus	A8	A8
SLAM	Select average memory	A8	A12-A9
SLOFAD	Select overflow ADC	A8	A12-A9
SLOTØ...6	Select output Ø...6	A8	A8
SLPRAB	Select pretrigger address bus	A8	A8
SLSSØ...6	Select status Ø...6	A8	A8
SP	Stop	A8	A8
SS	Status	A8	A8
SS1	Status 1	A8	A8
STRLF	Set real sample flag	A8	A12-A9
SYDP	Synchronize display	A3	-
TCCPCN	Terminal count copy address counter	A4	-
TCPRCN	Terminal count pre-trigger counter	A8	A8
TKSA	Take sample	A5	-
TRRY	Transfer ready	A8	A12-A5
UPCKØ8	Microprocessor clock 8 MHz	A6	-
UPCK16	Microprocessor clock 16 MHz	A6	-
UPDO	Up/Down	A8	A8
UPRD--LT	Microprocessor read	A6	-
UPWR--LT	Microprocessor write	A6	-
UPSL	Microprocessor select	A8	A8

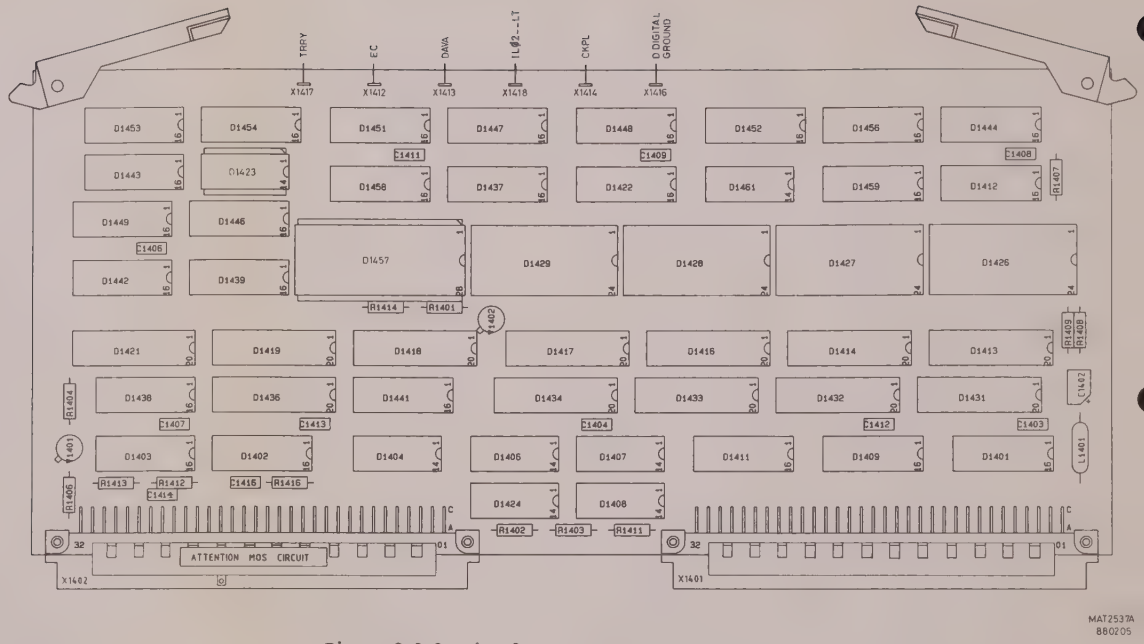

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Figure 8.8.3 Unit A8 - DPU CONTROL UNIT - p.c.b. lay-out.

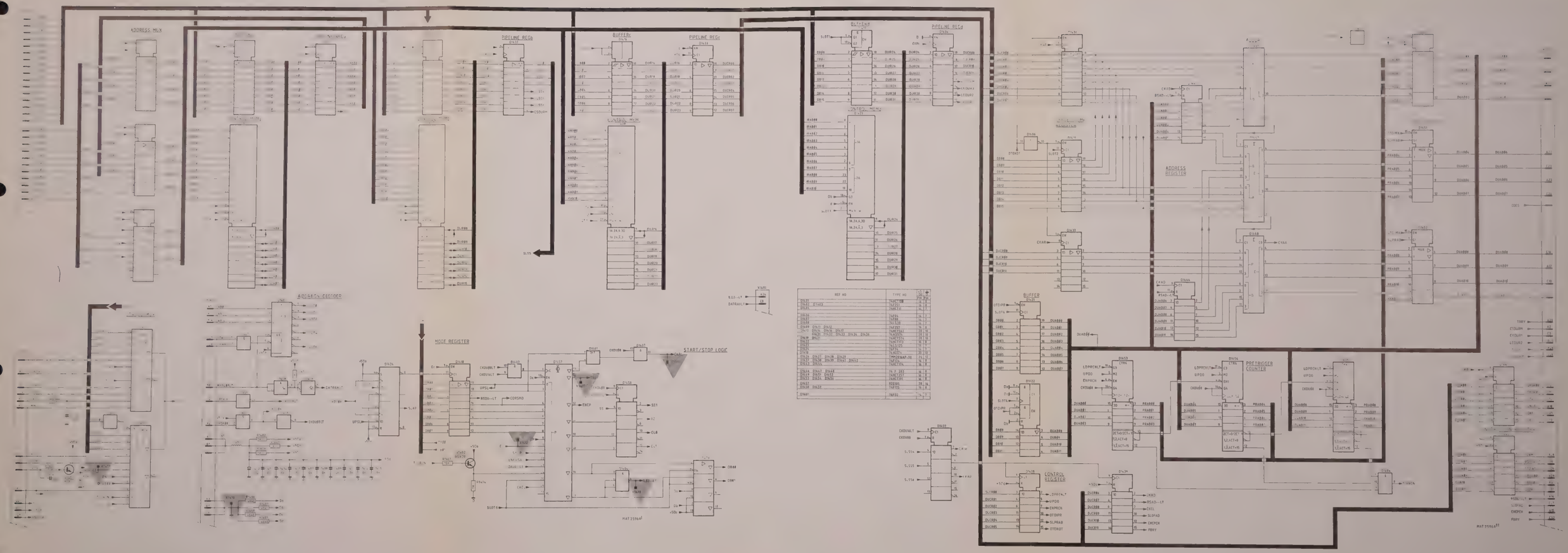
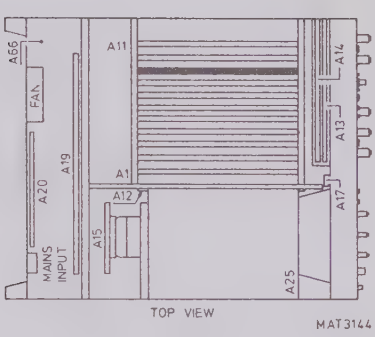


Figure 8.8.4 Unit A8 - DPU CONTROL UNIT - circuit diagram.

UNIT A9 - DPU UNIT



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8.9.1 General information

The DPU (Data Processing Unit) forms together with the DPU control (unit A8) a fast Data Processor. It is recommended to read first chapter 8.8.1 and 8.8.2 before reading chapter 8.9.2.

8.9.2 Circuit description

The DPU consists of the following parts:

- buffer
- register I
- complementer
- adder
- register III
- overflow detection
- reflection suppression
- shift register
- limit detection
- register II
- pretrigger ram
- average ram
- flag ram
- flag handler

All these parts, excepted the adder and the overflow detection, are interconnected via the 16 bits wide DPU data bus (DUDBØØ...15).

The BUFFER is a bidirectional data buffer (D1203, D1204 and D1206). To convert the 12 sample data bits to 16 DPU data bits SADB11 is applied to DUDB11...15.
Ten processed sample data bits (SADBØØ...Ø9) are applied to the display memory (unit A4).
When OTDIAD is low, data are transferred from the ADC (unit A11) to the DPU. When OTDIAD is high LEDP is high, data is transferred from

the DPU to the display memory. When OTDIAD is high and FBRY is high, data is transferred from the DPU to the Feedback DACs on the Management unit A25.

REGISTER I (D1216 + D1217) is a resettable latch, which is clocked by CKDUR1. It is used for various latching functions.

The COMPLEMENTER (+/-) complements data (D1211...D1214). It is used for substractions with the adder.
Because the DPU calculates in two's complement notation, after complemention 1 should be added to get the correct negative number. This is done by the CO signal on the carry input of the adder (D1218 pin 7).

The ADDER (D1218, D1219, D1221, D1222) adds the data from the complementer and register I.
The carry signal at pin 9 of D1222 can generate the CYOT signal via some logic (D1223).

REGISTER III (D1224 + D1226) is a latch, that latches the output result of the adder. It is clocked by CKDUR3.

The OVERFLOW DETECTION (D1231 and associated components) latches on CKDUR3 an overflow bit from D1228 pin 3 and a sign bit from D1222 pin 10 in D1231. So the two bits belong to the data that is clocked in register III. The table below shows which overflow is selected:

SLOFAD	ENOFD	Overflow from
X	0	always "1"
0	1	ADDER
1	1	ADC

Via the logic in D1227 the OTDI3 signal enables wether register 3 by OTEN3-LT or the reflection suppression by OTENRSLT, depending on the presence of overflow.

D1254 decodes the OEDUØØ and OEDUØ1 signals to register control signals, which are active when RDDURM is low.

The REFLECTION SUPPRESSION (D1236...D1239) puts data on the DPU data bus when an overflow occurs, instead of Register III. It consists of a multiplexer, that selects 0000 0000 0011 1111 or 1111 1111 1100 0000, depending on the sign bit from D1231 pin 8.
This circuit prevents the arise of reflection of the input signal in the bottom of the display when high input voltages cause overflow in the display amplitude.
The same is valid in the top of the display with high negative input voltages.

The SHIFT REGISTER (D1242 + D1243) reads data from the DPU data bus, shifts them (left or right) and writes them back to the DPU data bus. This is used for multiplication or division by factors which are a multiple of 2.
The contents of the shift register can be cleared by RSSR--LT, which is used to write zeroes to the DPU data bus.
The signals SFSRØØ and SFSRØ1 determine the function of the register (shift left or right, load or hold) on the clock signal CKSR.

The LIMIT DETECTION detects wether DUDBØ4...11 are all zero or one. This means that the data on the data bus represents a number that is between -16 and +16. This is used for some calculations.

REGISTER II (D1207 + D1208) is a latch, which is used for the intermediate storage of calculation results. It is clocked by CKDUR2LT. When OTDI2 is low, the register writes its data to the DPU data bus.

The PRETRIGGER + AVERAGE RAM consists of two 8Kx8 rams (D1249 + D1251), forming together an 8Kx16 ram. The lower address range is used as a 4Kx16 pretrigger ram. The higher address range is used as a 4Kx16 average ram.
The addresses for the ram are generated by the address generator on the DPU control (unit A8).
The highest address bit of the ram (pin 2) determines wether the pretrigger or the average ram is selected.
In the pretrigger ram a data word consists of 14 data bits, a real sample flag bit and an overflow flag bit.
In the average ram a data word consists of 16 data bits.

The FLAG RAM consists of a REAL SAMPLE FLAG RAM and an OVERFLOW FLAG RAM. Each consists of a 4Kx1 ram (D1252 and D152), which contain the flags for the data in the average ram.
A real sample flag indicates wether a sample is a real taken sample or a sample that is obtained by means of interpolation between two real samples.
An overflow flag indicates an overflow of a sample. If one or both of two real samples behind each other have an overflow flag, all interpolated samples between them have an overflow flag.

The main functions of the FLAG HANDLER (D1241 and D1232...D1234) are given in the table below.

RDDURM	SLAM	Function of flag handler
0	0	Write flags (STRFL and STOFF) in pretrigger ram.
1	0	Read flags from pretrigger ram and write flags to D1233 and/or to display memory (unit A4) via D1232.
0	1	Write flags in flag ram (D1252 and D1253). Connect DUDB14 and DUDB15 to two MSB's of average ram (D1251 pin 18 + 19)
1	1	Read flags from flag rams to D1233 and to display. Connect two MSB's of average ram to DUDB14 and DUDB15.

The circuit consisting of D1233 and the gates behind, generates an overflow flag for interpolated samples if one of the real samples has an overflow flag.

Note: the overflow flags are not used in this instrument, but they can be read by an option.

8.9.3 Example of DPU operation

The following example describes in a simplified way the calculation of 7 interpolated samples between 2 real samples.

It is supposed that:

- a sweep of real samples is placed in the pretrigger ram.
- the distance between 2 real samples is 8 address locations.
- the intermediate locations have to be filled with interpolated samples.
- none of the real samples has an overflow flag.

The next actions are taken by DPU:

1: copy a real sample from the pretrigger ram to register II and to the shift register.

2: copy the next real sample to register I.

3: enable the register II outputs and activate CO (complement); the inverted first sample is applied to the adder.

4: now the adder subtracts the first sample from the second sample.

5: clock the sample difference in register III.

6: copy the sample difference to register I.

7: in the meanwhile the shift register has shifted left three times, which means that the sample value is multiplied by 8.

8: add the shift register contents and the sample difference.

9: clock the result (interpolated sample x8) in register III.

10: copy the contents of register III in the shift register.

11: by the enabled register III the next interpolated sample x8 is offered to the inputs of this register via the adder and the sample difference in register I.

12: clock this next interpolated sample in register III.

13: the shift register shifts right three times; the result is an interpolated sample.

14: copy the result to the pretrigger ram.

15: repeat steps 10 to 14 another six times for the remaining calculations of interpolated samples.

NOTES: - For obtaining maximum accuracy, the sample difference is not divided by 8, but the sample values are multiplied by 8.
- The complex address generation for the pretrigger ram is done by the address generator on the DPU control.

8.9.4 Signal name list

UNIT A9

Signal name	Description	Signal source	Signal destination(s)
CKDUR1	Clock DPU register I	A8	-
CKDUR2LT	Clock DPU register II	A8	-
CKDUR3	Clock DPU register III	A8	-
CKF	Clock flags	A8	-
CKSR	Clock shift register	A9	A9
CO	Complement	A8	-
CSDURM	Chip select DPU ram	A8	-
CSF	Chip select flags	A9	A9
CYOT	Carry out	A9	A12-A8
DUABØØ...11	DPU address bus ØØ...11	A9	-
DUDBØØ...15	DPU databus ØØ...15	A9	A9
ENOFD	Enable overflow detection	A8	-
ENPM--LT	Enable pretrigger memory	A9	A9
FBRY	Feedback ready	A8	-
LEDP	Latch enable display	A8	-
OFAD	Overflow ADC	A11	-
OFDP	Overflow display	A9	A12-A4, A12-A8
OTDI2	Output disable DPU register II	A9	A9
OTDI3	Output disable DPU register III	A9	A9
OTDIAD	Output disable ADC	A8	-
OTDISR	Output disable shift register	A9	A9
OEDUØØ	Output enable DPU ØØ	A8	-
OEDUØ1	Output enable DPU Ø1	A8	-
OTENRSLT	Output enable reflection suppression	A9	A9
OTEN3-LT	Output enable DPU register III	A9	A9
OTLD	Output limit detection	A9	A12-A8
RDDURM	Read DPU ram	A8	-
RLDP	Real sample display	A9	A12-A4, A12-A8
RSDUR-LT	Reset DPU registers	A8	-
RSSR--LT	Reset shift register	A9	A9
SADBØØ...11	Sample data bus ØØ...11	A9+A11	A12-A4, A12-A5-A12-A25
SFSRØØ	Select function shift register ØØ	A8	-
SFSRØ1	Select function shift register Ø1	A8	-
SLAM	Select average memory	A8	-
SLOFAD	Select overflow ADC	A8	-
STOFF	Set overflow flag	A9	A9
STRLF	Set real sample flag	A8	-
UPCKØ8	Microprocessor clock 8 MHz	A6	-

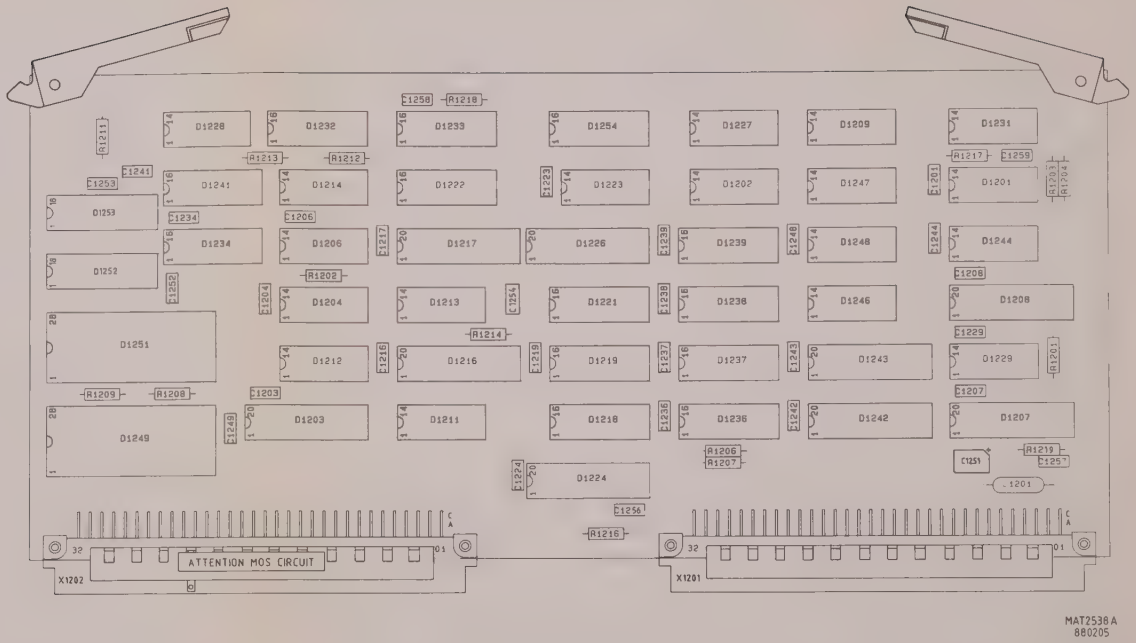


Figure 8.9.1 Unit A9 - DPU UNIT - p.c.b. lay-out.

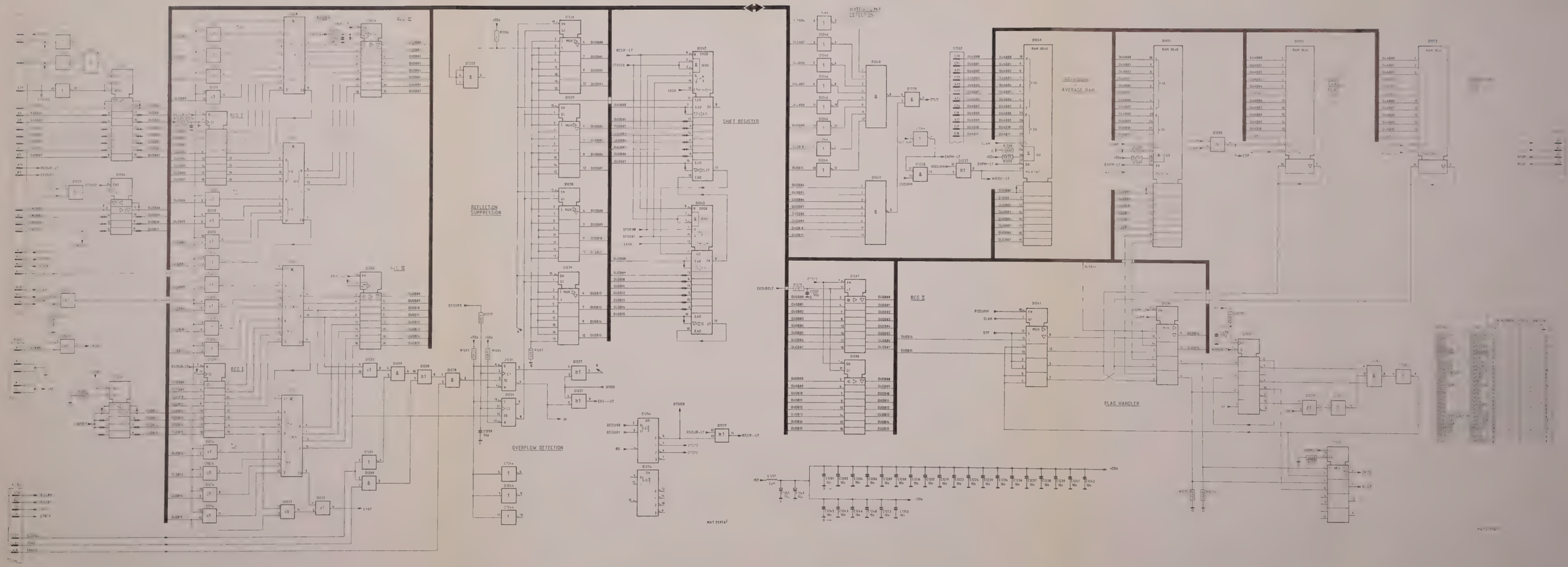
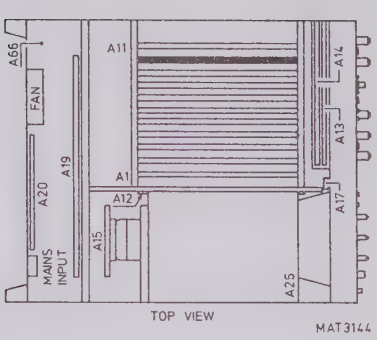


Figure 8.9.2 Unit A9 - DPU UNIT - circuit diagram.

UNIT A10 - OPTION 2



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8.10.1 General information

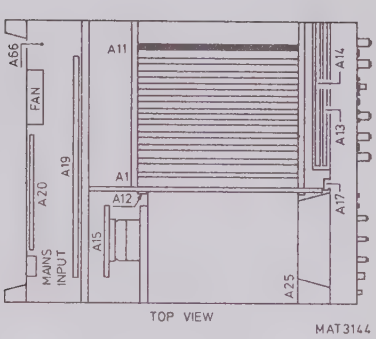
This OPTION 2 slot is reserved for an optional printed circuit board.

An optional printed circuit board in this slot is not available in standard instruments.

Another slot (OPTION 1) is also available in this instrument (see section 8.7.1).

NOTE: The first option to be installed in this instrument must always be placed in the OPTION 1 slot. The OPTION 2 slot may only be used if an option is installed already in the OPTION 1 slot.

UNIT A11 - ADC + T&H UNIT



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8.11.1 General information

The ADC and T&H unit accepts the samples from both input channels from the Vertical Signal unit A55 and converts these samples into 12 bits binary codes, which are routed to the DPU (unit A9) for further digital processing.

8.11.2 Circuit description

The samples from the Vertical Signal unit A55 are applied to the CORRECTION CIRCUIT.
Because jumper X608 is placed in position 2-3 in this instrument, the CORRECTION CIRCUIT operates as a linear amplifier. Potentiometer R721 has no function. The circuit controlled by transistor V622 is not active, due to the connection between the base and the emitter of V622.
The output signal at pin 15 of IC D616 is applied to a T&H gate (D613 and associated circuitry) via R707.

This T&H tracks the input signal continuously until the signal STCV-1 goes high. Now the output of D613 (pin 12) is held at the momentary value of the input signal.
Its output voltage goes via a buffer amplifier (V607, V608 and V609) to another buffer amplifier; N601 and associated components.
From this buffer amplifier the signal (THOTAN) goes to the ADC.
This buffer amplifier gives a feedback in the track mode (N601 pin 10) to the T&H gate. It is also a separation between the ADC and the T&H gate.

The signal THOTAN is applied to the ADC.
The ADC starts the conversion on the STAD--HT signal from the ADC logic. During this conversion the T&H gate is in the hold mode, to give the ADC a stable input signal.

The ADC output lines ADOT00...ADOT10 are led to the overflow detection circuit and to the sample data latch.
Line ADOT11 is buffered by D607. The three buffered lines ADOT11-1...ADOT11-3 are led to the overflow detection and the code converter.

The overflow detection detects whether all 11 ADC output signals are "0" (sample voltage too negative) or "1" (sample voltage too positive). The outputs (wired or) generate via D609 (pin 12 and 9) the OFAD signal to the DPU (unit A9) to indicate that an overflow occured during the conversion.

The code converter inverts ADOT11-3 (MSB) to convert the ADC output from straight binary code to two's complement code.
This two's complement code is latched by the sample data latch and afterwards applied to the DPU by the OTDIAD signal from the DPU.

The ADC logic generates the control signals from the UPCK16 signal. Figure 8.11.1 shows the timing diagram.

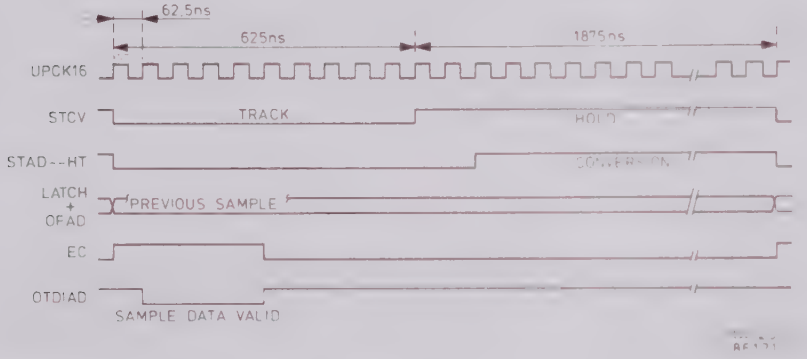


Figure 8.11.1 Timing diagram of the ADC and T&H unit.

8.11.3 Signal name list

UNIT A11

Signal name	Description	Signal source	Signal destination(s)
ADOTØØ...ADOT11	ADC out ØØ...11	A11	A11
ADOT11-1...11-3	ADC out 11-1...11-3	A11	A11
CDRSMO	(no function)	A8	-
EC	End of conversion	A11	A12-A8
	oscillator	A25	-
OFAD	Overflow ADC	A11	A12-A9
OTDIAD	Output disable ADC	A8	-
SADBØØ...11	Sample data bus ØØ...11	A11	A12-A9
STAD--HT	Start ADC	A11	A11
STAD--LT	Start ADC	A11	A11
STCV	Start conversion	A5	-
THINAN	Track & Hold in analogue	A55	-
THOTAN	Track & Hold out analogue	A11	A11
UPCK16	Microprocessor clock 16 MHz	A6	-

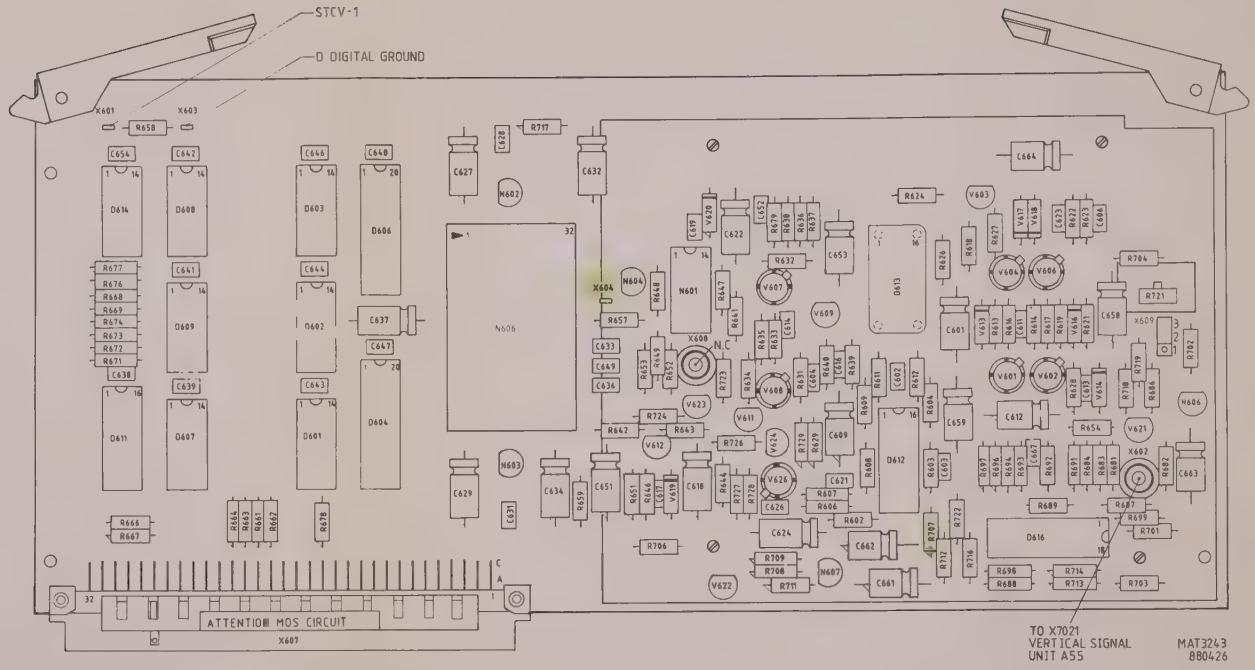


Figure 8.11.2 Unit A11 - ADC + T&H UNIT - p.c.b. lay-out.

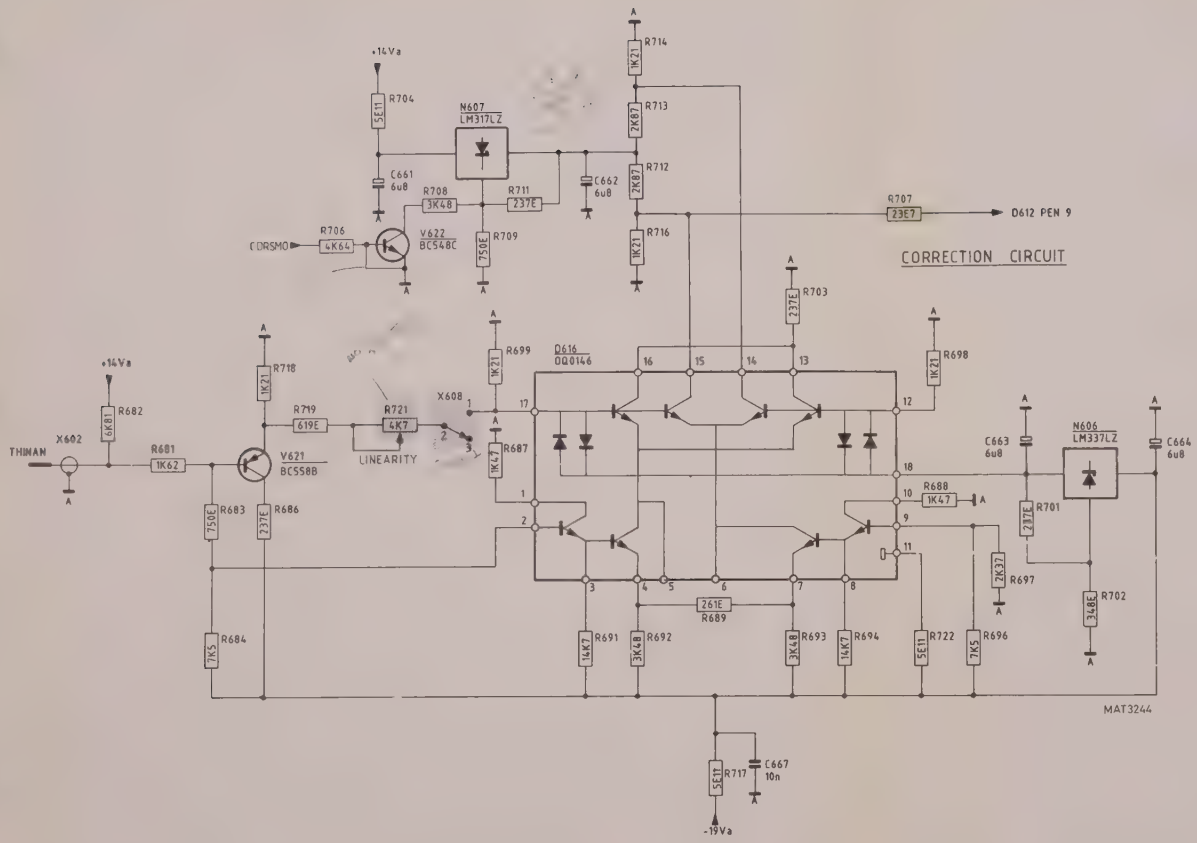


Figure 8.11.3 Unit A11 - ADC + T&H UNIT - circuit diagram.

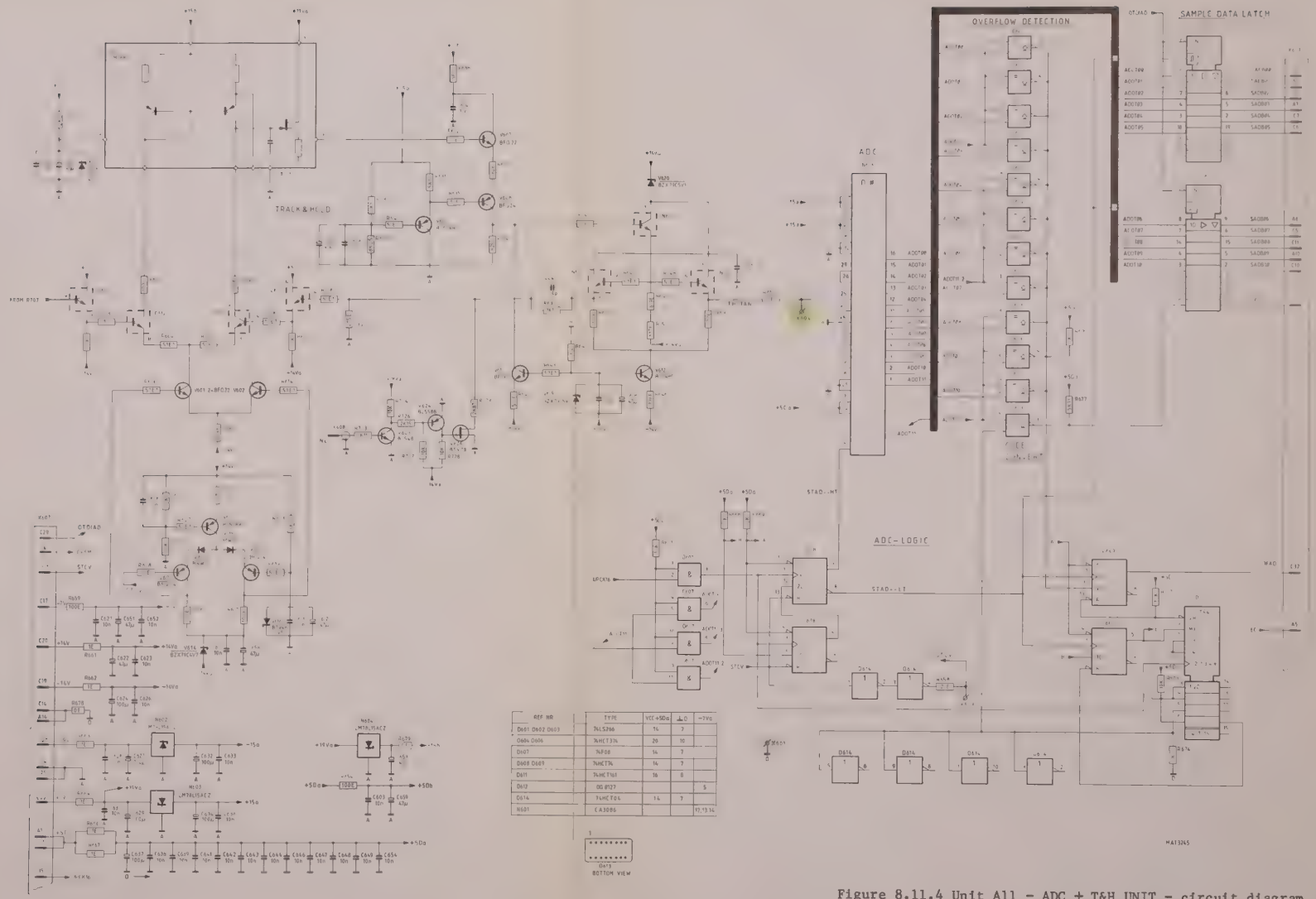
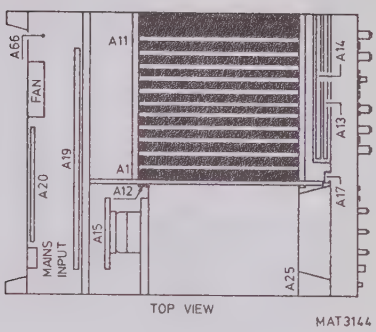


Figure 8.11.4 Unit A11 - ADC + T&H UNIT - circuit diagram.

UNIT A12 - MOTHERBOARD



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8.12.1 General information

The function of the motherboard unit is to interconnect the various plug-in units with each other as well as with the rest of the system.

8.12.2 Detailed information

No active components are mounted on this board.

Each plug-in unit is provided with one or two (three row) 96-pole EURO-connectors. One connector is used for the primary or CCU (Central Control Unit) - bus. The other connector is used for the so-called secundary - bus.

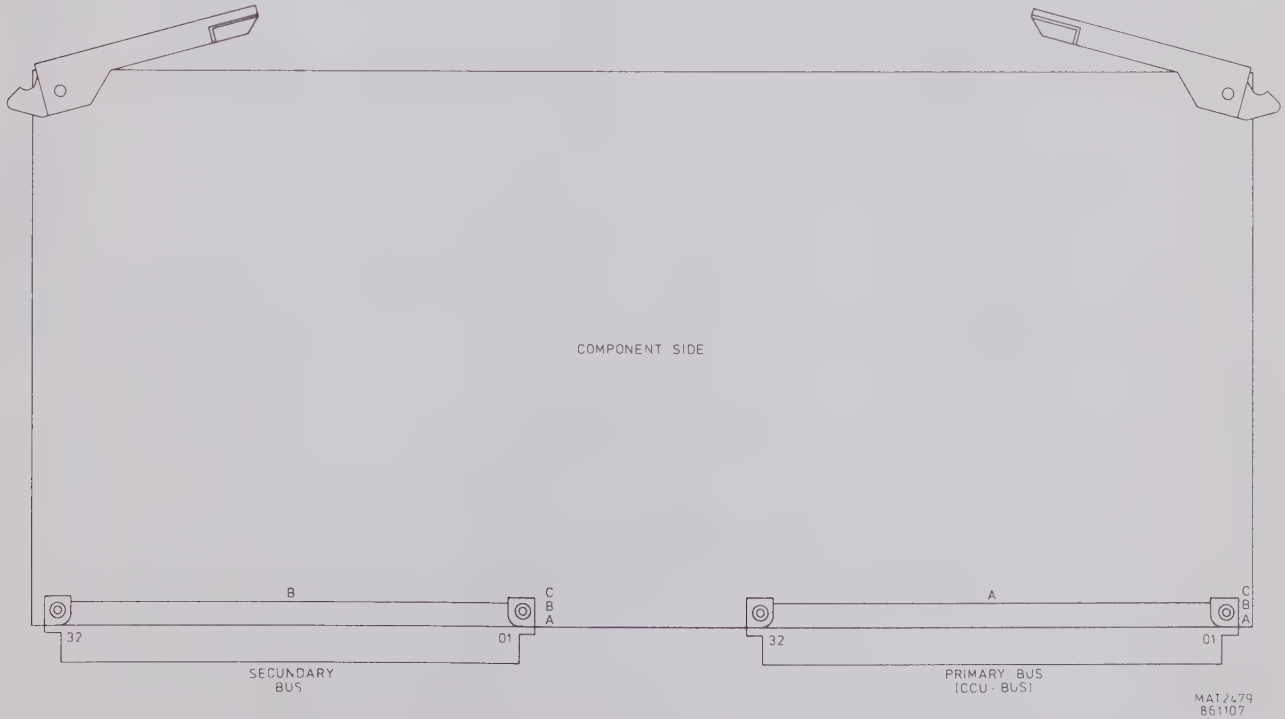


Figure 8.12.1 EURO-connectors.

8.12.3 Primary bus (CCU-bus)

This is a description of the pin lay out for the connectors of the CCU-bus on the motherboard.

```
MOTHERBOARD A12 -----> UNIT
X504 ----------------> A2 - X2301
X507 ----------------> A3 - X2101
X509 ----------------> A4 - X2002
X512 ----------------> A5 - X1801
X513 ----------------> A6 - X1701
X516 ----------------> A7 - X701
X518 ----------------> A8 - X1401
X521 ----------------> A9 - X1201
X523 ----------------> A10- X....
```

ROW A			ROW B			ROW C	
1	+5 D		1	+5 D		1	+5 D	
2	UPCKØ8		2	D		2	UPCK16	
3	D		3	D		3	D	
4	-		4	MYSLØ1LT	* R506/2	4	-	
5	MYSLDWLT		5	MYSLØ2LT	* R506/3	5	-	
6	VBB		6	MYSLØ3LT	* R506/4	6	-	
7	BAVO		7	MYSLØ4LT	* R506/5	7	UPRSOTLT	
8	ABØ1	* R502/2	8	ABØ8	* R506/6	8	DATRAKLT	
9	ABØ2	* R502/3	9	ABØ9	* R506/7	9	DALOSBLT	* R508/2
10	ABØ3	* R502/4	10	AB1Ø	* R506/8	10	DBØØ	* R508/3
11	ABØ4	* R502/5	11	AB11	* R506/9	11	DBØ1	* R508/4
12	ABØ5	* R503/2	12	AB12	* R502/6	12	DBØ2	* R508/5
13	ABØ6	* R503/4	13	AB13	* R503/3	13	DBØ3	* R508/6
14	ABØ7	* R502/7	14	AB14	* R502/8	14	DBØ4	* R508/7
15	IOSLØ3LT	* R503/5	15	AB15	* R502/9	15	DBØ5	* R508/8
16	IOSLØ4LT	* R501/2	16	AB16	* R503/9	16	DBØ6	* R508/9
17	IOSLØ5LT	* R501/4	17	AB17	* R501/3	17	DBØ7	* R503/6
18	IOSLØ6LT	* R504/3	18	AB18	* R504/2	18	DBØ8	* R503/7
19	IOSLØ7LT	* R504/4	19	AB19	* R501/5	19	DBØ9	* R503/8
20	IOSLØ8LT	* R504/6	20	AB2Ø	* R504/5	20	DB1Ø	* R507/2
21	IOSLØ9LT	* R501/6	21	AB21	* R504/7	21	DB11	* R507/3
22	IOSL1ØLT	* R501/7	22	-	* R504/8	22	DB12	* R507/4
23	ILØ1--LT		23	-		23	DB13	* R507/5
24	ILØ2--LT		24	-		24	DB14	* R507/6
25	ILØ3--LT		25	-		25	DB15	* R507/7
26	ILØ4--LT		26	-	* R504/9	26	DAHISBLT	* R507/8
27	ILØ5--LT		27	-	* R501/8	27	UPRD--LT	* R507/9
28	ILØ6--LT		28	WD----LT		28	UPWR--LT	* R501/9
29	ILØ7--LT		29	-		29	Z-MO--XT	
30	A		30	A		30	A	
31	-7 V		31	-7 V		31	-7 V	
32	+7 V		32	+7 V		32	+7 V	

* TERMINATED WITH R.../PINNUMBER

8.12.4 Description of the CCU-bus signals

a1, b1 and c1	: 5 V digital
a3, b2, b3 and c3	: Ground of the digital 5 V
a30, b30 and c30	: Analog earth
a31, b31 and c31	: Analog -7 V
a32, b32 and c32	: Analog 7 V
a2	: 8MHz processor clock
a5	: Memory select down. This line indicates that the chip select of the RAM´s must be disabled on battery back up.
a6	: Voltage for the battery back up RAM´s
a7	: Battery voltage
a8 ... a14	: Lowest 7 address lines
a15 ... a22	: I/O select lines for the selection of the input/output ports
a23 ... a29	: Interrupt level lines. The sequence is as follows: ILØ1--LT --> 40 ms interrupt ILØ2--LT --> DPU interrupt ILØ3--LT --> rotary interrupt ILØ4--LT --> option interrupt ILØ5--LT --> display interrupt ILØ6--LT --> not used ILØ7--LT --> power down interrupt (increasing priority ↓)
b4	: Memory select for the microprocessor RAM
b5	: Memory select for the display memory
b6	: Memory select for the DPU programm memory
b7	: Memory select for the options
b8 ... b21	: Address lines 8 ... 21
b22	: Not used
b23	: Not used
b24	: Not used
b26	: Not used
b27	: Not used
b28	: Watch dog trigger line. Masters can trigger the watchdog via this line.
c2	: 16 MHz clock from the microprocessor unit.
c7	: Microprocessor reset output.
c8	: Data transfer acknowledge. This is an open collector line on which units, which are addressed via MYSLØ1 ... MYSLØ4, can indicate that the data on the data bus is accepted or stable.
C9	: Data lower strobe. With this line active, the lowest 8 data bus lines can be used for read or write actions.
c10 ... c25	: Databus
c27	: Data higher strobe. With this line active, the highest 8 data bus lines can be used for read or write actions.
c28	: Microprocessor read.
c29	: Microprocessor write.
c30	: Z modulation frequency of 200 kHz.

8.12.5 Secundary bus

MOTHERBOARD A12 ---> UNIT A1
X502 ----------> X2501

ROW A		ROW B	ROW C	
1	-	1	1	Z-MO--XT
2	-	2	2	ANCPY-HT
3	-	3	3	ANEPY-HT
4	-	4	4	DPTR--HT
5	-	5	5	DIOS--HT
6	+5D	6	6	Z-BL--HT
7	-	7	7	A
8	-7V	8	8	VREPX2
9	-	9	9	VREPX1
10	+7V	10	10	A
11	A	11	11	X2IN
12	100V	12	12	X1IN
13	A	13	13	A
14	40V	14	14	Y2IN
15	A	15	15	Y1IN
16	+19V	16	16	A
17	A	17	17	-
18	-19V	18	18	-
19	A	19	19	-
20	+14V	20	20	-
21	A	21	21	-
22	-14V	22	22	-
23	-	23	23	-
24	-	24	24	-
25	-	25	25	A
26	-	26	26	A
27	-	27	27	-
28	-	28	28	-
29	-	29	29	SAPL
30	-	30	30	PLZEOT
31	-	31	31	PFPY
32	-	32	32	PU----LT

MOTHERBOARD A12 ---> UNIT A2
X503 ----------> X2302

	ROW A	ROW B	ROW C
1	LEDA--HT	1	LEDA--LT
2	WRHOPOLT	2	VEDBØ9
3	WRVEPOLT	3	VEDB1Ø
4	-	4	VEDB11
5	DPTR--HT	5	VEDB12
6	DIOS--HT	6	EPY-ØØ
7	ENTRHOLT	7	EPY-Ø1
8	EPX-ØØ	8	IVDCDB
9	EPX-Ø1	9	ENTXLNLT
10	DCDBØ2	10	EPDBØØ
11	DCDBØØ	11	EPDBØ1
12	DCDBØ5	12	EPDBØ2
13	DCDBØ4	13	EPDBØ3
14	DCDBØ3	14	EPDBØ4
15	DCDBØ7	15	EPDBØ5
16	DCDBØ1	16	EPDBØ6
17	DCDBØ8	17	EPDBØ7
18	EP12--LT	18	EPDBØ8
19	EPHO14	19	EPDBØ9
20	VREPX2	20	EPDB1Ø
21	VREPX1	21	EPDB11
22	EPX-Ø2	22	CKEPVE
23	-	23	DCDBØ9
24	Z-OTØ3	24	DPRJ
25	DCDBØ6	25	-
26	X2IN	26	WRHOVRLT
27	X1IN	27	DJAC--HT
28	Y2IN	28	DPRJDW
29	Y1IN	29	SM----LT
30	-7 V	30	+7 V
31	-14 V	31	+14 V
32	-19 V	32	A

MOTHERBOARD A12 ---> UNIT A3
X506 ----------> X2102

ROW	A	ROW	B	ROW	C
1	OETX--LT	1	CSTX--LT	1	WETX--LT
2	RDDM--LT	2	DITXTR	2	DAAK--LT
3	LEDA--HT	3	DRTXTR	3	DPAB11
4	LEDA--LT	4	DPABØ9	4	TXAB13
5	VEDBØ9	5	WRHOPOLT	5	DAPBØ8
6	VEDB1Ø	6	WRVEPOLT	6	DPAB1Ø
7	VEDB11	7	ANCPY-HT	7	OETRØ2LT
8	VEDB12	8	ANEPY-HT	8	WETRØ2LT
9	EPY-ØØ	9	DPTR--HT	9	DPABØØ
10	EPY-Ø1	10	DIOS--HT	10	DPABØ3
11	1VDCDB	11	ENTRHOLT	11	DPABØ2
12	ENTXLNLT	12	EPXØØ	12	DPABØ1
13	EPDBØØ	13	EPXØ1	13	CLUPAB
14	EPDBØ1	14	Z-BL-HT	14	DPABØ7
15	EPDBØ2	15	DPABØ5	15	DPABØ6
16	EPDBØ3	16	DAAK--HT	16	DPABØ4
17	EPDBØ4	17	WETRØ1LT	17	CPABØØ n.u.
18	EPDBØ5	18	OETRØ1LT	18	MXCPAD
19	EPDBØ6	19	TRAB13	19	CKSVLA
20	EPDBØ7	20	DIDBTX	20	CLDPAB
21	EPDBØ8	21	DISVLA	21	LEDC
22	EPDBØ9	22	EP12--LT	22	DCDB15
23	EPDB1Ø	23	EPHO14	23	SARYAKLT
24	EPDB11	24	EPX-Ø2	24	DCDB14
25	CKEPVE	25	DCDB11	25	DCDB13
26	DCDBØ9	26	-	26	DCDB12
27	DPRJUPLT	27	Z-OTØ3	27	SARY
28	-	28	WRHOVRLT	28	DCDB1Ø
29	DJAC--HT	29	DPRJDWLT	29	SLTR2LLT
30	SM----LT	30	SLTR1HLT	30	SLTR2HLT
31	SAPL	31	PLZEOT	31	SLTR1LLT
32	PFPY	32	PU----LT	32	SYDP

MOTHERBOARD A12 ---> UNIT A4
X508 ----------> X2001

ROW	A	ROW	B	ROW	C
1	WETX--LT	1	CSTX--LT	1	OETX--LT
2	DAAK--LT	2	DITXTR	2	RDDM--LT
3	DPAB11	3	DRTXTR	3	TXAB13
4	DPABØ8	4	DPABØ9	4	DPAB1Ø
5	OETRØ2LT	5	WETRØ2LT	5	SADBØ7
6	SADBØ6	6	DPABØ3	6	SADBØ5
7	SADBØ3	7	DPABØ2	7	SADBØ4
8	SADBØ1	8	DPABØ1	8	SADBØ
9	DPABØØ	9	CLUPAB	9	SADBØØ
10	SADBØ9	10	DPABØ7	10	OFDP
11	DPABØ6	11	DPABØ5	11	SADBØ8
12	DPABØ4	12	DAAK--HT	12	TCCPCN
13	CPABØØ n.u.	13	WETRØ1LT	13	OETRØ1LT
14	MXCPAD	14	TRAB13	14	RLDP
15	RSDU--LT	15	CKSVLA	15	CNCPCN
16	DIDBTX	16	CLDPAB	16	DUABØ8
17	DUABØ9	17	DISVLA	17	DUAB11
18	DCDBØØ	18	DCDBØ2	18	DUAB1Ø
19	DCDBØ4	19	DCDBØ5	19	LEDC
20	DCDBØ7	20	DCDBØ3	20	DUABØØ
21	DCDBØ1	21	DUABØ2	21	DUABØ1
22	DCDBØ8	22	DUABØ4	22	DUABØ3
23	DUABØ6	23	SADB13	23	DUABØ5
24	SADB12	24	SADB15	24	DUABØ7
25	SADB14	25	SARYAKLT	25	DCDB15
26	DCDB13	26	DCDB14	26	DCDBØ9
27	DCDB11	27	DCDBØ6	27	DCDB12
28	DCDB1Ø	28	SARY	28	ENCPSA
29	SLTR2LLT	29	OTCM	29	DAVA
30	SLTR2HLT	30	SLTR1HLT	30	DIDCLA n.u.
31	-	31	SLTR1LLT	31	LEDP
32	-	32	-	32	-

MOTHERBOARD A12 ---> UNIT A5
X511 ----------> X1802

ROW	A	ROW	B	ROW	C
1	SADBØ7	1		1	SADBØ5
2	SADBØ4	2		2	SADBØ6
3	SADBØ8	3		3	SECK1
4	TKSA	4		4	SADB11
5	-	5		5	SADBØ7
6	SADBØ6	6		6	SADBØ5
7	SADBØ3	7		7	SADBØ4
8	SADBØ1	8		8	SADBØ2
9	OFDP	9		9	SADBØØ
10	SADBØ9	10		10	SADB1Ø
11	SADBØ8	11		11	-
12	SADBØ3	12		12	CHPT
13	SADBØ9	13		13	SADB11
14	RLDP	14		14	UPRSOTLT
15	SADBØ2	15		15	STCV
16	SADB1Ø	16		16	LEACL
17	SADBØ1	17		17	SEDA1
18	-	18		18	STSAGTLT
19	SADBØØ	19		19	-
20	FBRY	20		20	SHIELD
21	-	21		21	TRRY
22	CHSW	22		22	CNSTCNLT
23	CHPT	23		23	-
24	ILØ2--LT	24		24	RSSTCNLT
25	-	25		25	-
26	-	26		26	-
27	-14V	27		27	D
28	A	28		28	-
29	+14V	29		29	DAVA
30	+19V	30		30	-
31	A	31		31	LEDP
32	-19V	32		32	FBRY

MOTHERBOARD A12 ---> UNIT A7
X514 ----------> X....

ROW A		ROW B		ROW C	
1	TKSA	1		1	TKSA
2	-	2		2	-
3	SADBØ6	3		3	SADBØ6
4	-	4		4	-
5	-	5		5	-
6	-	6		6	-
7	-	7		7	-
8	-	8		8	-
9	-	9		9	-
10	-	10		10	-
11	MMPT	11		11	MMPT
12	-	12		12	-
13	TCCPCN	13		13	TCCPCN
14	-	14		14	-
15	CNCPCN	15		15	CNCPCN
16	RSDU--LT	16		16	RSDU--LT
17	-	17		17	-
18	-	18		18	-
19	-	19		19	-
20	-	20		20	-
21	TRRY	21		21	TRRY
22	-	22		22	-
23	-	23		23	-
24	-	24		24	-
25	-	25		25	-
26	D	26		26	-
27	D	27		27	-
28	-	28		28	-
29	-19 V	29		29	+19 V
30	-	30		30	-
31	LEDP	31		31	LEDP
32	-	32		32	A

MOTHERBOARD A12 ---> UNIT A8
X517 ----------> X1402

ROW	A	ROW	B	ROW	C
1	TKSA	1		1	-
2	-	2		2	EC
3	-	3		3	CKDUR1
4	-	4		4	CDRSMO
5	-	5		5	-
6	-	6		6	-
7	-	7		7	-
8	-	8		8	-
9	OFDP	9		9	-
10	-	10		10	-
11	MMPT	11		11	SFSRØ1
12	CHPT	12		12	SFSRØØ
13	TCCPCN	13		13	CO
14	RLDP	14		14	OTLD
15	CNCPCN	15		15	STRLF
16	RSDU--LT	16		16	DUABØ8
17	DUABØ9	17		17	DUAB11
18	ENOFD	18		18	DUAB1Ø
19	-	19		19	RSDUR-LT
20	TRRY	20		20	DUABØØ
21	DUABØ2	21		21	DUABØ1
22	DUABØ4	22		22	DUABØ3
23	DUABØ6	23		23	DUABØ5
24	CYOT	24		24	DUABØ7
25	LEDUR2	25		25	CKF
26	CKDUR3	26		26	RDDURM
27	CSDURM	27		27	SLOFAD
28	SLAM	28		28	ENCPSA
29	OEDUØØ	29		29	OTDIAD
30	OTCM	30		30	DAVA
31	OEDUØ1	31		31	LEDP
32	SYDP	32		32	FBRY

MOTHERBOARD A12 ---> UNIT A9
X519 ----------> X1202

ROW	A	ROW	B	ROW	C
1	-	1		1	-
2	-	2		2	-
3	-	3		3	-
4	-	4		4	-
5	CKDUR1	5		5	SADBØ7
6	SADBØ6	6		6	SADBØ5
7	SADBØ3	7		7	SADBØ4
8	SADBØ1	8		8	SADBØ2
9	OFDP	9		9	SADBØØ
10	SADBØ9	10		10	SADB1Ø
11	SFSRØ1	11		11	SADBØ8
12	SFSRØØ	12		12	-
13	CO	13		13	SADB11
14	OTLD	14		14	RLDP
15	-	15		15	STRLF
16	-	16		16	DUABØ8
17	DUABØ9	17		17	DUAB11
18	ENOFD	18		18	DUAB1Ø
19	RSDUR-LT	19		19	-
20	-	20		20	DUABØØ
21	DUABØ2	21		21	DUABØ1
22	DUABØ4	22		22	DUABØ3
23	DUABØ6	23		23	DUABØ5
24	CYOT	24		24	DUABØ7
25	CKDUR2LT	25		25	CFK
26	CKDUR3	26		26	RDDURM
27	CSDURM	27		27	SLOFAD
28	SLAM	28		28	-
29	OEDUØØ	29		29	OTDIAD
30	-	30		30	-
31	OEDUØ1	31		31	LEDP
32	FBRY	32		32	OFAD

MOTHERBOARD A12 ---> UNIT A10
X522 ----------> X....

ROW A		ROW B		ROW C	
1	-	1		1	-
2	-	2		2	-
3	-	3		3	-
4	-	4		4	-
5	EC	5		5	SADBØ7
6	SADBØ6	6		6	SADBØ5
7	SADBØ3	7		7	SADBØ4
8	SADBØ1	8		8	SADBØ2
9	OFDP	9		9	SADBØØ
10	SADBØ9	10		10	SADB1Ø
11	-	11		11	-
12	-	12		12	-
13	-	13		13	SADB11
14	RLDP	14		14	D
15	-	15		15	-
16	-	16		16	D
17	-	17		17	-
18	-	18		18	-
19	-	19		19	-
20	-	20		20	-
21	-	21		21	-
22	-	22		22	-
23	-	23		23	-
24	-	24		24	-
25	+7 V	25		25	-
26	-7 V	26		26	-
27	-14 V	27		27	-
28	A	28		28	CKADOT
29	+14 V	29		29	OTDIAD
30	+19 V	30		30	LEDP
31	A	31		31	FBRY
32	-19 V	32		32	OFAD

MOTHERBOARD A12 ---> UNIT A11
X524 ----------> X607

ROW A		ROW B		ROW C	
1	-	1		1	-
2	-	2		2	-
3	-	3		3	-
4	-	4		4	CDRSMO
5	EC	5		5	SADBØ7
6	SADBØ6	6		6	SADBØ5
7	SADBØ3	7		7	SADBØ4
8	SADBØ1	8		8	SADBØ2
9	-	9		9	SADBØØ
10	SADBØ9	10		10	SADB1Ø
11	-	11		11	SADBØ8
12	-	12		12	-
13	STCV	13		13	SADB11
14	D	14		14	D
15	-	15		15	UPCK16
16	+5D	16		16	+5D
17	-	17		17	-7 V
18	-	18		18	-
19	-	19		19	-14 V
20	-	20		20	+14 V
21	-	21		21	-19 V
22	-	22		22	+19 V
23	-	23		23	-
24	-	24		24	A
25	-	25		25	A
26	-	26		26	-
27	-	27		27	-
28	-	28		28	-
29	-	29		29	OTDIAD
30	-	30		30	-
31	-	31		31	-
32	-	32		32	OFAD

8.12.6 Additional connections

MOTHERBOARD A12 ---> UNIT A14
X526 --> (CABLE)---> X4001

1	ABØ1
2	+5 D
3	ABØ2
4	DBØØ
5	ABØ3
6	DBØ1
7	ABØ4
8	DBØ2
9	DBØ3
10	DBØ4
11	DBØ5
12	DBØ6
13	IOSLØ4LT
14	DBØ7
15	ILØ3--LT
16	UPRD--LT
17	UPWR--LT
18	D
19	D
20	-7 V

MOTHERBOARD A12 ---> UNIT A19
X527 -->(CABLE) ---> X4406

1	A
2	A
3	-5 D
4	BAVO
5	CON
6	+100 V
7	+7 V
8	+7 V
9	-7 V
10	-7 V
11	-14 V
12	-14 V
13	+14 V
14	+14 V
15	-19 V
16	-19 V
17	+19 V
18	+19 V
19	+40 V
20	+40 V

MOTHERBOARD A12 ---> UNIT A25
X501 --> (CABLE)---> X2502

ROW	A	ROW	B	ROW	C
1	-	1	-	1	
2	CHSW	2	CHPT	2	
3	FBRY	3	-	3	
4	-	4	SADBØØ	4	
5	SADB1Ø	5	SADBØ1	5	
6	SADBØ9	6	SADBØ2	6	
7	SADBØ8	7	SADBØ3	7	
8	SADBØ7	8	SADBØ4	8	
9	SADBØ6	9	SADBØ5	9	
10	SADB11	10	SECK1	10	
11	-	11	UPRSOTLT	11	
12	SEDA1	12	LEACL	12	
13	-	13	STSAGTLT	13	
14	CNSTCNLT	14	-	14	
15	RSSTCNLT	15	-	15	
16	-	16	-	16	
17	UPWR--LT	17	-	17	
18	DB15 * R507/7	18	UPRD--LT	18	
19	DB13 * R507/5	19	DB14 * R507/6	19	
20	DB11 * R507/3	20	DB12 * R507/4	20	
21	IOSLØ7LT	21	DB1Ø* R507/2	21	
22	IOSLØ6LT	22	DBØ9* R503/8	22	
23	DBØ7* R503/6	23	DBØ8* R503/7	23	
24	DBØ5* R508/7	24	DBØ6* R508/9	24	
25	DBØ3* R508/6	25	DBØ4* R508/7	25	
26	DBØ2* R508/5	26	ABØ5* -	26	
27	DBØ1* R508/4	27	ABØ4* R502/5	27	
28	DBØØ* R508/3	28	ABØ3* R502/4	28	
29	ABØ1* R502/2	29	ABØ2* R503/3	29	
30	D	30	D	30	
31	+5 D	31	D	31	
32	+5 D	32	+5 D	32	

* TERMINATED WITH R.../PINNUMBER

NOTE: The flatcable has crossed interconnections.
This means that connector pin A1 on one end becomes B32 on the other end, etc.

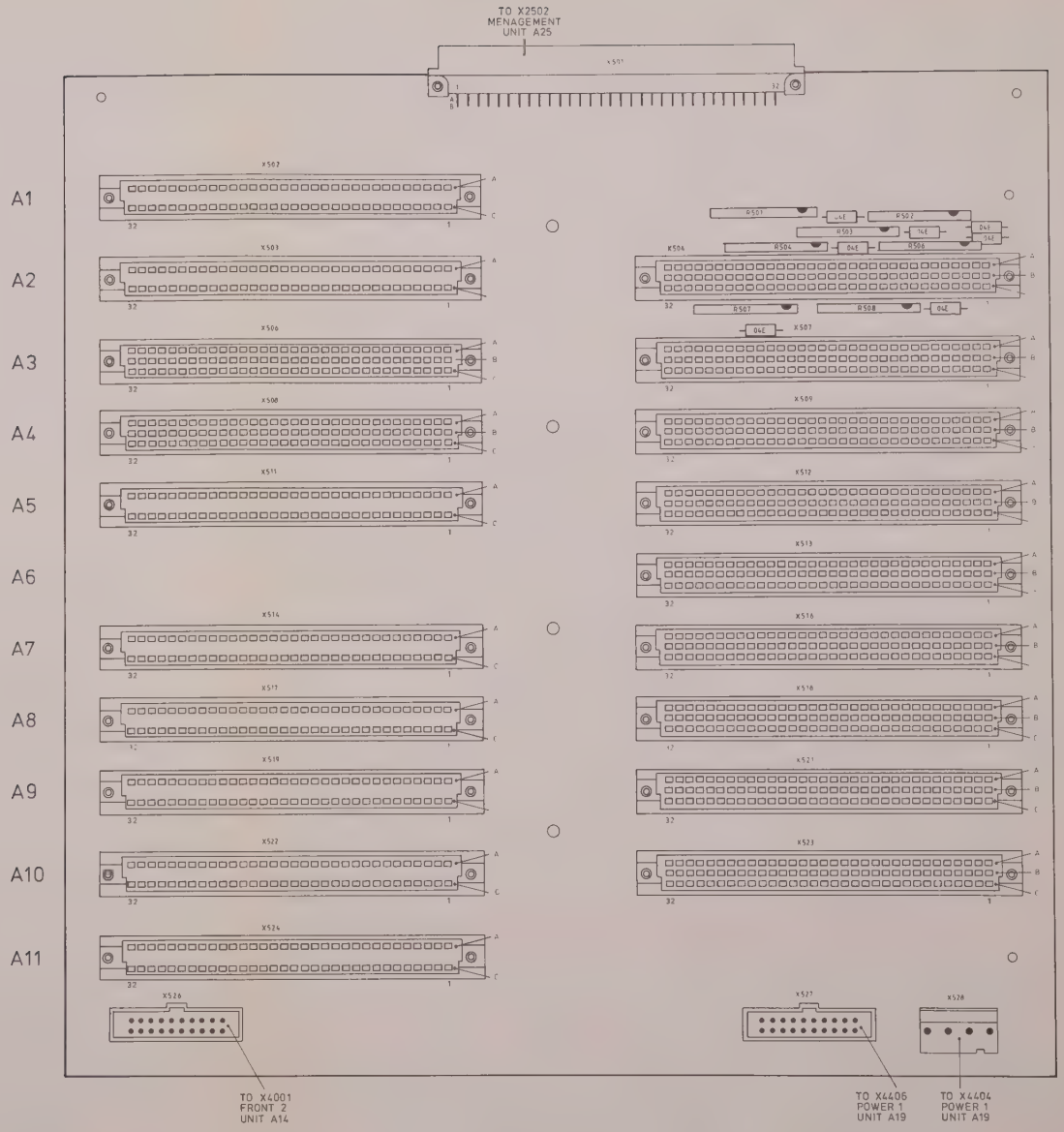


Figure 8.12.2 Unit A12 - MOTHERBOARD - p.c.b. lay-out.

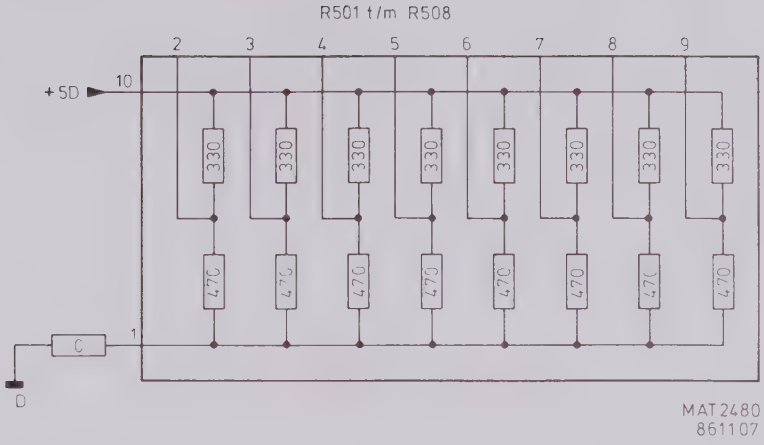
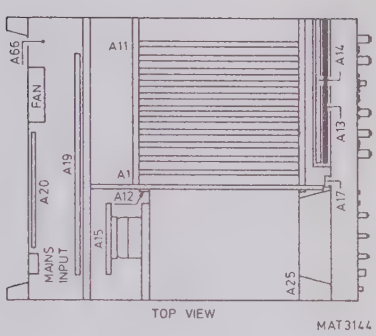


Figure 8.12.3 Unit A12 - MOTHERBOARD - circuit diagram.

UNIT A13 - FRONT 1



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8.13.1 General information

This front unit contains the front-panel pilot lamps, front-switches and front-switches with built-in pilot lamps.

8.13.2 Pilot lamps

The front panel pilot lamps are controlled by the microprocessor via the data bus lines DBØØ ... DBØ7 and latches D4206 and D4207.
Each latch can be activated by an output signal from the decoder D4204. This decoder decodes the three microprocessor address bits ABØ1, ABØ2 and ABØ3 and is enabled by the signals ABØ4, UPWR--LT and IOSLØ4LT.
This is done when the microprocessor generates the front unit addresses and the UPWR--LT signals for the control of the pilot lamps.
Latch D4206 controls the pilot lamps DOTS, AVERAGE C=4, NEGATIVE SLOPE, TRIGGER, SYNCHRONIZE and COUNT DOWN.
Latch D4207 controls the pilot lamps UNCAL A, UNCAL B, REMOTE, X-EXPAND UNCAL, LOCK and WRITE.

8.13.3 Front-switches

The settings of all the front-switches are periodically read by the microprocessor system.
The front-switches are therefore placed in a matrix structure.
Eight switches at a time can offer their settings to the inputs of data buffer D4203.
Each row of eight switches can be activated by one of the output signals CNØØ ... CNØ6 from the address decoder D4201. These signals are on a -0,7 V level because of the -0,7 V level on input 3 of D4201. In this way the 0,7 V accross the diodes is compensated and the signals RWØØ ... RWØ7 are brought on a 0 V level.
This decoder decodes the three microprocessor address bits ABØ1, ABØ2 and ABØ3 and is enabled by the signal combination ABØ4, UPRD--LT and IOSLØ4LT.
This combination resulting in signal ENFTSWLT is generated when the microprocessor generates the front unit addresses and the UPRD--LT signals for the reading of the soft-switch settings.
When signal ENFTSWLT is active, front switch buffer D4203 will place the matrix data RWØØ ... RWØ7 on the data bus lines DBØØ ... DBØ7.
The matrix is scanned by the microprocessor, every 40ms.

8.13.4 Address decoding table

The addresses which are generated by the microprocessor are decoded by address decoders D4204 and D4201 according to the following table.

IOSLØ4LT	ABØ4	ABØ3	ABØ2	ABØ1	Function WR	RD
0	0	0	0	0	Leds (4206)	CNØØ
0	0	0	0	1	Leds (4207)	CNØ1
0	0	0	1	0		CNØ2
0	0	0	1	1		CNØ3
0	0	1	0	0		CNØ4
0	0	1	0	1		CNØ5
0	0	1	1	0		CNØ6

8.13.5 Signal name list

UNIT A13

Signal name	Description	Signal source	Signal destination(s)
ABØ1...Ø4	Address bus	A6+Option	-
CNØØ...Ø6	Count ØØ...Ø6	A13	A13
COMMON1	Common line 1	A13	A18
COMMON2	Common line 2	A13	A17
DBØØ...Ø7	Data bus ØØ...Ø7	A6+Option	-
ENFTSWLT	Enter front switch	A13	A13
IOSLØ4LT	I/O select Ø4	A6	-
RWØ...Ø7	Row ØØ...Ø7	A13	A13
UPRD--LT	Microprocessor read	A6	-
UPWR--LT	Microprocessor write	A6	-

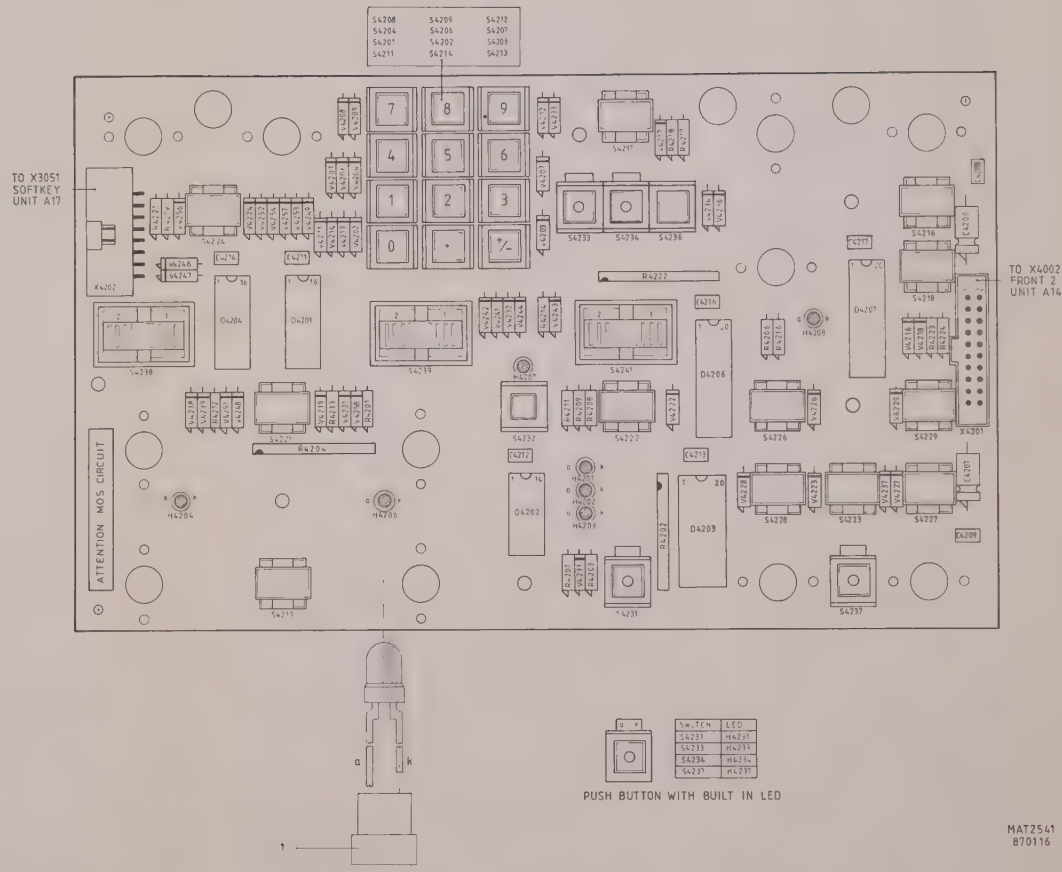


Figure 8.13.1 Unit A13 - FRONT 1 - p.c.b. lay-out.

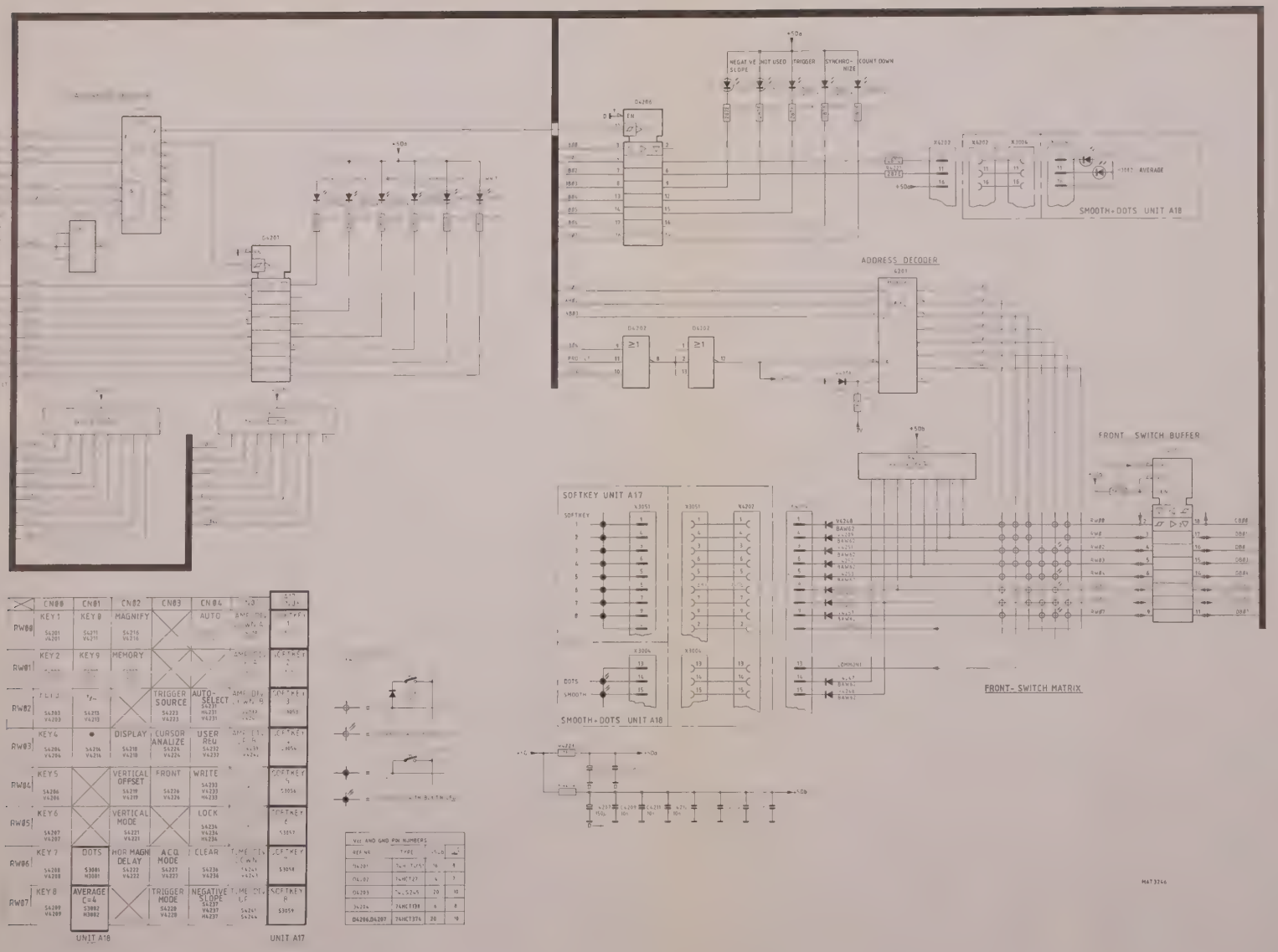
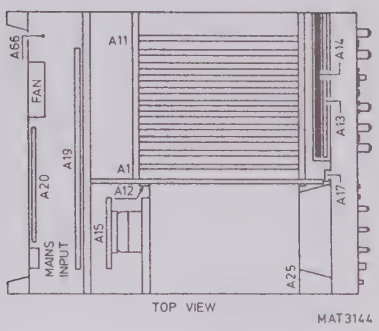


Figure 8.13.2 Unit A13 - FRONT 1 - circuit diagram.

UNIT A14 - FRONT 2



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8.14.1 General information

This front unit contains all the front-panel optical switches and their photo-sensitive transistors.
There are eleven identical optical switches for the following functions:

- X-POSITION
- X-EXPAND
- VARIABLE-B
- Y-POSITION
- OFFSET-A
- VARIABLE-A
- OFFSET-B
- 1st CURSOR
- 2nd CURSOR
- LEVEL
- HOLD OFF/SYNC

8.14.2 Optical switches

The rotation of an optical switch is detected by the two internal photo-transistors. If the control is turned from one position to another, light from the infra-red LED´s falls in the photo-transistors, pulsed via the holes in a perforated disc. As a result, the photo-transistors conduct for some time and their collectors are low.

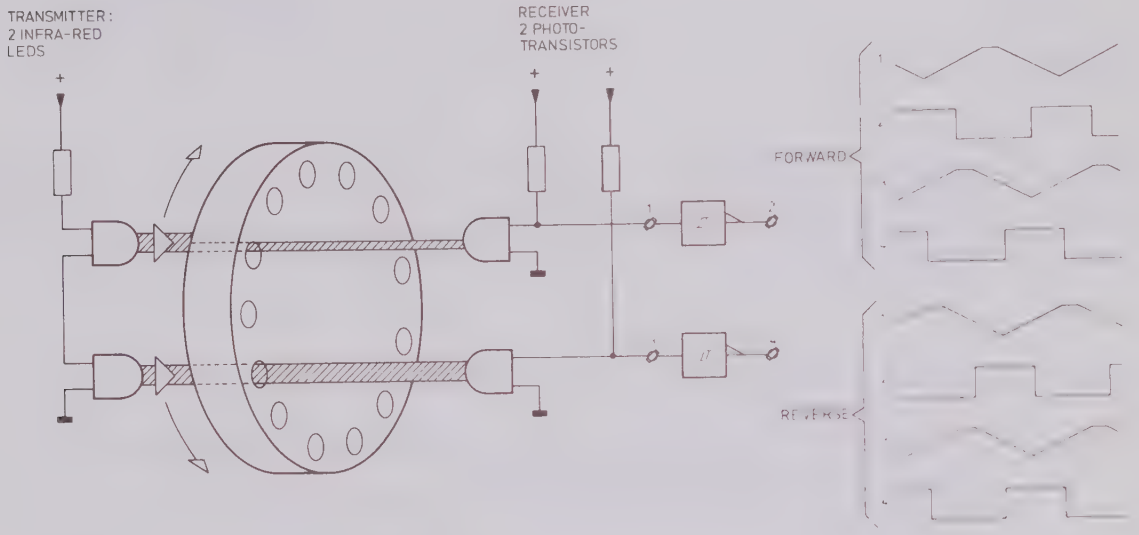


Figure 8.14.1 Optical switches

The collector signals of the photo-transistors are applied to three 3-state registers D4012, D4011, and D4009 as rotate forward signals RTFWØ1 ... RTFW12 and rotate backward signals RTBWØ1 ... RTBW12. This is done via SCHMITT-trigger inverters for good pulse definition.

If one of the optical switches is operated, the relevant RTFW.. pulse is used for the generation of an interrupt level pulse ILØ3PU on output point 9 of NAND D4014 on each positive or negative going signal edge.
This pulse is used as clockpulse for the D-type flip flop D4016, resulting in an interrupt level signal ILØ3--LT which interrupts the microprocessor. This is done to realize a very quick reaction by the microprocessor when an optical switch is operated.

The flip flop output signal ILØ3--HT is used to clock the actual photo-transistor output levels in the three 3-state registers via the databus lines DBØØ ... DBØ7 for further processing.
In this way the microprocessor knows which switch is operated and in which direction.
The microprocessor will be interrupted by signal ILØ3--LT and generates in turn three different addresses and the UPRD--LT signals in order to read the contents of the 3-state registers.
If a front unit address is generated, the IO select signal IOSLØ4LT for the front unit will be active.

Selection of one of the 3-state registers is achieved then by decoder D4013, which decodes the three microprocessor address lines ABØ1, ABØ2 and ABØ3. This results then in one active low decoder output line (enable rotate) ENRTØ1, ENRTØ2 or ENRTØ3. This are the output enable signals for the three 3-state registers and the one which is enabled places its data on the microprocessor data bus lines DBØØ... DBØ7.
During the read cycle, flip flop D4016 will be set to its zero state again by signal ENRTØ1.

8.14.3 Address decoding table

The addresses which are generated by the microprocessor are decoded by address decoder D4013 according to the following table.

IOSLØ4LT	ABØ4	ABØ3	ABØ2	ABØ1	Function
0	1	0	0	0	ENRTØ1
0	1	0	0	1	ENRTØ2
0	1	0	1	0	ENRTØ3

8.14.4 Signal name list

UNIT A14

Signal name	Description	Signal source	Signal destination(s)
ABØ1...Ø4	Address bus Ø1...Ø4	A6+option	-
DBØØ...Ø7	Data bus ØØ...Ø7	A6+option	-
ENRTØ1	Enable rotate Ø1	A14	-
ENRTØ2	Enable rotate Ø2	A14	-
ENRTØ3	Enable rotate Ø3	A14	-
ILØ3--LT	Interrupt level Ø3	A14	A6
ILØ3--HT	Interrupt level Ø3	A14	-
ILØ3PU	Interrupt pulse	A14	-
IOSLØ4LT	I/O select Ø4	A6	-
RTBWØ1...12	Rotate backward Ø1...12	A14	-
RTFWØ1...12	Rotate forward Ø1...12	A14	-
UPRD--LT	Microprocessor read	A6	-
UPWR--LT	Microprocessor write	A6	-

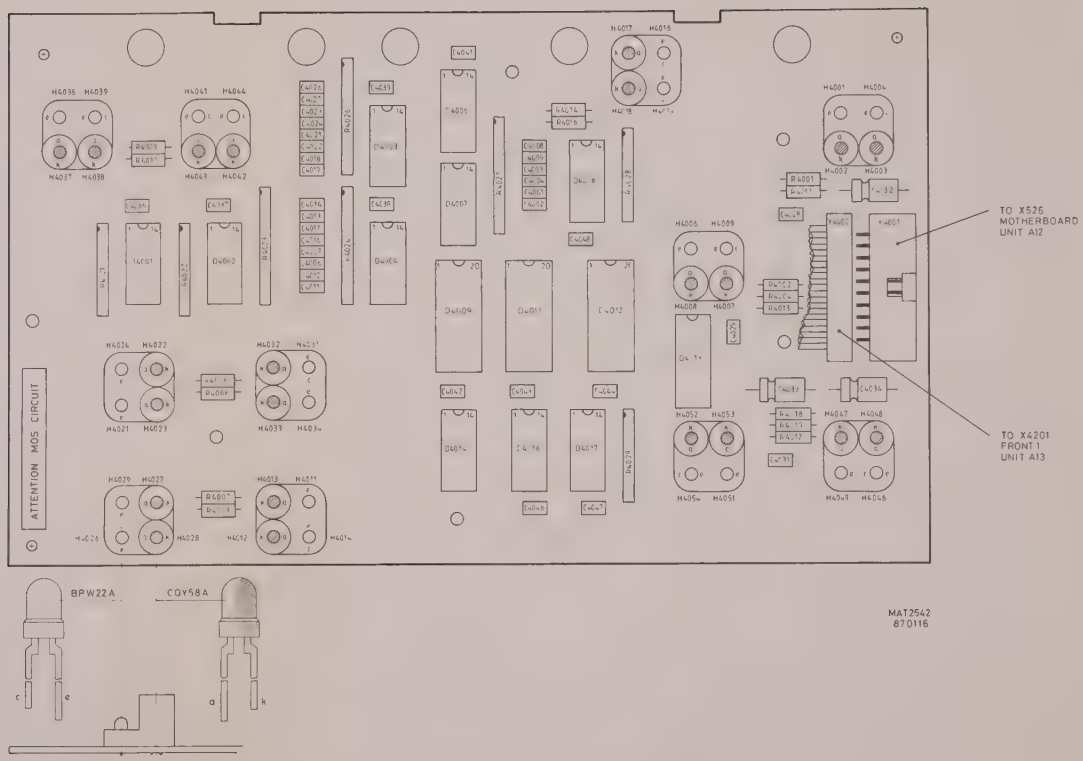


Figure 8.14.2 Unit A14 - FRONT 2 - p.c.b. lay out.

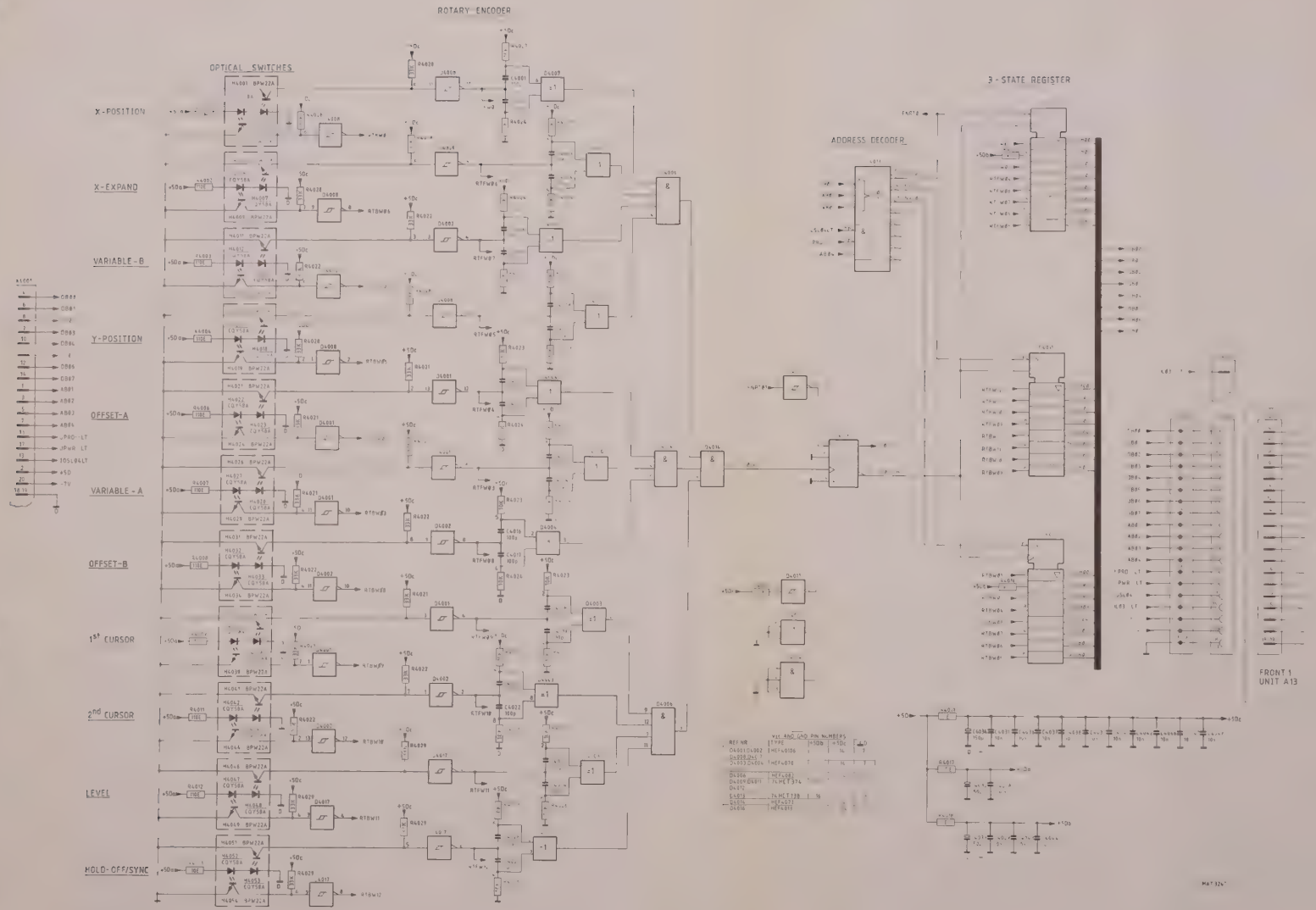
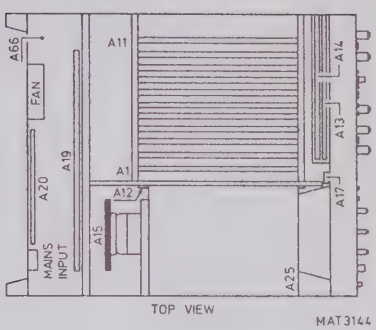


Figure 8.14.3 Unit A14 - FRONT 2 - circuit diagram.

UNIT A15 - Z AMPLIFIER UNIT



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8.15.3 Final focus stage..... 8.15-1
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8.15.1 General information

This unit basically comprises a Z-demodulator circuit, a final Z-stage and a final focus stage.

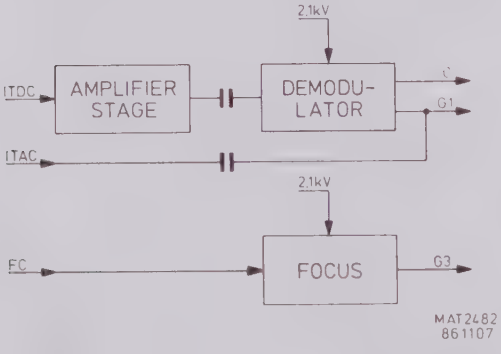


Figure 8.15.1 Blockdiagram final Z-stage.

8.15.2 Final Z-stage

The high frequency component ITAC of the Z-signal is fed via a high voltage capacitor C2806 to the high voltage part of the circuit.
The modulated low frequency component ITDC of the Z-signal is fed via a high voltage capacitor C2803 to a demodulator circuit in the high voltage part of the circuit.
The resulting demodulated signal is then combined with the high frequency component from C2806 and applied to the intensity grid G1 of the C.R.T.

8.15.3 Final focus stage

The focus signal FC is applied to the final focus stage brought on a correct level and applied to the focus grid G3 of the C.R.T.

8.15.4 Signal name list

Signal name	Description	Signal source	Signal destination(s)
f1	Filament 1	A20	-
f2	Filament 2	A20	-
FC	Focus	A1	-
ITAC	Intens a.c. component	A1	-
ITDC	Intens d.c. component	A1	-
X1	X1 input for C.R.T.	A1	-
X2	X2 input for C.R.T.	A1	-
Y1	Y1 input for C.R.T.	A1	-
Y2	Y2 input for C.R.T.	A1	-
-2,1 kV	-2,1 kV C.R.T.	A20	-

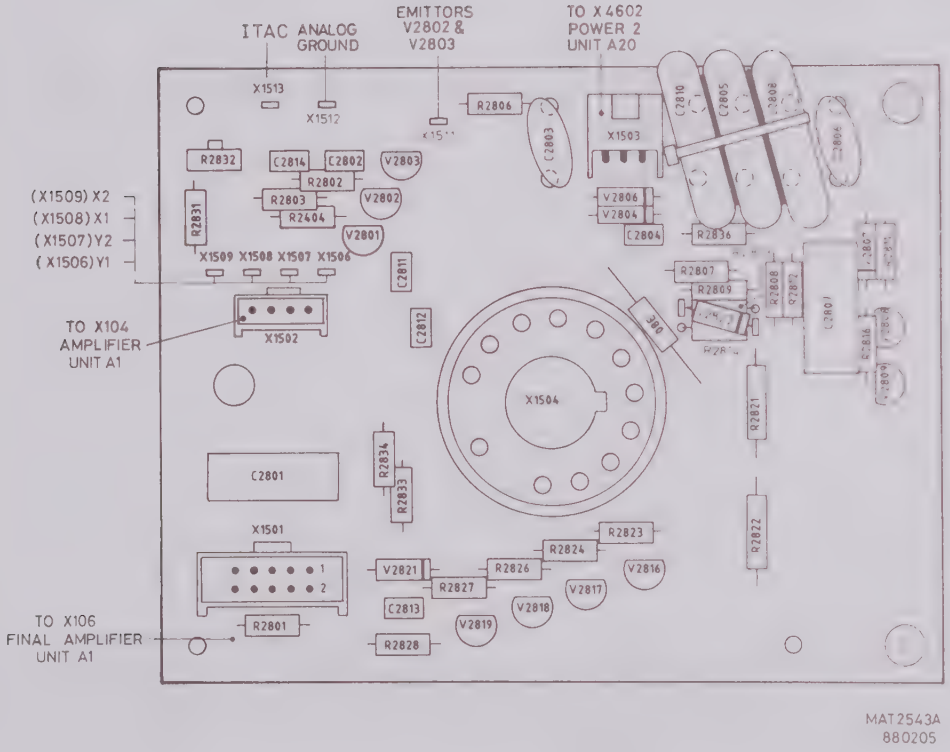


Figure 8.15.2 Unit A15 - Z-AMPLIFIER - p.c.b. lay-out.

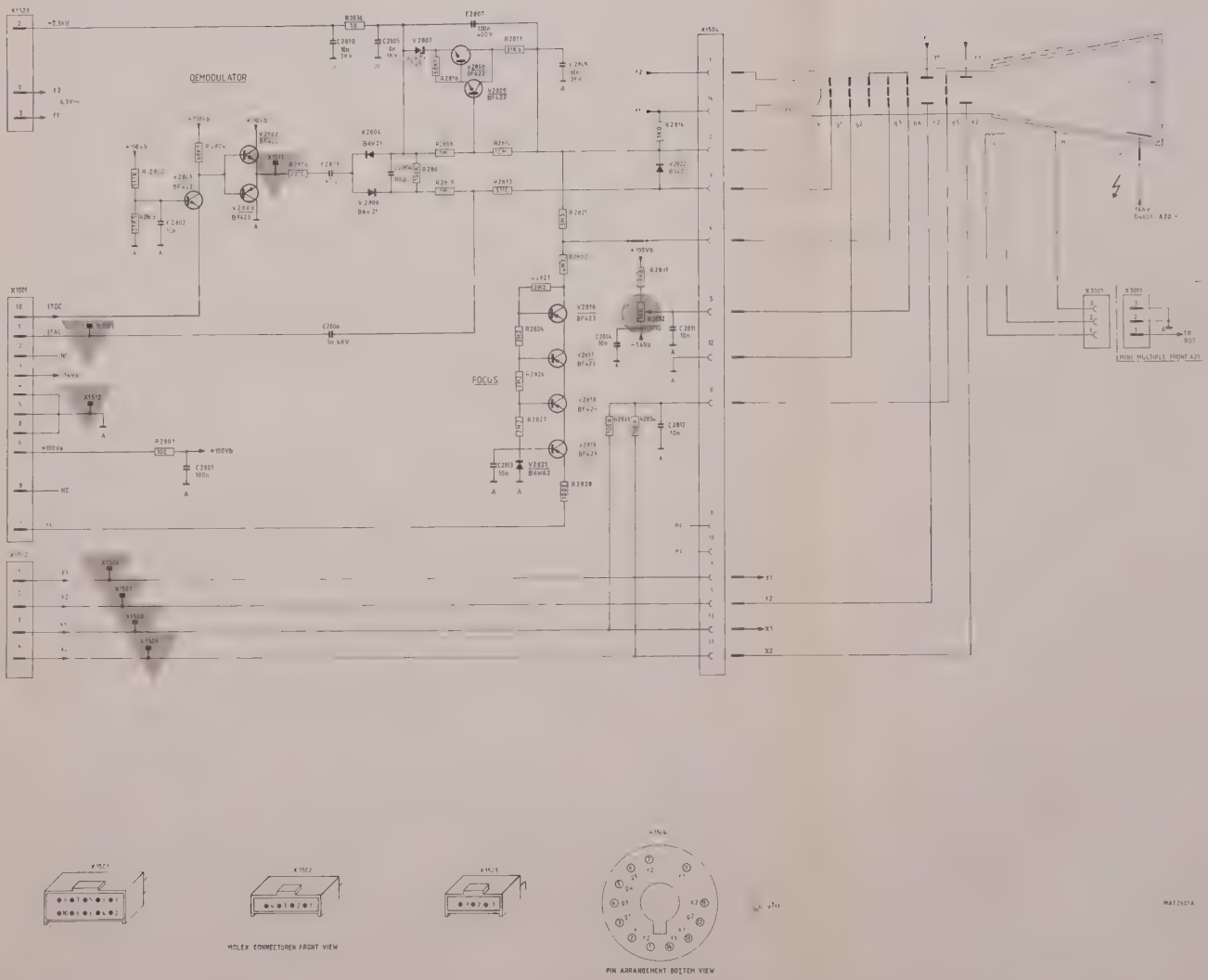
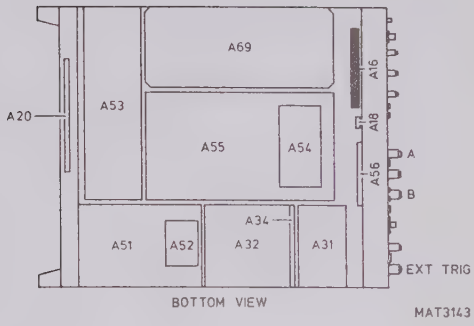


Figure 8.15.3 Unit A15 - Z-AMPLIFIER - circuit diagram.

UNIT A16 - C.R.T CONTROL UNIT



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8.16.2 Signal name list..... 8.16-2

8.16.1 General information

The C.R.T. CONTROL unit, which is located below the C.R.T., contains the frontpanel C.R.T. controls:

- FOCUS
- INTENS TRACE
- INTENS TEXT
- ILLUM
- TRACE ROT

The FOCUS level FCIN is applied to the focus circuit on unit A1.

The INTENSITY levels ITTR and ITTX are applied to unit A1 and depending on the current display block (trace or text) one of these two (trace or text) levels will be selected and applied to the Z-amplifier.

8.16.2 Signal name list

Signal name	Description	Signal source	Signal destination(s)
FCIN	Focus input	A16	A1
ITTR	Intensity trace	A16	A1
ITTX	Intensity text	A16	A1
TRRT	Trace rotation	A16	C.R.T.

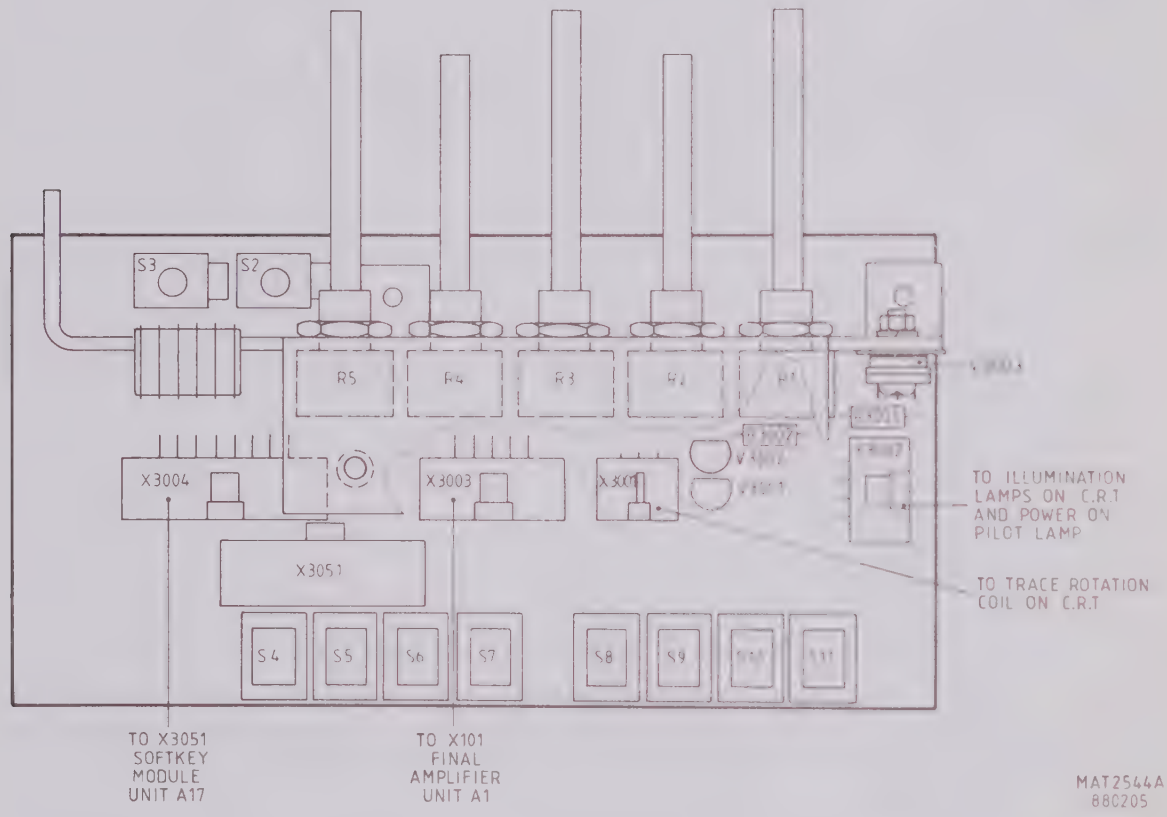


Figure 8.16.1 Unit A16 - C.R.T. CONTROL - p.c.b. lay out.

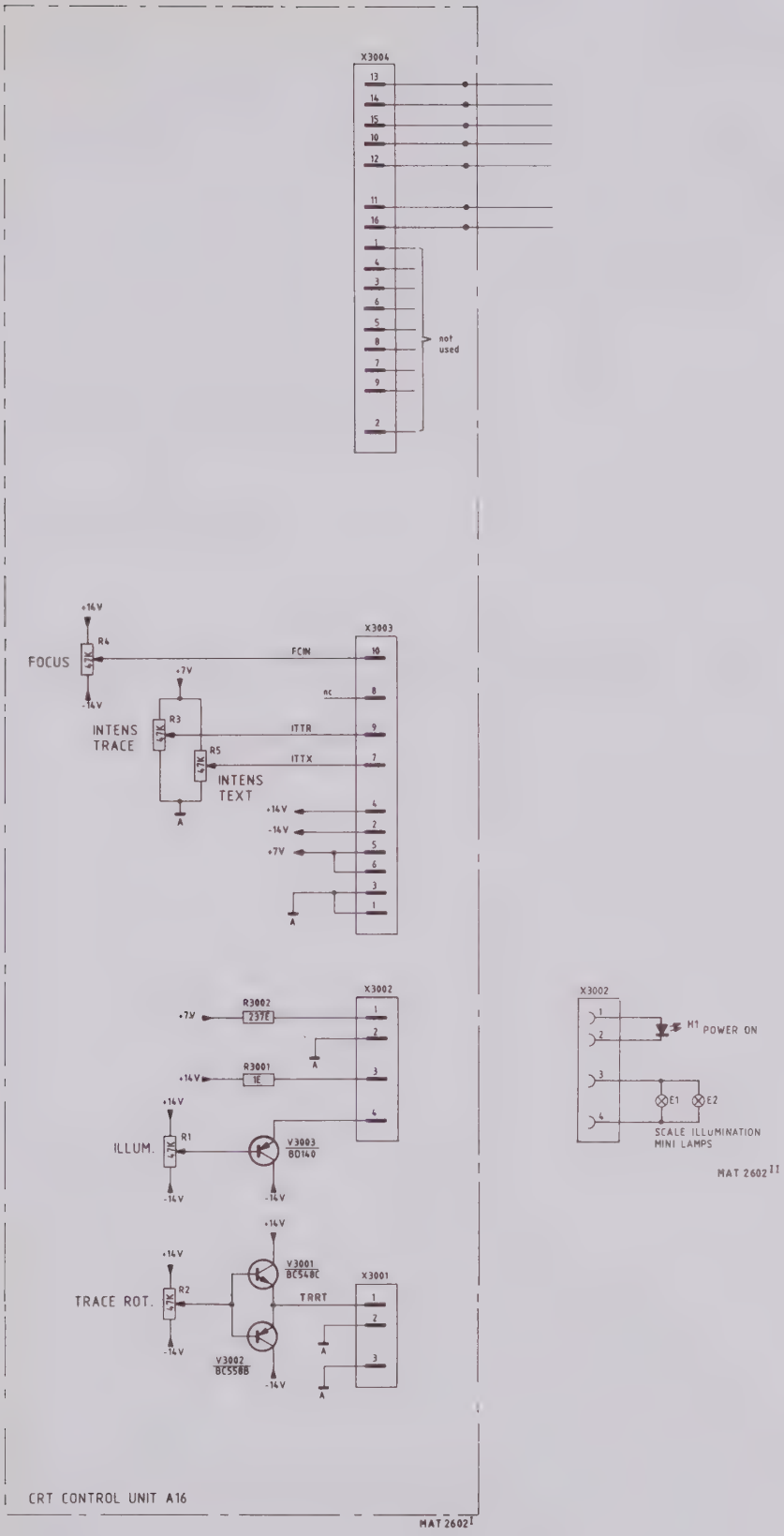
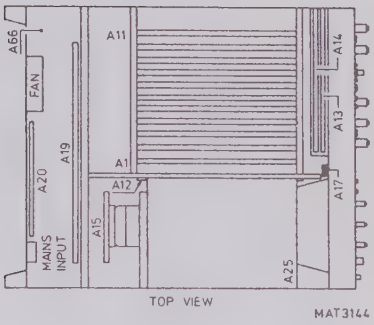


Figure 8.16.2 Unit A16 - C.R.T. CONTROL - circuit diagram.

UNIT A17 - SOFTKEY UNIT



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8.17.1 General information..... 8.17-1

8.17.1 General information

The SOFTKEY unit, which is located on the right side of the C.R.T., contains the row of eight frontpanel softkey switches.

See also section 8.13 FRONT 1.

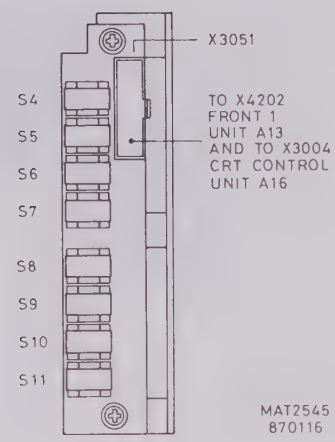


Figure 8.17.1 Unit A17 - SOFTKEY UNIT - p.c.b. lay-out.

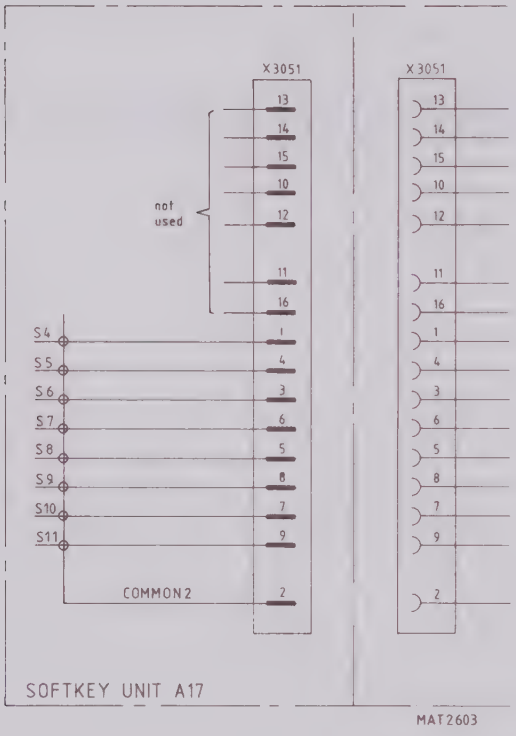
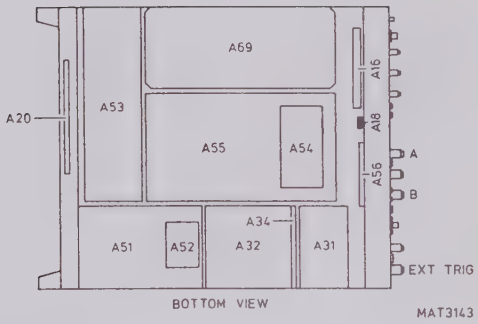


Figure 8.17.2 Unit A17 - SOFTKEY UNIT - circuit diagram.

UNIT A18 - SMOOTH + DOTS UNIT



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8.18.1 General information..... 8.18-1

8.18.1 General information

The SMOOTH + DOTS unit, which is located below the C.R.T., contains the switches DOTS and AVERAGE C=4 including the leds.

See also section 8.13 FRONT 1.

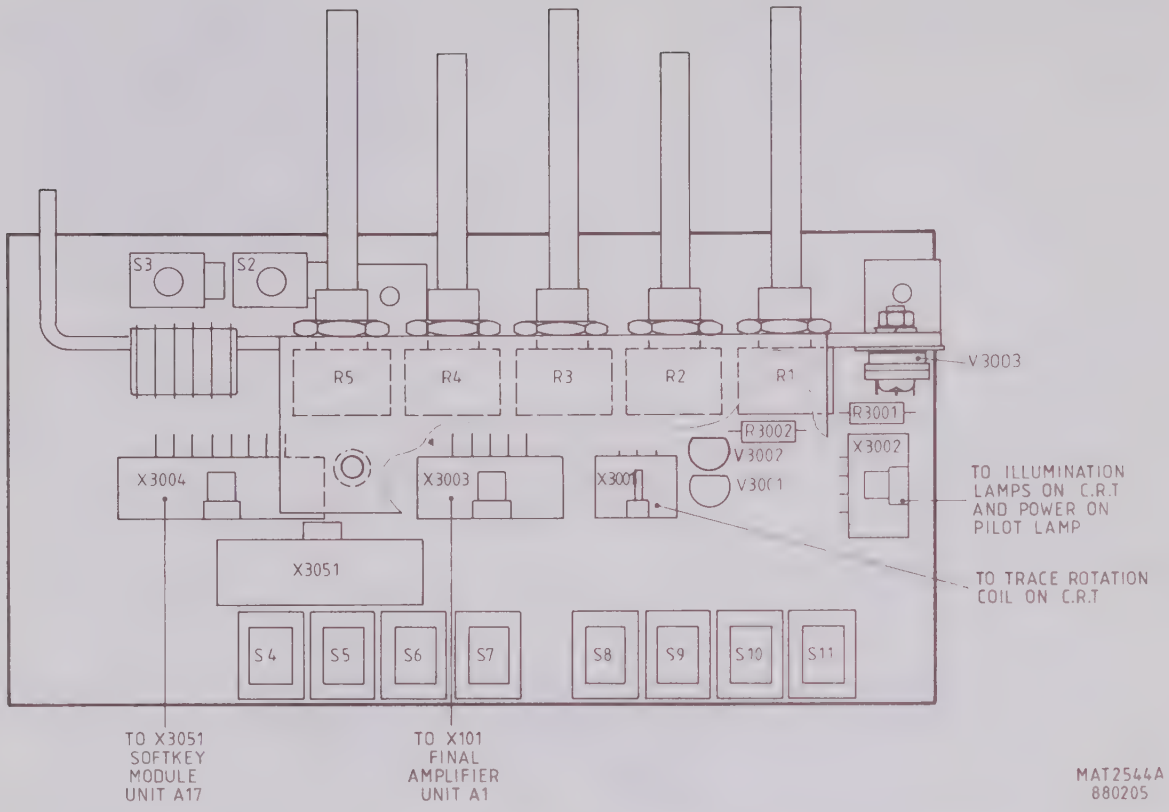


Figure 8.18.1 Unit A18 - SMOOTH + DOTS UNIT - p.c.b. lay-out.

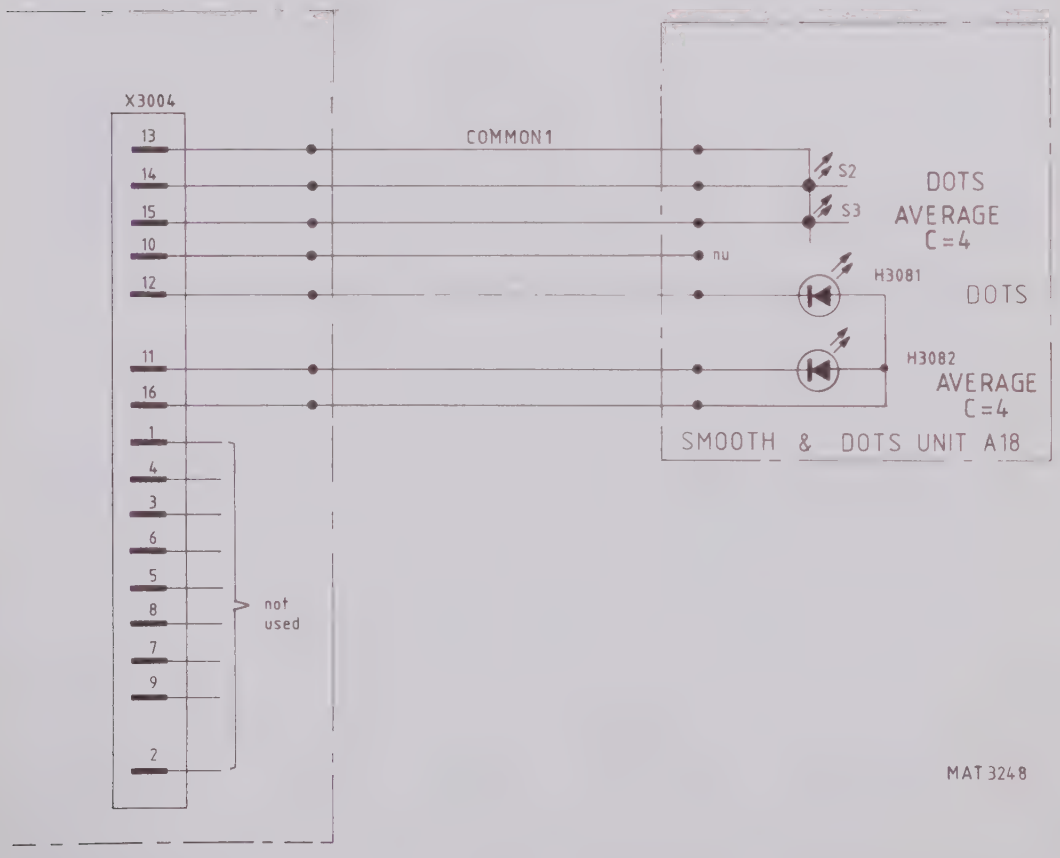
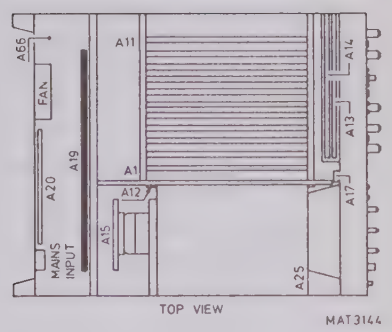


Figure 8.18.2 Unit A18 - SMOOTH + DOTS UNIT - circuit diagram.

UNIT A19 - POWER 1



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8.19.1 General Information

8

WARNING: The complete circuit is at mains potential up to transformer T4401 and opto-coupler H4401. To avoid any electrical shock, it is strongly recommended to read section 10.1 first.

The block diagram below shows the parts of this unit.

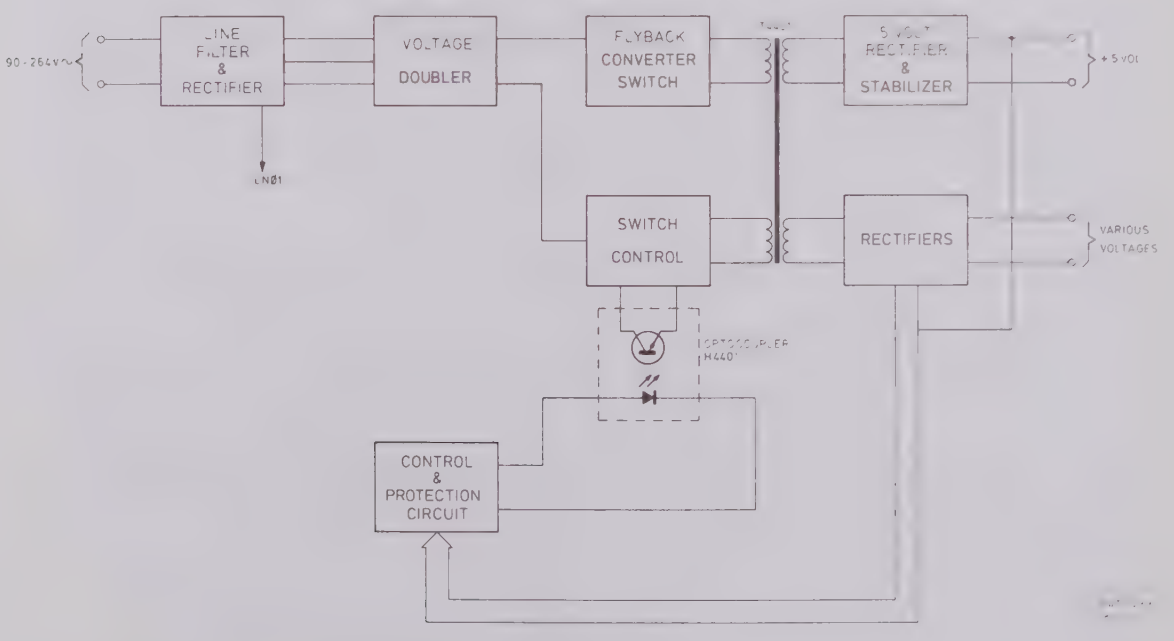


Figure 8.19.1 Block diagram.

The line voltage is applied via a line filter and a rectifier to a voltage doubler. The voltage is only doubled if the line voltage is below 140 V.
The output voltage of the voltage doubler is applied to transformer T4401 via a flyback converter, which consists of a flyback converter switch and a switch control circuit.
The switch control is influenced by the control and protection circuit via opto-coupler H4401. The latter and transformer T4401 perform a galvanic separation of the instrument from the line voltage.
The various output voltages of transformer T4401 are controlled by the control & protection circuit, which gives protection against over- and undervoltage and a too high temperature.
The +5 V for the digital circuitry has a separate stabilizer.
When the power is on, the POWER ON led on the front panel lights. This led is connected to +7 V on the CRT control unit A16.

8.19.2 The Mains filter and rectifier

The mains input (90 V...264 Vac) is filtered by a mains filter, consisting of C4401 and L4401 and fed into a full bridge rectifier (V4401...4404).
Resistors R4402 and R4403 have a surge current limiting function.
A capacitive network C4402...C4407 across the input serves to reduce interference, the centre-point being coupled to earth to provide electromagnetic compatibility. C4403 and R4401 provide a trigger pick-off point LNØ1 for LINE triggering.

8.19.3 The voltage doubler

To avoid the flyback converter switching high currents a voltage doubler has been provided. This doubler is switched off at high input voltages.
The principle of the voltage doubler is given in figure 8.19.2.

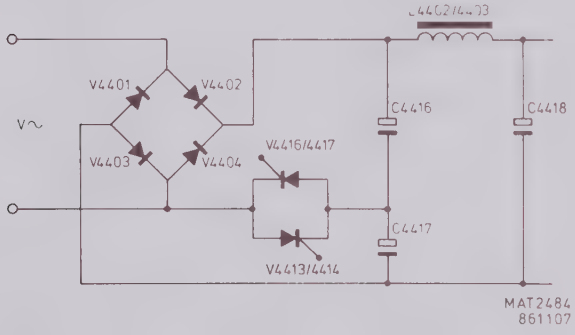


Figure 8.19.2 Simplified diagram of the voltage doubler.

The thyristors are turned on if the output voltage of the doubler is below 200 V approx. (double output voltage).
They are turned off if the output voltage rises above 400 V approx.

If the thyristors are off, the ac-voltage charges the series connection of C4416 and C4417 to the peak value. The voltage on both capacitors is smoothed by L4402/4403 and C4418.

If the thyristors are on, the positive phase of the ac-voltage charges C4416 via V4402 and V4416/17 to the peak value.
The negative phase charges C4417 via V4401 and V4413/4414 to the peak value.
The voltage on the series connection of C4416 and C4417, which is twice the peak voltage of Vac, is smoothed by L4402/4403 and C4418.

The thyristors are switched on and off by a schmitt-trigger circuit consisting of V4406/4408, V4407 and their associated components.

8.19.4 The flyback converter switch (see also figure 8.19.3)

The switch consists of a power transistor V4429, connected in series with diode V4419. The transistor is switched by 2 MOSFETS V4424/V4426, which are controlled by the switch control. By regulating the on and off periods of the switch, the output voltages of T4401 are controlled. The other components of the switch serve as a dV/dt limiter to decrease the switching dissipation, to reduce interference and to protect the switching transistors against overvoltages.

8.19.5 The switch control

The switch control is a rather complicated circuit, which will be explained by the simplified circuit diagram of figure 8.19.3.
After power on, a current via R4434/4436 and the b-c diode of V4433 charges C4423 until the treshold voltage of the FET is reached, after which the converter switch turns on. The current through winding 1-2 of T4401 and R4448...R4452 increases linearly and charges T4401.
This causes a linearly increasing voltage on winding 3-4, which turns the converter switch further on.
This is the forward stroke.

If the voltage over R4448...R4452 rises above 1,2 V the cathode-gate voltage of thyristor V4441 rises above 0,6 V and it will be fired.
The NTC resistor R4444 provides temperature compensation for the firing point of the thyristor.
Now the converter switch is blocked and the flyback stroke starts, during which the secondary windings of T4401 discharge via the rectifiers into the smoothing capacitors.
In this situation winding 3-4 of the transformer gives a negative voltage, which charges C4423 as indicated. The output voltage of V4433 will be zero, so the thyristor extinghuishes.

If the transformer is discharged, the output voltage of winding 3-4 drops to zero and C4423 supplies a positive voltage to V4433, which will turn the converter switch on. The forward stroke starts again and so on.

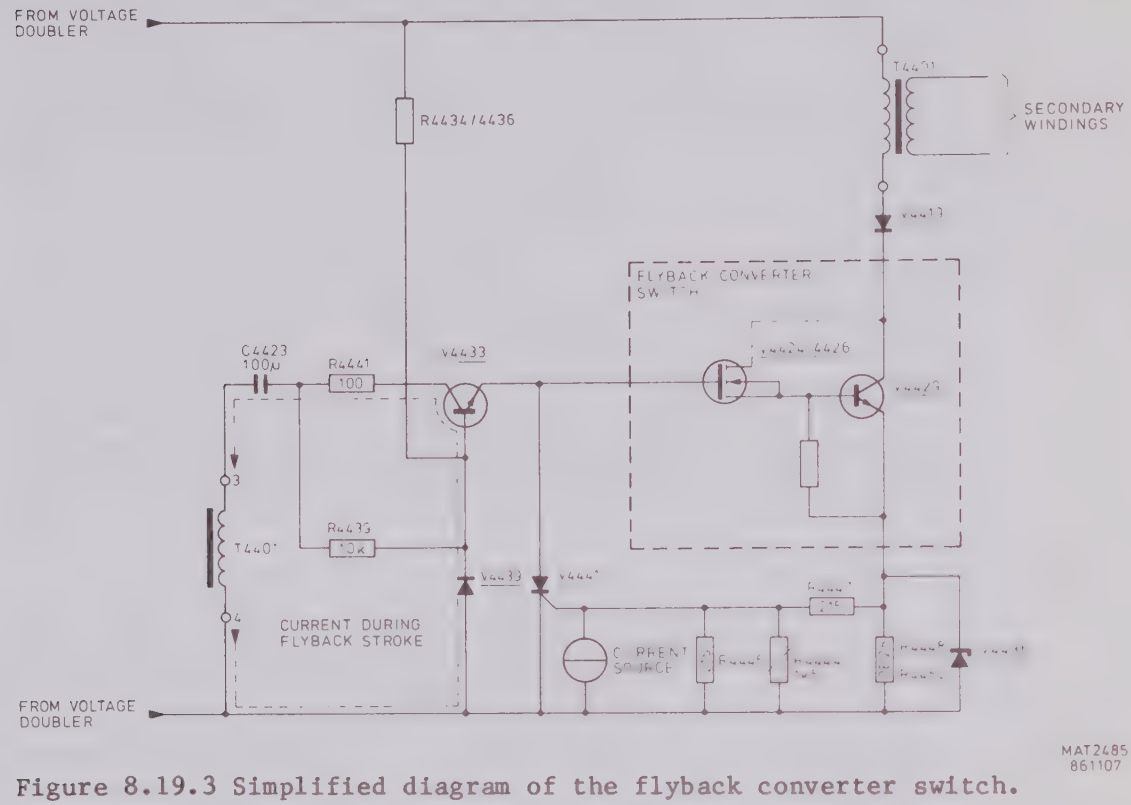


Figure 8.19.3 Simplified diagram of the flyback converter switch.

V4433, R4439 and V4439 form a voltage stabilizer circuit during the forward stroke, which limits the voltage on the gates of the MOSFETS to 15 V. The switching frequency varies from 20 kHz to 40 kHz, depending on the input voltage.

By inserting a current in R4446 with a current source, the on/off time of the converter switch (duty cycle) can be influenced. This is used to control the output voltages of T4401.
The current source is realised with opto-coupler H4401, which is supplied by C4424. This capacitor is charged during the forward stroke via V4438.
The opto coupler is controlled by the control and protection circuit.

If one or more of the transistors of the converter switch are blown, the zenerdiode V4436 prevents the burning out of R4448...R4452 and the whole switch control circuit, because it blows itself and makes a short circuit over R4448...R4452.
Afterwards, the mains fuse will blow.
If, after having replaced the converter switch transistors and the mains fuse, the power is turned on again, the thyristor V4441 can´t be fired due to the short circuit of V4436. In consequence the converter switch won´t be turned off and the TRANSISTORS and MAINS FUSE will BLOW AGAIN.

WARNING: Replace always zenerdiode V4436 after having replaced one or more converter switch transistors (V4424, V4426 and V4429) and the mains fuse.

Figure 8.19.4 shows some wave-forms in the flyback converter.

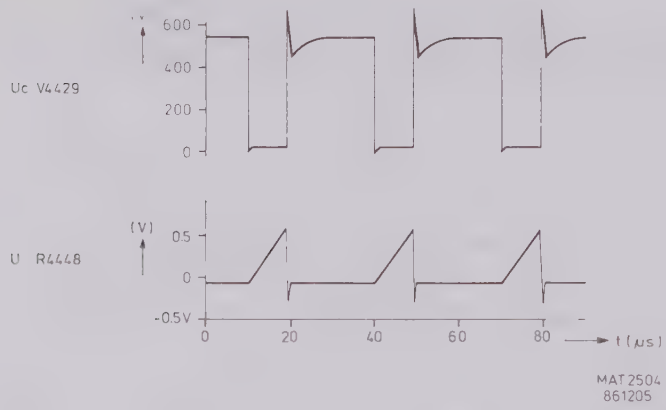


Figure 8.19.4 Voltage waveforms in the flyback converter.

8.19.6 The control circuit

This circuit consists of an operational amplifier (N4401) with some associated components.
The rectified and smoothed +14 V is fed back to the op-amp and compared with the 10 V reference voltage, RV10, which comes from unit A20.
If the +14 V is too high, the op-amp supplies more current into the opto coupler. Next, the opto coupler supplies more current into R4446, which causes the thyristor V4441 to be fired earlier. This shortens the forward stroke, so transformer T4401 is charged less. Next the flyback stroke will be shorter and the smoothing capacitors will be charged less and the output voltages, +14 V inclusive, decrease. So only the +14 V is regulated. All the other voltages are not regulated, except the +5 volt (+5D).
Because the output voltages depend on the length of the flyback stroke, the flyback stroke is regulated by the control circuit.
The +5D has a separate stabilizer, which works during the forward stroke (see 8.19.8)

Resumed:

- If the load on +14 V varies, the forward and the flyback stroke vary. The duty cycle remains constant; the frequency varies.
- If the input voltage varies, only the forward stroke varies; the flyback stroke remains constant. A higher input voltage results in a shorter forward stroke.
- The load on the +5D influences only the waveform of primary current through transformer T4401 during the forward stroke. The frequency and the duty cycle remain constant.

8.19.7 The protection circuit

The protection circuit gives the protection against:

- overvoltage on +5D
- overvoltage on +14 V
- too high temperature
- undervoltage on -7 V

The signal C-ON serves as a power supply for this circuit.
Overvoltage on +5D or on +14 V makes V4476 conducting. A too high temperature (e.g. caused by a failure of the fan) also makes V4476 conducting, due to the effect of PTC R4469.
V4476 makes V4474 conducting and via R4459 both transistors keep themselves conducting.
Now V4474 supplies a high current into the opto-coupler, which makes the forward stroke very short and eliminates the overvoltage.

If there is a short circuit in one of the voltage on the secondary side of the transformer all voltages will drop, the -7 V inclusive. This causes V4473 to conduct, due to a voltage rise on the node V4471, R4461, V4472. Next V4471 conducts, which makes the forward stroke very short. No components will be overcharged in this way, in spite of the short circuit.
To prevent the undervoltage protection being active immediate after power on, a delay circuit consisting of R4461 and C4461 is provided. After an over- or undervoltage detection C4461 is discharged fastly by the mains switch, which has a contact connected to connector X4402, when the oscilloscope is switched off.

8.19.8 The +5 volt stabilizer

The output voltage of winding 10-20 of transformer T4401 depends on the load of the +14 V, because this voltage is regulated by the control unit by means of the flyback stroke.
To get a stable +5 V power supply for the digital circuits (+5D) a stabilizer is provided, which works during the forward stroke (forward converter).
During the positive phase of winding 10-20 (the forward stroke), C4429 is charged via L4408, V4449 and L4409. The voltage on C4429 is smoothed by L4411/4412 and C4431.
During the negative phase (the flyback stroke), V4451 acts as a flywheel diode for L4409.
There also flows a current from +5D through V4486, and V4484 in the reverse direction through choke L4408. This demagnetises the core of L4408 or even magnetises it in the reverse direction, depending on the value of the reverse current.
During the forward stroke, the core of L4408 has to be magnetised again. The more the core has to be magnetised, the higher the self inductance will be and the lower the voltage on C4429 and C4431 will be.
A lower voltage on +5D causes the operational amplifier N4401 to give a higher output voltage. The transistor V4486 conducts less, the reverse current through choke L4408 and so the self inductance decrease and so the voltage on C4429 and C4431 rises.
RV10 serves as a reference voltage.

8.19.9 The rectifiers

The rectifiers consist of standard rectifying circuits with smoothing filters.

8.19.10 Signal name list

UNIT A19

Signal name	Description	Signal source	Signal destination(s)
BAVO	Battery voltage	A66	-
C-ON	Converter on	A19	A19,A20
FRUVP	Fast reset under voltage protection	A19	A66
ILØ7--LT	Interrupt level Ø7	A20	-
LNØ1	Line Ø1	A19	A20
M1	Mains 1	A66	-
M2	Mains 2	A66	-
PE	Protective earth	A66	-
RVG	Reference voltage ground	A20	-
RV1Ø	Reference voltage 1Ø V	A20	-
A	Analogue ground	A19	General
D	Digital ground	A19	General
+5D	+5 Volt digital	A19	General
-5D	-5 Volt digital	A19	General
+7V	+7 Volt	A19	General
-7V	-7 Volt	A19	General
+14V	+14 Volt	A19	General
-14V	-14 Volt	A19	General
+19V	+19 Volt	A19	General
-19V	-19 Volt	A19	General
+40V	+40 Volt	A19	General
+100V	+100 Volt	A19	General

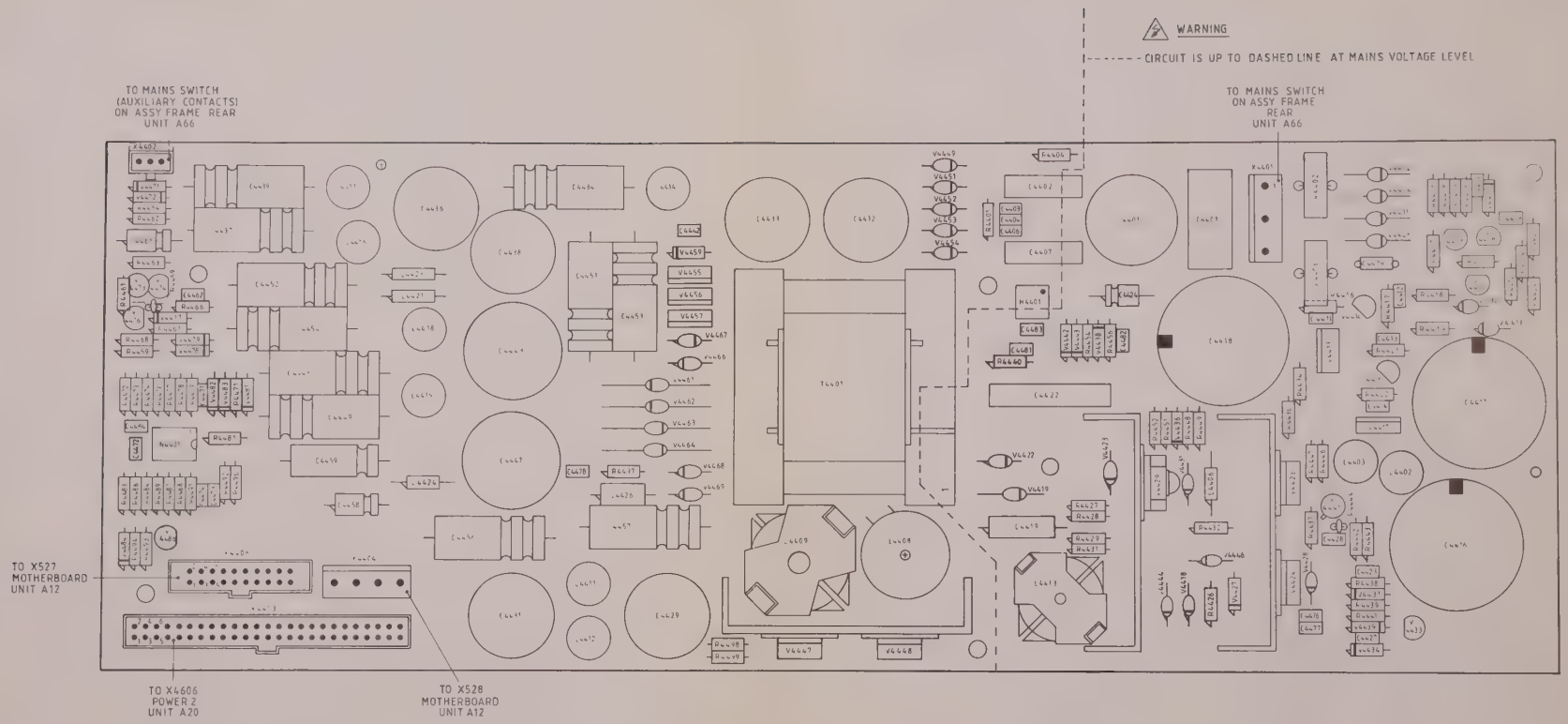


Figure 8.19.5 Unit A19 - POWER 1 - p.c.b. lay-out.

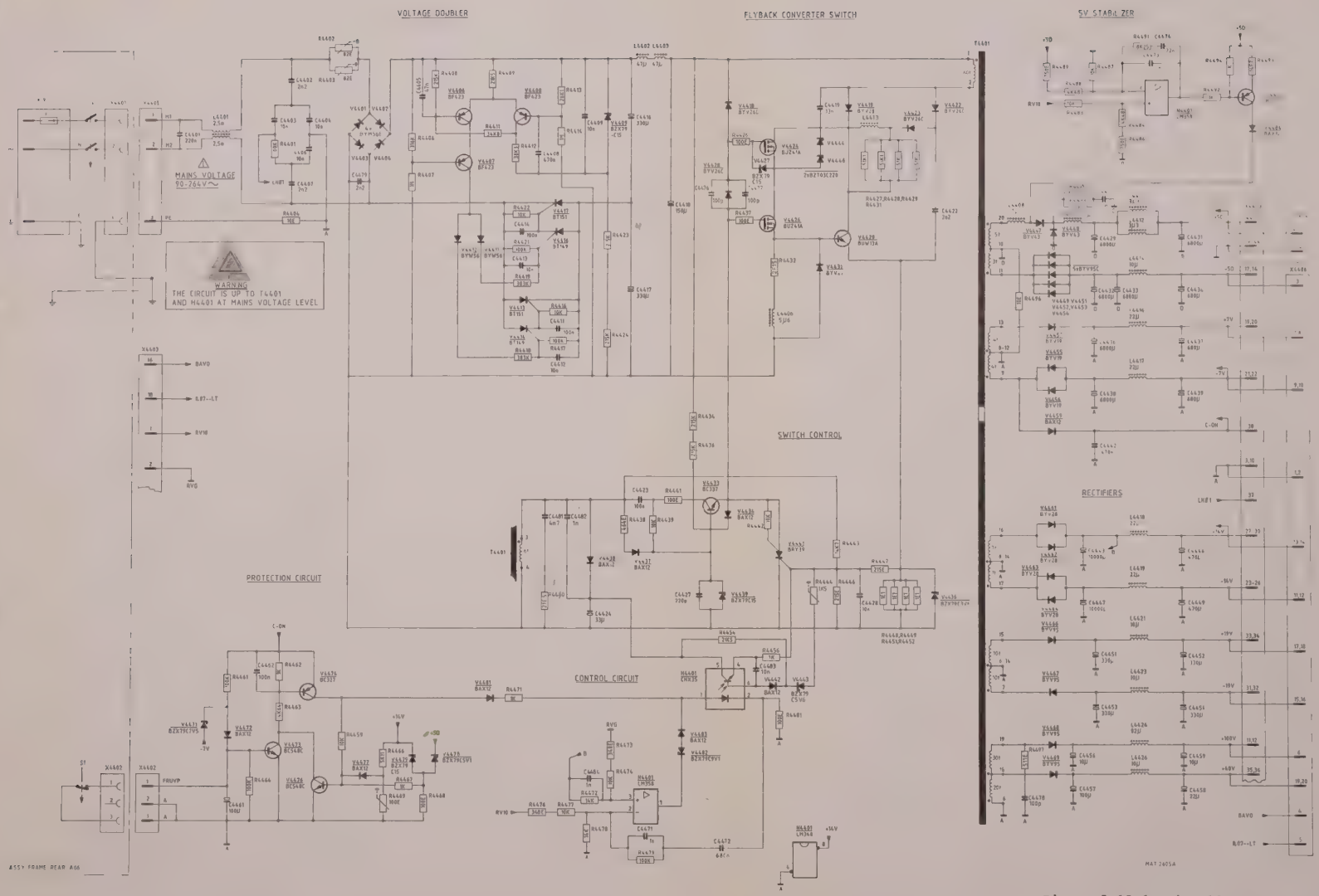
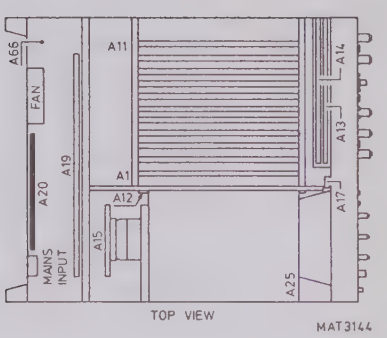


Figure 8.19.6 Unit A19 - POWER 1 - circuit diagram.

UNIT A20 - POWER 2



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8.20.3 The line trigger circuit..... 8.20-1
8.20.4 The power down/up detection circuit..... 8.20-2
8.20.5 The EHT converter..... 8.20-2
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8.20.1 General information

This unit consists of several circuits:

- a reference voltage source
- a line trigger circuit
- a power down/up detection circuit
- an EHT converter
- a fan-control circuit

WARNING: To avoid any electrical shock, it is strongly recommended to read section 10.1 first.

8.20.2 The reference voltage source

The voltage source consists of an operational amplifier N4601 with the associated components.
The zenerdiode V4601 (6,5 V) serves as the reference voltage source for the op-amp.
Via diode V4602 the node R4601, R4602, V4602 is kept at a stable voltage of 9,4 V to achieve a stable current through zenerdiode V4601.
The output voltage RV10 can be adjusted with R4607.

8.20.3 The line trigger circuit

The line trigger circuit is not used in this instrument.

8.20.4 The power down/up detection circuit

The circuit consists of two comparators (N4602) with their associated components.
After power on, the signal C-ON goes high (> 20 V). After a time delay of 0.1 sec, determined by R4644 and C4622, the ILØ7--LT goes high. This signal, which is routed to the microprocessor unit A6, tells the microprocessor that the power is on and it can start.
In case of a converter failure, the C-ON-signal goes immediately low, which causes the signal ILØ7--LT to go low with a very short time delay, because C4622 is discharged fast via R4643 and N4602. The microprocessor will stop.

NOTE: C4622 can´t be charged via R4643, because N4602 has open collector outputs.

8.20.5 The EHT converter

Transformer T4601 forms with the various capacitive loads an LC resonance circuit, with an own frequency of approx. 60 kHz.
The circuit is every period charged by a thyristor circuit, consisting of transistors V4608 and V4612 (switched parallel resonance converter).
The thyristor circuit is fired on the negative peak of T4601-9 (see figure 8.20.1). On the negative peak of T4601 - 9, the capacitor C4609 is charged via V4603, R4616, R4618, the b-e junction of V4608 and diode V4607. This fires the thyristor circuit.
Now V4611 charges the LC resonance circuit as soon as T4601 - 9 becomes positive, and V4608 discharges V4608.
When V4608 is discharged the thyristor circuit turns off, because the current from V4603 is below the treshold current of the thyristor circuit. Now C4608 is charged again via V4603.
A higher voltage at the base of V4603 results in a higher charge of C4608 and causes the thyristor circuit to be turned off later, so there will be supplied more energy to the resonance circuit, in this case the output transformer.
During the off-time of the thyristor circuit C4608 is discharged via R4616.

One output voltage (-2,1 kV) is fed back into op-amp N4601 to perform voltage stabilisation.
If the output voltage rises (i.e. -2,1 kV goes more negative) then N4601-3, N4601-1 and the emitter of V4603 go more negative. The on-time of the thyristor circuit will be shorter; the energy supplied to the transformer will decrease and therefore the output voltages will also decrease.

The output voltage F1/F2 (6,3 V) supplies the filament.
The output voltage of T4601-6 is rectified by V4613 and gives the -2,1 kV cathode voltage for the CRT and the feedback to N4601.
The output voltage of T4601-11 is converted to 14 kV in the HT-multiplier D4001 to supply the post acceleration anode of the CRT.
For security reasons the EHT ground is separated from the analogue ground on connector X4604 (1A, 1C, 2A, 2C) when the unit is removed.
The EHT is not available now (see also section 10.4).

The following figure gives some voltages in the circuit.

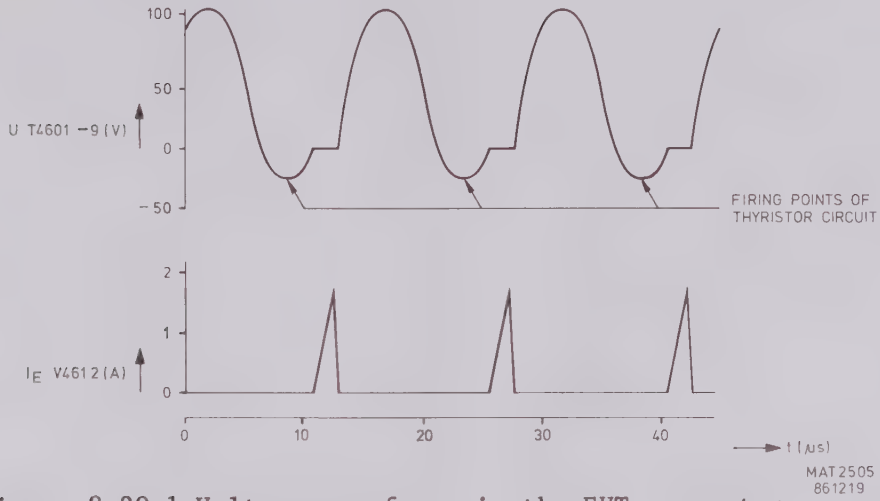


Figure 8.20.1 Voltage waveforms in the EHT converter.

8.20.6 The fan control circuit

In this circuit, a triangle wave voltage of 70 kHz is generated by comparator N4602. Resistor R4652 loads the open collector output. This triangle voltage is on N4602-5 compared with a voltage on N4602-4, which is influenced by a NTC resistor R4656 on this board.
The output voltage on N4602-2 is a square-wave signal, whose duty cycle depends on the temperature of the NTC. This square-wave switches via V4621 and V4622 a converter, consisting of L4601, V4619 and C4624, which gives a maximum voltage of 28 V. The output voltage is supplied to the fan and fed back to N4602-4 via V4618 to achieve an overvoltage protection for the fan.
If V4622 doesn't switch for some reason, the fan runs on 14 V via L4601, V4619 and L4602, which is mostly sufficient to keep the oscilloscope running.

8.20.7 Signal name list

UNIT A20

Signal name	Description	Signal source	Signal destination(s)
BAVO	Battery voltage	A66	-
C-ON	Converter on	A19	-
EG	EHT ground	A20	A25
FS	Fan supply	A20	A66
f1	Filament 1	A20	A15-C.R.T.
f2	Filament 2	A20	A15-C.R.T.
ILØ7--LT	Interrupt level Ø7	A20	A19-A12-A6
LNØ1	Line Ø1	A19	-
LN	Line trigger	A20	Not used
RVG	Reference voltage ground	A20	A20,A19
RV1Ø	Reference voltage 1Ø V	A20	A20,A19
-2,1 kV	-2,1 kV C.R.T.	A20	A20,A15-C.R.T.
14 kV	14 kV EHT C.R.T.	A20	C.R.T.

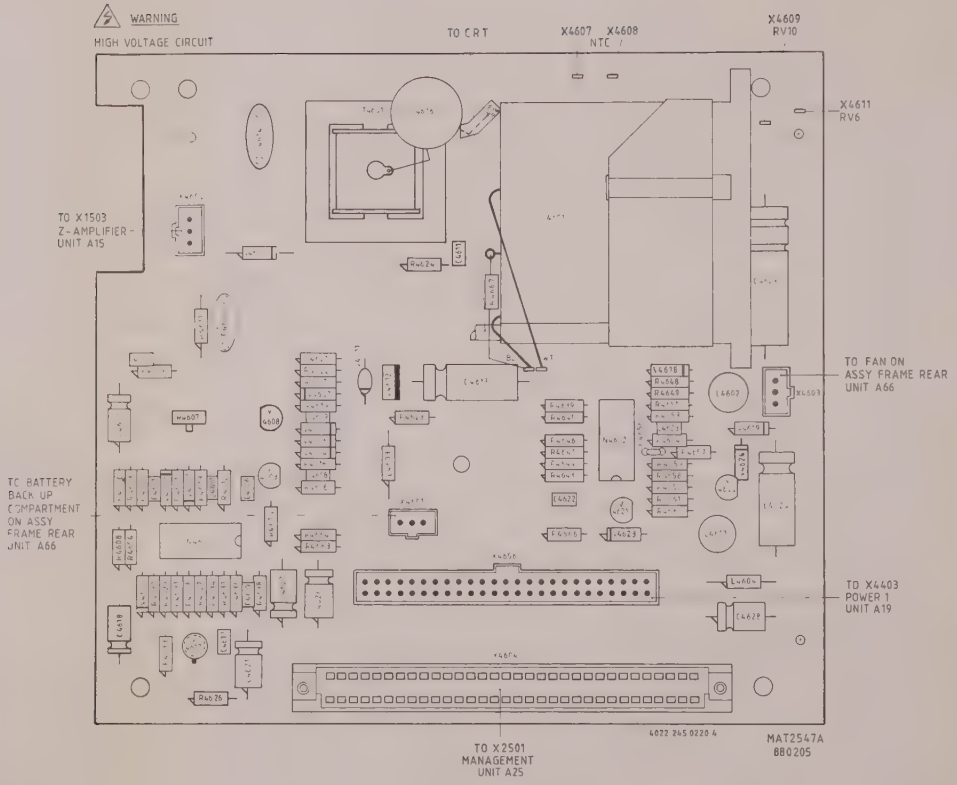


Figure 8.20.2 Unit A20 - POWER 2 - p.c.b. lay-out.

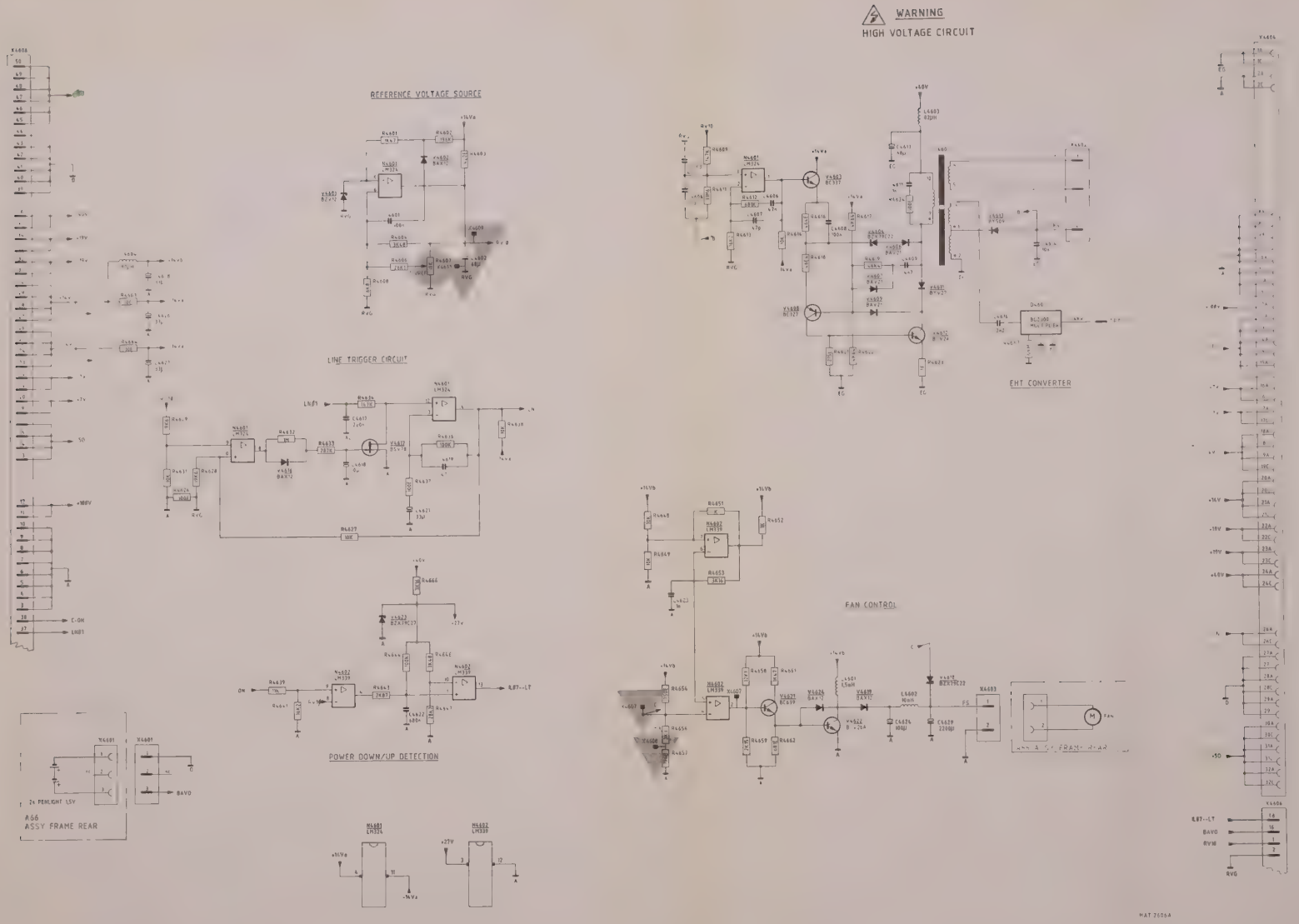
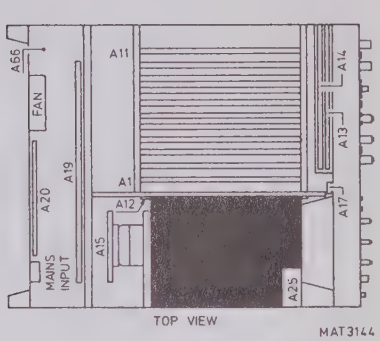


Figure 8.20.3 Unit A20 - POWER 2 - circuit diagram.

UNIT A25 - MANAGEMENT UNIT



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8.25.4 Auxiliar circuits..... 8.25-2
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8.25.1 General information

This unit mainly consists of:
- an interface between the microprocessor (unit A6) and the signal acquisition units (A31, A32, A34, A51 and A52).
- the first part of feedback loop.
- some auxiliar circuits.

8

8.25.2 Interface

The interface part consists of:

DATA BUFFER	D3101
ADDRESS BUFFER	D3102
I/O SELECT DELAY	D3117, D3119
ADDRESS DECODER	D3104, D3106, D3107
STATUS FLIPFLOPS	D3108, D3109, D3111, D3112, D3113, D3114, D3116
INPUT PORT	D3103
OFFSET DACs	D3136, D3137, D3138, D3139
TRIGGER LEVEL DAC	D3141

Data from or to the microprocessor are buffered by the bidirectional DATA BUFFER.
The ADDRESS BUFFER buffers four address lines (ABØ1...ABØ4) from the microprocessor before they are applied to the ADDRESS DECODER. It also buffers some control signals.
The I/O SELECT DELAY generates correctly timed signals to control the buffers.
The ADDRESS DECODER generates clock signals for the STATUS FLIPFLOPS and 4 latch enable signals for DACs on this unit and the Time-base unit A51. These signals are: LETRLV, LETRDL, LEHDOF and LEFSRM.
The latch enable signal for the INPUT PORT is generated at D3104 pin 14.
The STATUS FLIPFLOPS generate a number of latch enable signals for serial latches, and data plus clock signals for these latches (SEDA1, SEDA2, SECK1 and SECK2).

The latch enable signals are:

Name	Destination
LEVGBA	Management unit A25
LEVGBB	Management unit A25
LEVGFA	Vertical signal unit A55
LEVGFB	Vertical signal unit A55
LEVEA	Vertical signal unit A55
LEVEB	Vertical signal unit A55
LETRST	Trigger control unit A34
LETBST	Time-base unit A51

If a setting modification of the instrument means that a new acquisition should be started, then the new setting is done via SEDA1 and SECK1 (e.g. TRIGGER LEVEL), otherwise it is done via SEDA2 and SECK2 (e.g. OFFSET).
Via the INPUT PORT the microprocessor reads four probe information signals from the Distribution unit A53 and three signals from the Trigger control unit A34.
The four OFFSET DACs are 14 bit serial DACs. Two DACs give an offset coarse signal (one for each channel) and the other two DACs give an offset fine signal. The four output signals are applied to the Vertical signal unit A55.
The TRIGGER LEVEL DAC is also a 14 bit serial DAC. Its output signal is applied to the Trigger control unit A34.

8.25.3 Feedback loop

The part of the feedback loop that is mounted on this unit consists of twice the same circuit, one for each channel. Only the part from channel A will be described.
The sample data from the DPU unit A9 are stored in the SAMPLE DATA REGISTER (D3122, D3123). The most significant dataline SADB11 is inverted in CODE CONVERT to obtain conversion from two´s complemented code to straight binary code.
When FBRY goes high the sample data are stored. The signal CHPTdetermines wether the sample data are for channel A (high) or for channel B (low).
The sample data are converted into an analoge voltage by the FEEDBACK DAC (D1327) and two opamps (N3129, N3131) and associated circuitry. This voltage is applied to a multiplying DAC (D3143) of the VARIABLE FEEDBACK circuit. The digital code to the DAC comes from a shift register (D3142), which gets its data from the microprocessor. The output signal of the DAC is buffered and applied to the Vertical signal unit A55.

8.25.4 Auxiliar circuits

The CHANNEL SWITCH DRIVER converts the channel switch signal (CHSW) in a current (CHSW-1) which is able to drive the CHANNEL SWITCH on the Vertical signal unit A55.

NOTE: The flatcable between connector X501 on the Motherboard unit A12 and connector X3101 on this unit has crossed interconnections. This means that connector pin A1 on one end becomes B32 on the other end, etc.

8.25.5 Signal name list

UNIT 25

Signal name	Description	Signal source	Signal destination(s)
ABØ1...Ø4	Address bus Ø1...Ø4	A6+Option	-
ABØ1-1...Ø4-1	Address bus Ø1-1... Ø4-1	A25	A25
CHPT	Channel pointer	A5	-
CHSW	Channel switch	A5	-
CHSW-1	Channel switch 1	A25	A53-A55
CKVEA	Clock vertical A	A25	A25
CKVEB	Clock vertical B	A25	A25
CKACL	Clock acquisition control logic	A25	A25
CKSEDA	Clock serial data	A25	A25
CKTB	Clock time-base	A25	A25
CKTR	Clock trigger	A25	A25
CKVGBA	Clock variable gain backward A	A25	A25
CKVGBB	Clock variable gain backward B	A25	A25
CKVGFA	Clock variable gain forward A	A25	A25
CKVGFB	Clock variable gain forward B	A25	A25
CNDWMO	Count down mode	A34	-
CNSTCNLT	Count stair counter	A5	-
DBØ8...15	Data bus Ø8...15	A6+Option	-
DBØ8-1...15-1	Data bus Ø8-1...15-1	A25	A25
FBOTA	Feedback output A	A25	A25
FBOTB	Feedback output B	A25	A25
FBRY	Feedback ready	A8	-
IOSLØ7LT	I/O select Ø7	A6	-
IOSLØ7-1	I/O select Ø7-1	A25	A25
LEACL	Latch enable acquisition control logic	A25	A12-A5
LEFSRM	Latch enable fast ramp	A25	A53-A51
LEHDOF	Latch enable hold off	A25	A53-A51
LETBST	Latch enable time-base status	A25	A53-A51
LETRDL	Latch enable trigger delay	A25	A53-A51
LETRLV	Latch enable trigger level	A25	A25
LETRST	Latch enable trigger status	A25	A53-A51-A34
LEVEA	Latch enable vertical A	A25	A53-A55
LEVEB	Latch enable vertical B	A25	A53-A55
LEVGBA	Latch enable veriable gain backward A	A25	A25
LEVGBB	Latch enable variable gain backward B	A25	A25

Signal name	Description	Signal source	Signal destination(s)
LEVGFA	Latch enable variable gain forward A	A25	A53-A55
LEVGFB	Latch enable variable gain forward B	A25	A53-A55
LOSCRA	Latch offset coarse A	A25	A25
LOSCRB	Latch offset coarse B	A25	A25
LOSFIA	Latch offset fine A	A25	A25
LOSFIB	Latch offset fine B	A25	A25
OSCRA	Offset coarse A	A25	A55
OSCRB	Offset coarse B	A25	A55
OSFIA	Offset fine A	A25	A55
OSFIB	Offset fine B	A25	A55
PRIFA1	Probe information A1	A53	-
PRIFA2	Probe information A2	A53	-
PRIFB1	Probe information B1	A53	-
PRIFB2	Probe information B2	A53	-
RDPRIF	Read probe information	A25	A25
RSSTCNLT	Reset stair counter	A5	-
SADBØØ...1Ø	Sample data bus ØØ...1Ø	A9+A11	-
SECK1	Serial clock 1	A25	A25, A53-A55, A53-A51, A53-A51-A34
SECK2	Serial clock 2	A25	A25, A53-A55, A53-A51
SEDA1	Serial data 1	A25	A25, A53-A55, A53-A51, A53-A51-A34
SEDA2	Serial data 2	A25	A25, A53-A55, A53-A51
STSAGTLT	Start sampling gate	A52	-
SYMO--LT	Synchronize mode	A34	-
TRLV	Trigger level	A25	A34
TRSVHI	Trigger sensitivity high	A34	-
UPRD--LT	Microprocessor read	A6	-
UPRD-1LT	Microprocessor read 1	A25	A25
UPRSOT-1	Microprocessor reset output 1	A25	A25
UPRSOTLT	Microprocessor reset out	A6	-
UPWR--LT	Microprocessor write	A6	-
UPWR-1LT	Microprocessor write 1	A25	A25
VBOTA	Variable backward output A	A25	A55
VBOTB	Variable backward output B	A25	A55
VGDAØØ...11	Variable gain data A ØØ...11	A25	A25
VGDBØØ...11	Variable gain data B ØØ...11	A25	A25

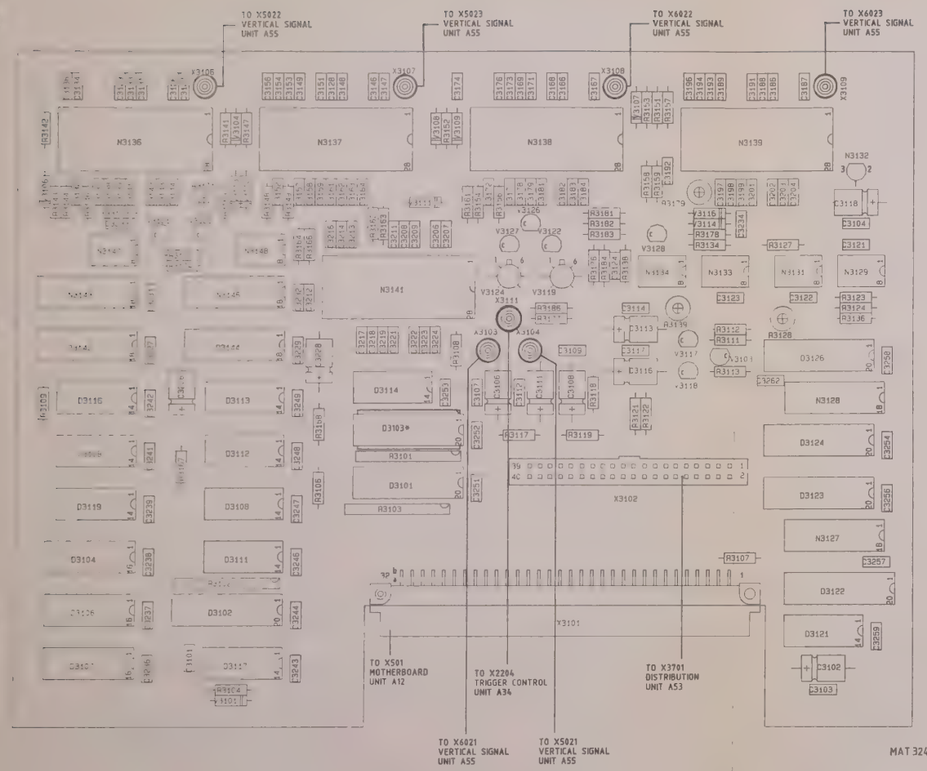
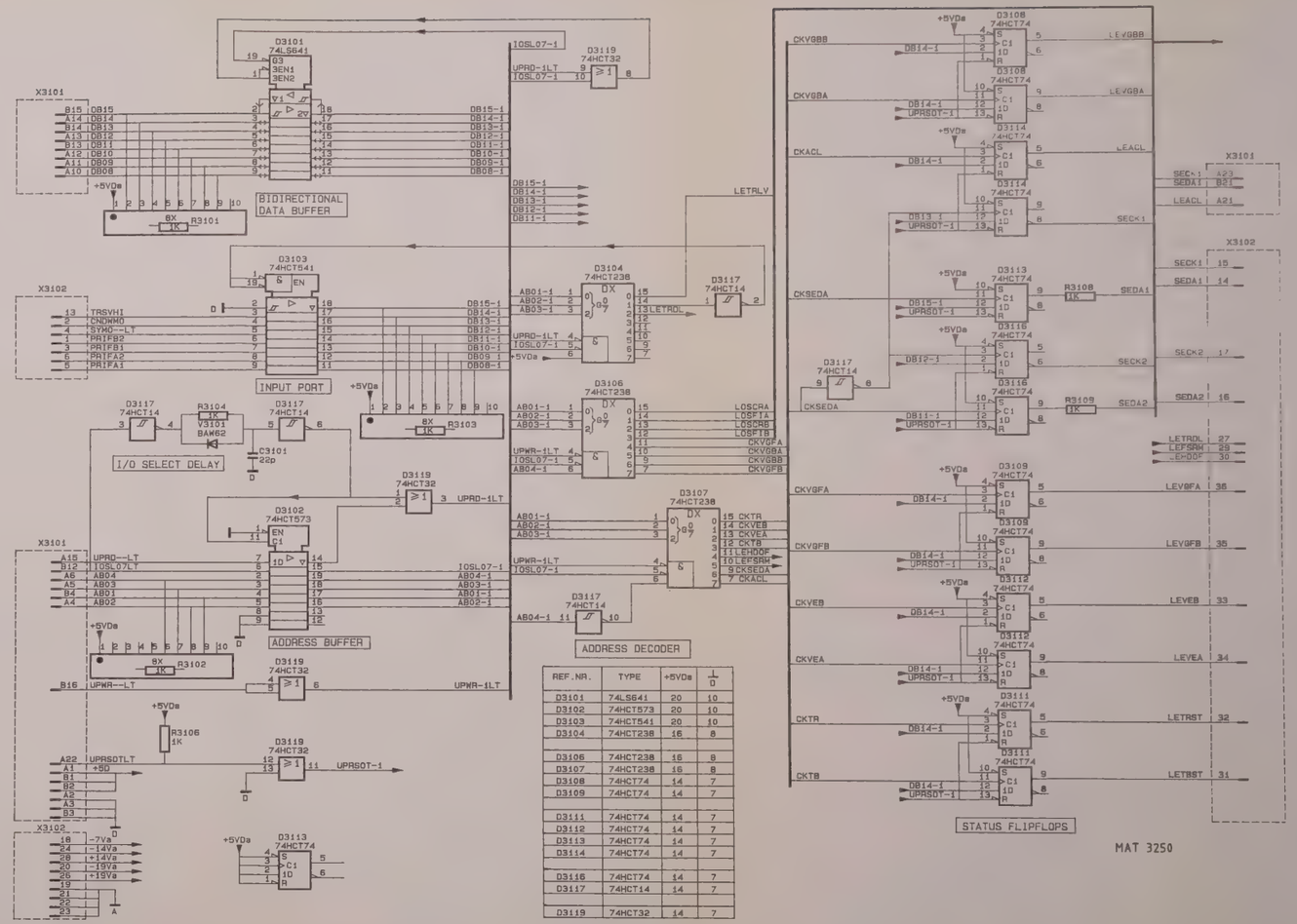
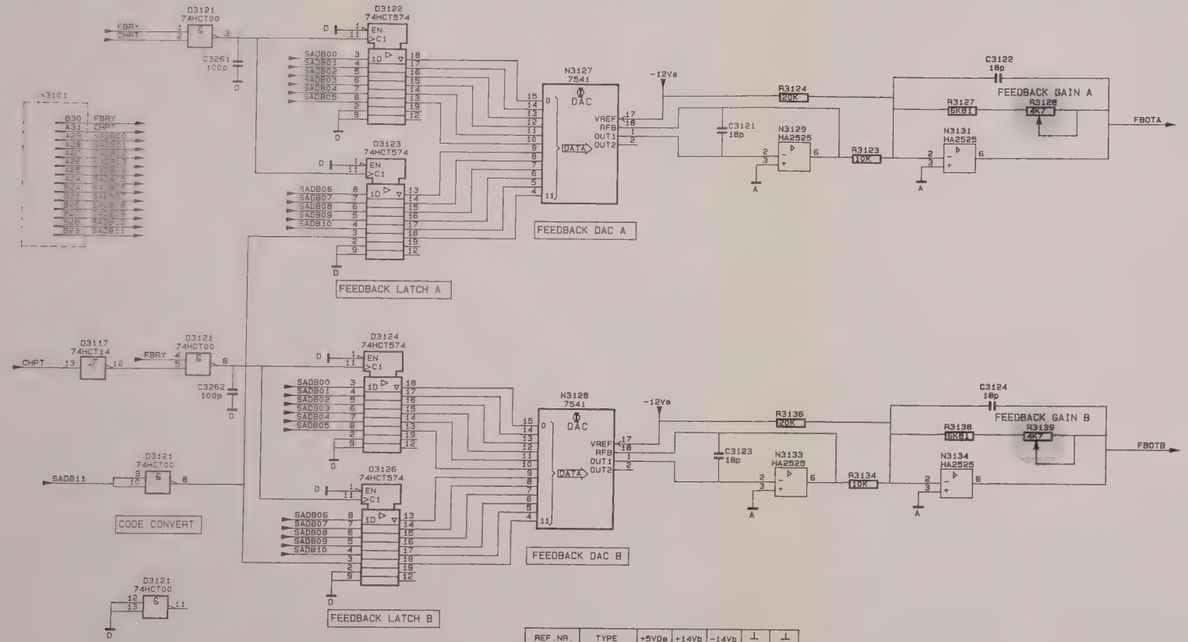


Figure 8.25.1 Unit A25 - MANAGEMENT UNIT - p.c.b. lay-out.

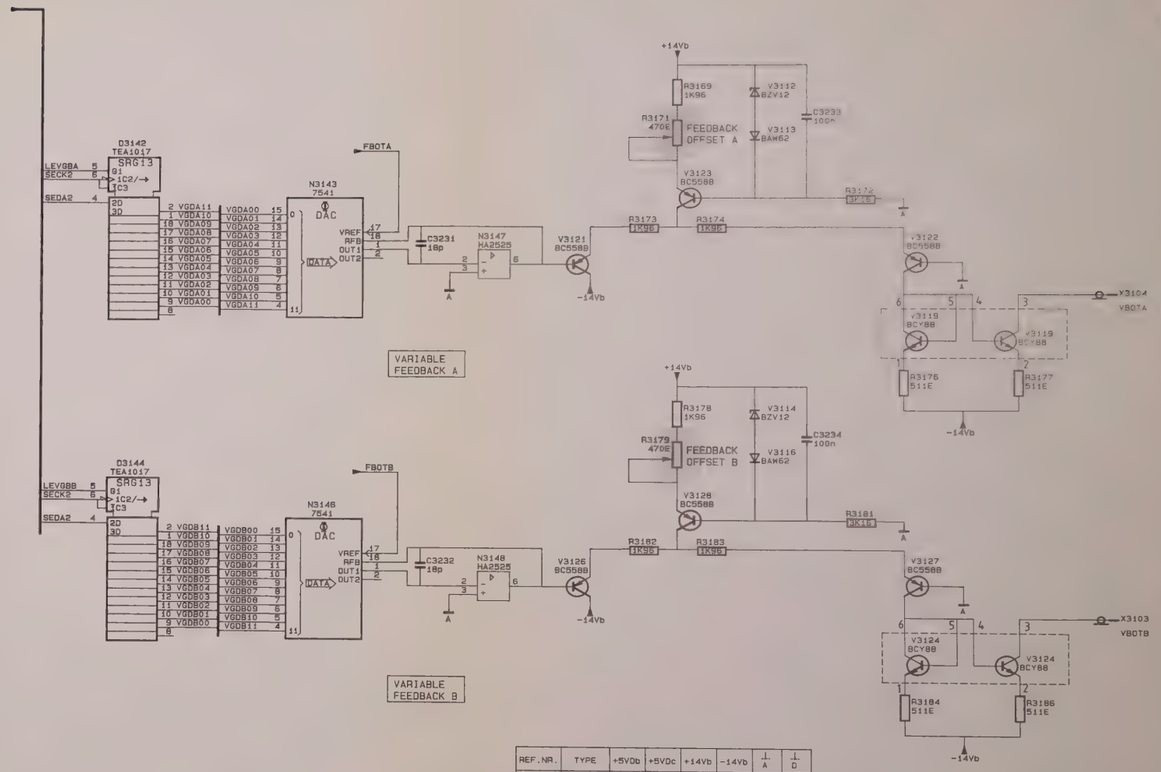


REF.NR.	TYPE	+5VDa	⏚
D3101	74LS641	20	10
D3102	74HCT573	20	10
D3103	74HCT541	20	10
D3104	74HCT238	16	8
D3106	74HCT238	16	8
D3107	74HCT238	16	8
D3108	74HCT74	14	7
D3109	74HCT74	14	7
D3111	74HCT74	14	7
D3112	74HCT74	14	7
D3113	74HCT74	14	7
D3114	74HCT74	14	7
D3116	74HCT74	14	7
D3117	74HCT14	14	7
D3119	74HCT32	14	7

Figure 8.25.2 Unit A25 - MANAGEMENT UNIT - circuit diagram.

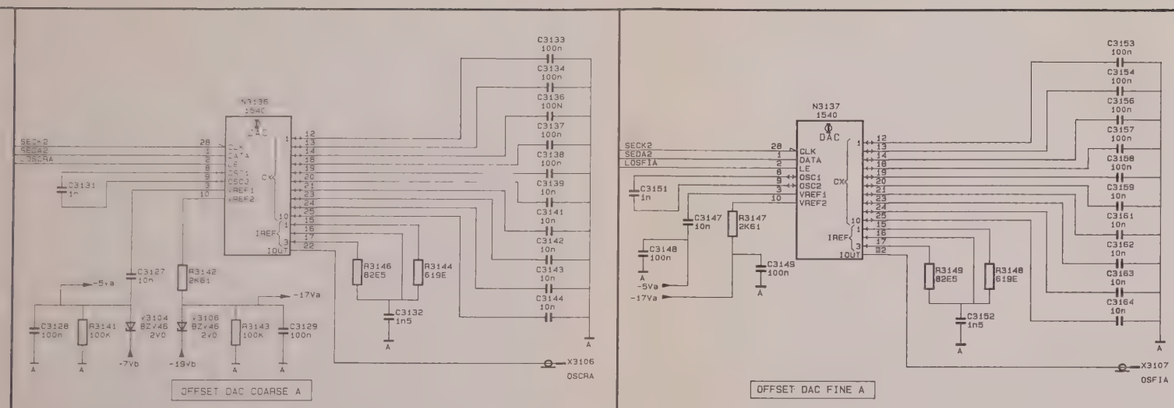


REF.NR.	TYPE	+5VDa	+14Vb	-14Vb	⊥ A	⊥ D
D3122	74HCT574	20				10
D3123	74HCT574	20				10
D3124	74HCT574	20				10
D3126	74HCT574	20				10
D3127	AD7541		16		3	
D3128	AD7541		16		3	
D3129	HA2525		7	4		
D3131	HA2525		7	4		
D3133	HA2525		7	4		
D3134	HA2525		7	4		



REF.NR.	TYPE	+5VDb	+5VDc	+14Vb	-14Vb	⊥ A	⊥ D
D3142	TEA1017		7				3
D3144	TEA1017	7					3
N3143	AD7541			16		3	
N3146	AD7541			16		3	
N3147	HA2525			7	4		
N3148	HA2525			7	4		

Figure 8.25.3 Unit A25 - MANAGEMENT UNIT - circuit diagram.

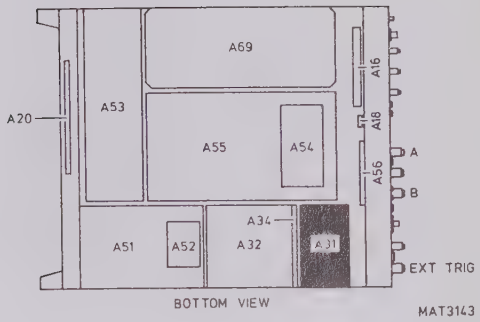


REF.NR.	TYPE	+5VDa	-5Va	-5Vb	-17Va	-17Vb	⊥/D
N3136	TDA1540	4	7		11		6
N3137	TDA1540	4	7		11		6
N3138	TDA1540	4		7		11	6
N3139	TDA1540	4		7		11	6

REF.NR.	TYPE	+5VDa	-5Vc	-17Vc	⊥/D
N3141	TDA1540	4	7	11	6

Figure 8.25.4 Unit A25 - MANAGEMENT UNIT - circuit diagram.

UNIT A31 - TRIGGER INPUT UNIT



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8.31.3 Signal name list..... 8.31-2

8.31.1 General information

The Trigger Input unit amplifies the signals from both trigger pick offs and the external trigger signal. The trigger source selection is also performed on this unit. Finally the prescaler for the Count Down mode can be found on this unit.
This unit is built up with S.M.D. technology.

8.31.2 Circuit description

The PRE-AMPLIFIER/SELECTOR amplifies one of the two trigger pick off signals (TRPO-A or TRPO-B), depending on the position of relay K1301 and K1302.
The amplified signal at the output of N1302 has the same amplitude as the corresponding input signal of the oscilloscope.
Relay K1303 selects between an external trigger source or channel A or B.
All trigger signals are terminated with 50 ohm, when they are not used.
The coils L1301 and L1302 filter low frequency resonances of the trigger pick offs, which might cause false triggers.
The AMPLIFIER X1/X10 amplifies the trigger signal 10 times in trigger sensitivity high mode. If relay K1304 is activated, the amplifier is bridged.

The PRESCALER, which is only active if relay K1305 is not activated, divides frequency of the trigger signal by 128. The output signal is a square wave. Because its frequency is much lower as the input signal, trigger level control on the edges results in a good trigger level range on the input signal.
It consists of a pre-amplifier (N1306 and N1307), followed by a 2 GHz divide-by-2 stage (D1301) and a 1 GHz divide-by-64 stage. Transistor V1313 buffers the output signal.
The TRIGGER AMPLITUDE DETECTOR detects if the selected trigger signal has a level, which is equivalent to 40 mV at the input of the oscilloscope, with the X1/X10 AMPLIFIER switched on.
The signal to diode V1308 is rectified by this diode. If the signal amplitude increases the voltage at the node V1308 and R1357 goes more negative. If the treshold level is passed, the signal TRADOT goes high. This signal is applied to the Trigger Control unit A34.

Now pin 3 of divider D1302 is pulled high inside D1302, which enables the divider. If the input signal of the oscilloscope is too small, the TRADOT signal is low and the divider is not enabled and so there is no output signal at pin 7 of D1302.
Nevertheless the signal may be sufficiant in certain frequency ranges. Therefore the prescaler can be enabled by the ENPS--LT signal from the microprocessor.
The filter consisting of C1351, C1352 and L1312 adapts the detectors sensitivity to losses in the path between the instruments inputs and this detector.

NOTES:
- This board is made of a special material, which is suitable for very high frequencies. This material can be bended easily; so please handle carefully.
- IC D1301 is mounted topside down.
- If the relays are switching with a frequency higher than about 2 Hz, which only happens if there is something wrong in the instrument, the freewheel diodes inside the relays burn out. In this case the flatcable to this unit has to be disconnected, after which the fault can be traced.
- The relays can not be unsoldered. In case of a relay failure the board should be replaced.
- In the circuit diagrams the relays are drawn in there quiescent position.
- If an electrolytic capacitor in the coupling circuits between the various stages breakes down, the low pass cut off frequency rises significantly, which results in false triggers.
  If the board is OK the cut off frequency of the board itself is lower than 1 kHz. If one of the capacitors is broken this frequency rises to a frequency higher than 100 kHz.
- Above 1 GHz all amplification factors decrease.
- Sometimes multiple parallel resistors are used to spread dissipation.

8.31.3 Signal name list

UNIT 31

Signal name	Description	Signal source	Signal destination(s)
CNDWMOLT	Count down mode	A34	-
ENPS--LT	Enable prescaler	A34	-
EXT	External trigger signal	A57	-
ETTR	External triggering	A34	-
TR-A	Triggering channel A	A34	-
TR-B	Triggering channel B	A34	-
TRADOT	Trigger amplitude detector output	A31	A34
TRPO-A	Trigger pick off A	A56	-
TRPO-B	Trigger pick off B	A56	-
TRSG	Trigger signal	A31	A32
TRSG1	Trigger signal 1	A31	A31
TRSG2	Trigger signal 2	A31	A31
TRSG3	Trigger signal 3	A31	A31
TRSVHILT	Trigger sensitivity high	A34	-

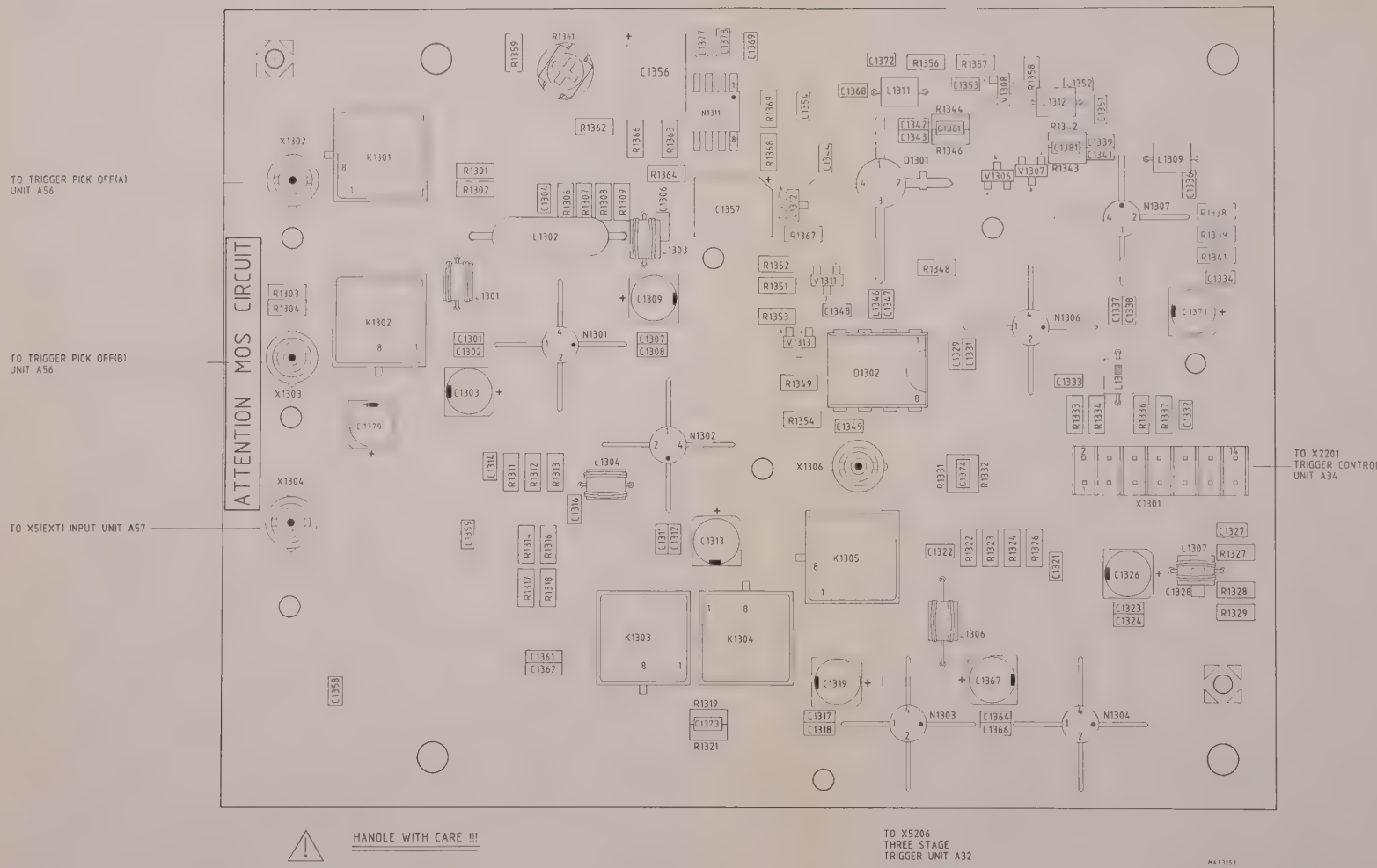
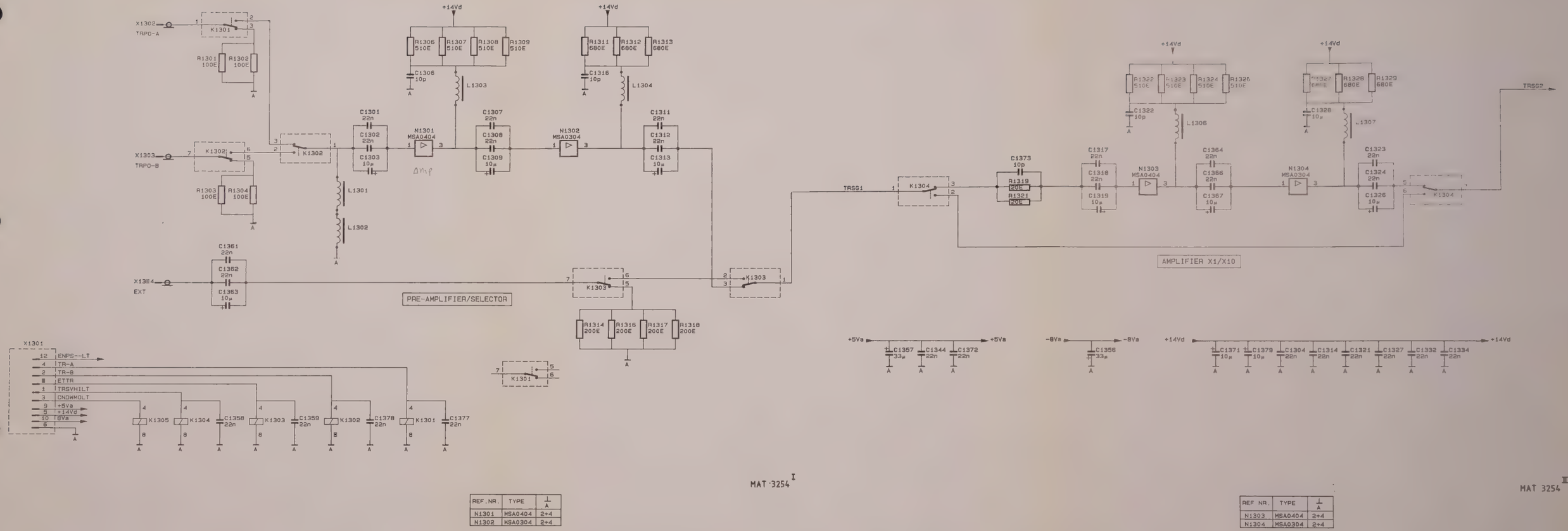


Figure 8.31.1 Unit A31 - TRIGGER INPUT UNIT - p.c.b. lay-out.



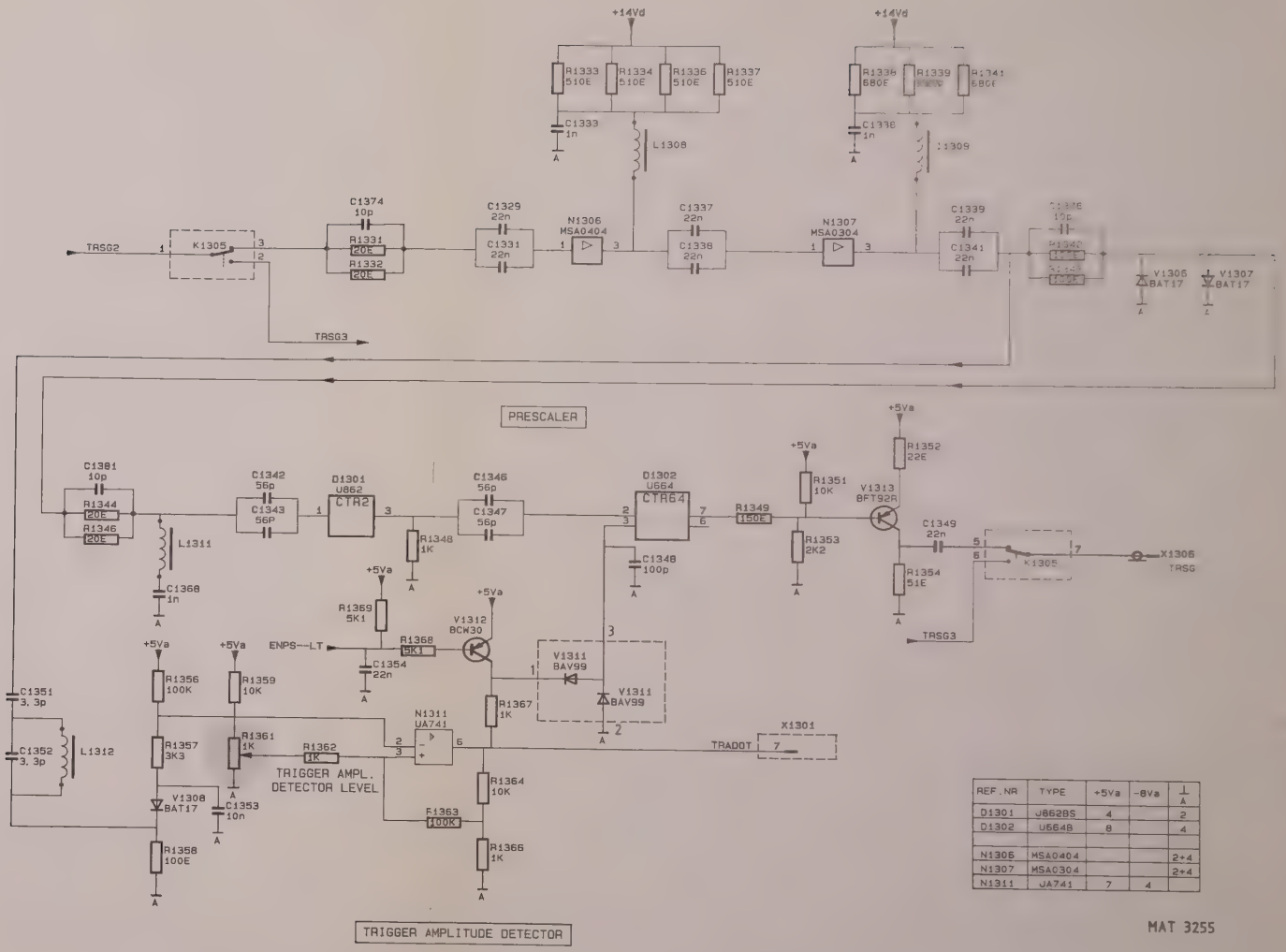
MAT 3254 I

REF. NR.	TYPE	⊥ A
N1301	MSA0404	2÷4
N1302	MSA0304	2÷4

MAT 3254 II

REF NR.	TYPE	⊥ A
N1303	MSA0404	2÷4
N1304	MSA0304	2÷4

Figure 8.31.2 Unit A31 - TRIGGER INPUT UNIT - circuit diagram.

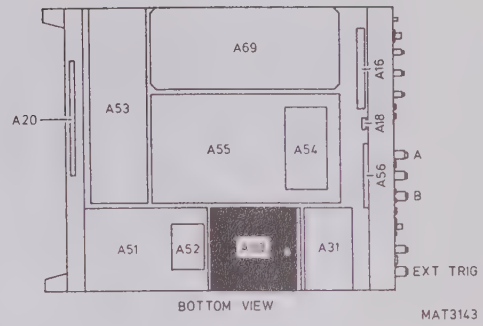


REF.NR	TYPE	+5Va	-8Va	⊥ A
D1301	U862BS	4		2
D1302	U664B	8		4
N1306	MSA0404			2+4
N1307	MSA0304			2+4
N1311	UA741	7	4	

MAT 3255

Figure 8.31.3 Unit A31 - TRIGGER INPUT UNIT - circuit diagram.

UNIT A32 - THREE STAGE TRIGGER UNIT



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8.32.1 General information..... 8.32-1
8.32.2 Three stage trigger circuit..... 8.32-1
8.32.3 Circuit description..... 8.32-4
8.32.4 Signal name list..... 8.32-6

8.32.1 General information

This unit consists of a trigger circuit that generates a trigger signal to start the fast ramp generator as the trigger signal crosses the trigger level with the correct slope and if the hold off time is elapsed. In the synchronised mode this signal is generated directly after the hold off time being elapsed. Furtheron, the units contains a filter amplifier for the trigger signal, followed by a number of divider stages. The output signals are applied to the trigger control circuit. The board is built up in SMD technology.

8.32.2 Three stage trigger circuit

The circuit consists of three schmitt trigger circuits (stages) in sequence (see figure 8.32.1).

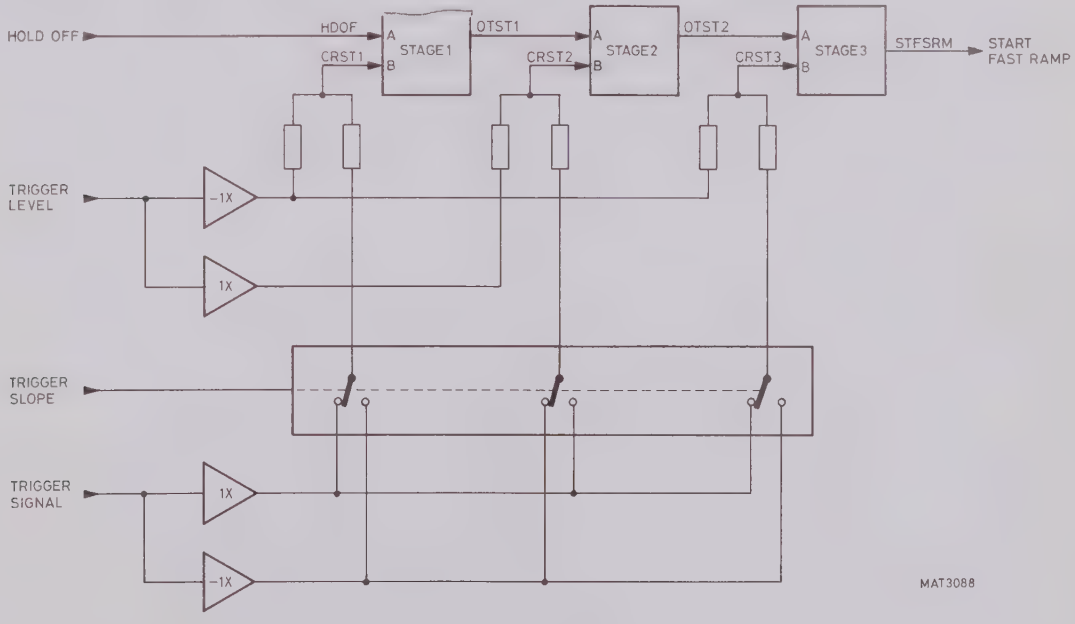


Figure 8.32.1 Block diagram of three stage trigger circuit.

Each stage has two inputs. Input B is non-inverting with a hysteresis. The output can only go high if input A is low.
A conventional trigger circuit consists only of one of these stages. If the hold off time is elapsed, the A input (HDOF) is low. As soon as the trigger signal passes the trigger level, the output of the schmitt trigger goes high to start the fast ramp. Due to propagation delay times in the circuit, a small time uncertainty may arise if HDOF goes low at the moment that the trigger signal crosses the trigger level. This time jitter is unacceptable in this instrument. Therefore three stages are used.
Stage 1 and stage 3 get the trigger signal minus the trigger level, while stage 2 gets the trigger level minus the trigger signal.
The timing diagram in figure 8.32 shows how the three stages change over behind each other after the falling edge of HDOF, with the trigger level set at zero.

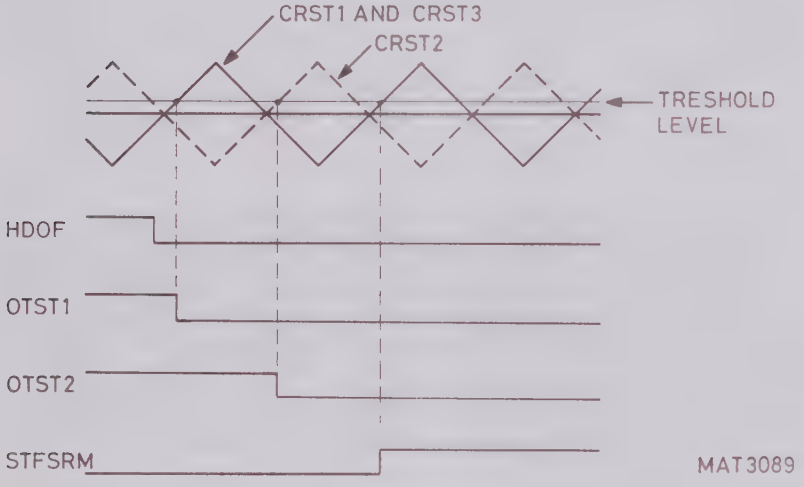


Figure 8.32.2 Timing diagram 1 of the three stage trigger circuit.

If HDOF goes low at the moment that CRST1 crosses the threshold level, or just a bit later, the signal OTST1 changes over immediately. Nevertheless OTST2 changes over almost a half period later. The same happens with STFSRM.

Figure 8.32.3 shows what happens if the trigger level is increased until triggering is just possible and HDOF goes low at the trigger moment. Now stage 1 changes over immediately at HDOF. If HDOF suffers from some jitter, the output of stage 1 will also jitter. Now stage 2 also suffers from some jitter, because it changes over just behind stage 1.
Nevertheless stage 3 changes over almost one period later, so this stage will not suffer from jitter and the fast ramp starts at a fixed moment.

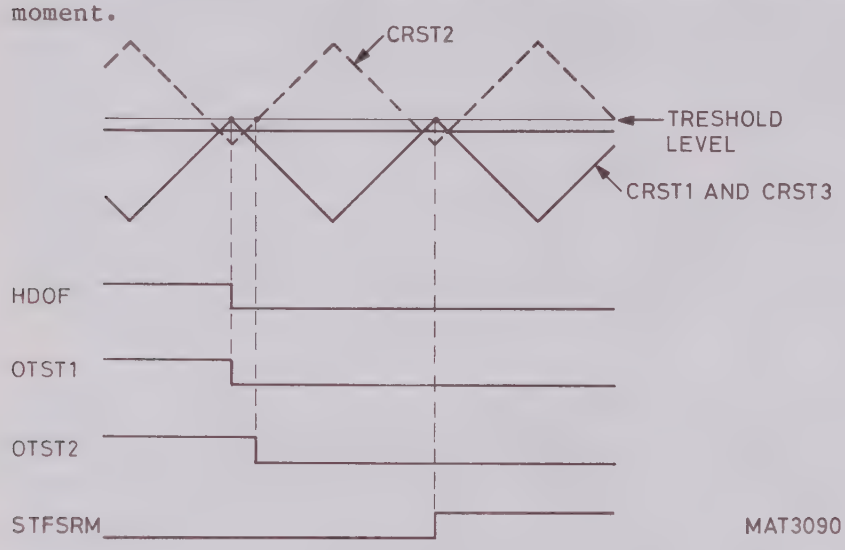


Figure 8.32.3 Timing diagram 2 of the three stage trigger circuit.

In synchronised mode all three stages should change over immediately behind each other when HDOF goes low.
This realised by some auxiliar circuits, which are not indicated in figure 8.32.1.
These circuits pull the B-inputs down. So after the falling edge of HDOF, all three stages change over immediately behind each other.
The edges of the HDOF signal are less steep in synchronised mode (see also section 8.51.3). On these slow rising/falling edges, the trigger signal is superimposed by another auxiliar circuit.
The change over of the three stages is now influenced by the trigger signal. This results is a synchronized mode with a lock range.
A signal which is displayed stable, remains stable in spite of minor changes in the hold off time, e.g. due to drift.

8.32.3 Circuit description

The circuits described in section 8.32.2 are realised with current controlled circuits.
As the three stage of the three stage trigger circuit are almost identical only STAGE 1 will be described.
The hart of the stage is a flip-flop circuit, consisting of transistors V5206, V5207, V5203 and V5204.
Furtheron there is an output buffer (V5212 and V5213) and a buffer in a positive feedback circuit (V5209 and V5211).
During the hold off time the status of the transistors is as given in the table below:

Conducts	Blocks
V5201	V5208
V5207	V5206
V5203	V5204
V5213	V5212
V5202	
V5211	V5209

After the hold off time, transistor V5201 blocks. The current which is sunk to CRST1 via diode V5257 depends on the trigger level and the trigger signal.
When the trigger signal passes the trigger level, transistor V5202 will block and all transistors will change over.
The positive feedback line via transistor V5211 speeds up the changing over and creates some hysteresis.

In SYNCHRONIZED MODE, signal SYSG is derived from the trigger signal and is coupled to the base of transistor V5208 via capacitor C5201. In this way it is added to the hold off signal HDOF to obtain a lock range. In the triggered mode there is a fixed DC level applied to capacitor C5201.

The LEVEL CONTROL circuit sinks a current, depending on the selected trigger level from the 3 control points of the stages (CRST1, CRST2 and CRST3). If the trigger level is increased, the current through X5207 (TRLV-1) to resistor R5298 increases. Therefore the voltage at measuring point X30 rises. The current which is sunk from CRST2 will increase and the currents from CRST1 and CRST3 will decrease. Note that the voltage at measuring point X29 remains constant.

The SYNC CONTROL B circuit sinks a current from CRST2 in SYNCHRONIZED MODE, because SYM0--LT is low.
Now STAGE 2 changes over immediately when OTST1 goes low.

Stage 3 has a different output stage, to control the FAST RAMP GENERATOR on the FAST RAMP UNIT A52.

The trigger signal (TRSG) from the TRIGGER INPUT unit A31 is buffered, amplified and split into symmetrical signals TRSG1 and TRSG2 by the BUFFER circuit around IC D5206. These two signals sink currents in the SLOPE CONTROL circuit from CRST1, CRST2 and CRST3 depending on the TRSP signal, according to the following table.

	TRSP	TRSG1	TRSG2
POS SLOPE	LOW	CRST2	CRST1+CRST2
NEG SLOPE	HIGH	CRST1+CRST2	CRST2

Furtheron the SLOPE CONTROL circuit has a potentiometer to adjust the trigger gap (R5397).

In synchronized mode, the SYNC CONTROL A circuit unbalances the BUFFER and the SLOPE CONTROL in such a way that STAGE 1 and STAGE 3 change over immediately after the falling edge of HDOF.
As already mentioned the SYNC CONTROL B circuit takes care that STAGE 2 changes over immediately.

The FILTER/AMPLIFIER amplifies and filters the trigger signal from the TRIGGER INPUT unit A31 and splits it into two symmectrical signals TRSGFL-1 and TRSGFL-2, which are applied to dividers.
The higher order filter cuts off frequencies above 175 MHz, which cannot be processed by the following hardware.
The DIVIDER HIGH AMPL consists of a schmitt trigger circuit (D5494, R5461 and R5462), followed by 4 divide-by-four stages.
The schmitt trigger gives an output signal if the input signal of the oscilloscope is 20 mVp-p or more (in SENS HIGH mode).
The DIVIDER LOW AMPL is similar to the DIVIDER HIGH AMPL. The schmitt trigger (D5494, R5458 and R5459) gives an output signal if the input signal of the oscilloscope is 10 mVp-p or more (in SENS HIGH mode).
The signal at pin 11 of IC D5498 is divided by two by another divider stage.
The dividers are built up with ECL circuits.
The three output buffers (D5499) convert the signals to TTL level, resulting in TRSGHA, TRSGLA and TRSGLA-2, which are routed to the TRIGGER CONTROL UNIT A34.

In synchronized mode, the SYNC CONTROL C amplifies the filtered trigger signal from the transistor in D5204 (pin 2) and applies at as signal SYSG to STAGE 1, where it is added to the hold off signal, to obtain a lock range for the synchronized mode. In triggered mode SYSG is at fixed DC level.

Note: This unit forms together with the Time-base unit A51 and the Fast Ramp unit A52 a closed loop (see also figure 8.51.1). When a unit hangs up the loop can be opened by disconnecting the coax cable at X5202 (HDOF).
By applying a square wave of 1 kHz with an amplitude of 400 mVp-p symmetrically around zero to X5202 the correct operation of these units can be checked, if an input signal is present to generate triggers.

8.32.4 Signal name list

UNIT 32

Signal name	Description	Signal source	Signal destination(s)
CRST1	Control stage 1	A32	A32
CRST2	Control stage 2	A32	A32
CRST3	Control stage 3	A32	A32
HDOF	Hold off	A52	-
OTST1	Output stage 1	A32	A32
OTST2	Output stage 2	A32	A32
STFSRMHX	Start fast ramp	A32	A52
STFSRMLX	Start fast ramp	A32	A52
SYMO--LT	Synchronized mode	A34	-
SYSG	Synchronize signal	A32	A32
TRVL-1	Trigger level 1	A34	-
TRSG	Trigger signal	A31	-
TRSG1	Trigger signal 1	A32	A32
TRSG2	Trigger signal 2	A32	A32
TRSGFL-1	Trigger signal filtered 1	A32	A32
TRSGFL-2	Trigger signal filtered 2	A32	A32
TRSGHA	Trigger signal high amplitude	A32	A34
TRSGLA	Trigger signal low amplitude	A32	A34
TRSGLA-2	Trigger signal low amplitude 2	A32	A34
TRSP	Trigger slope	A34	-

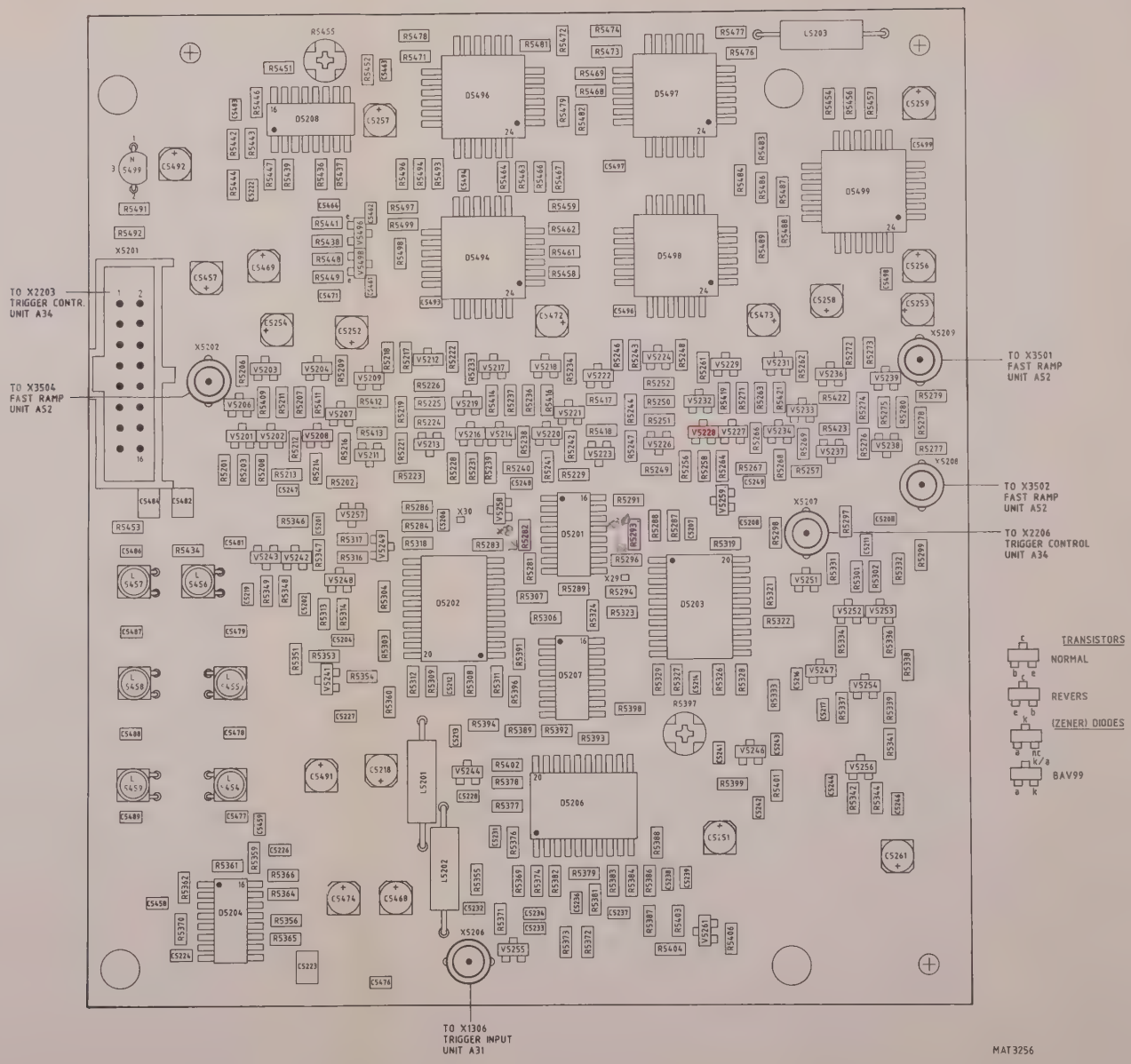


Figure 8.32.4 Unit A32 - THREE STAGE TRIGGER UNIT - p.c.b. lay-out.

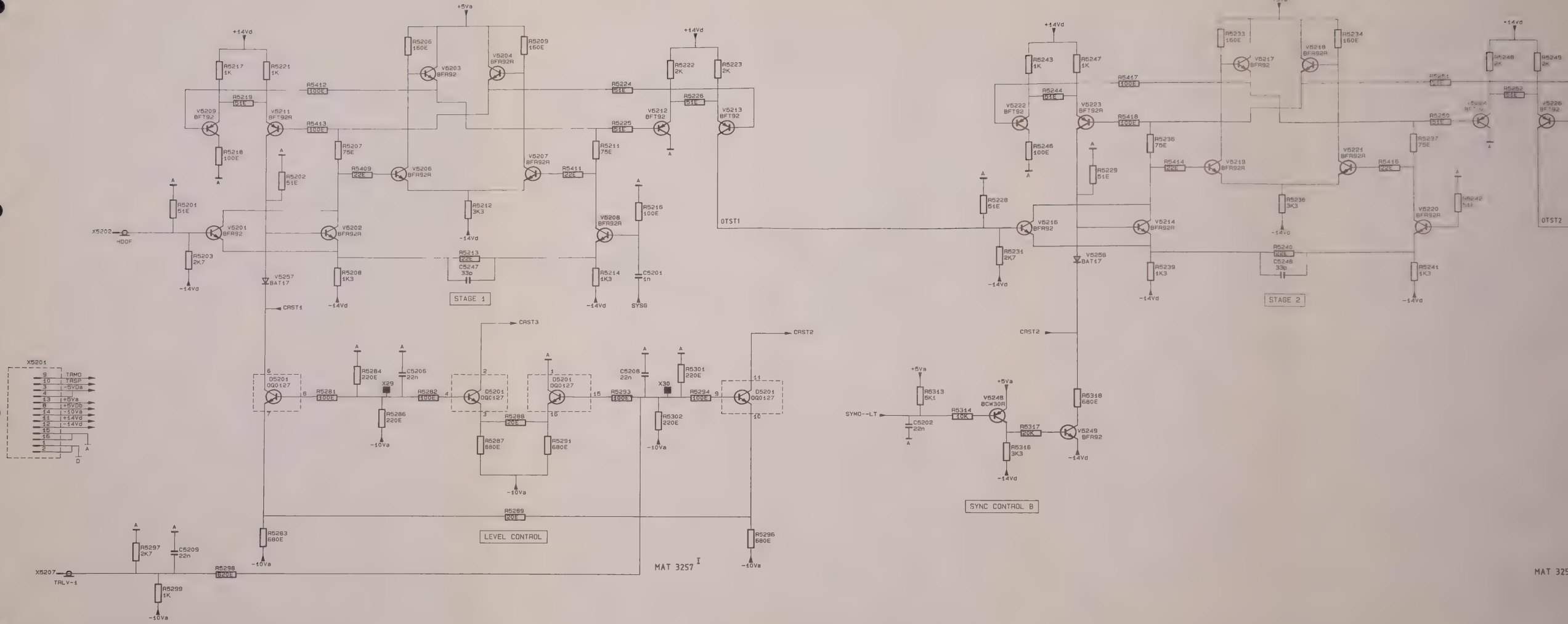
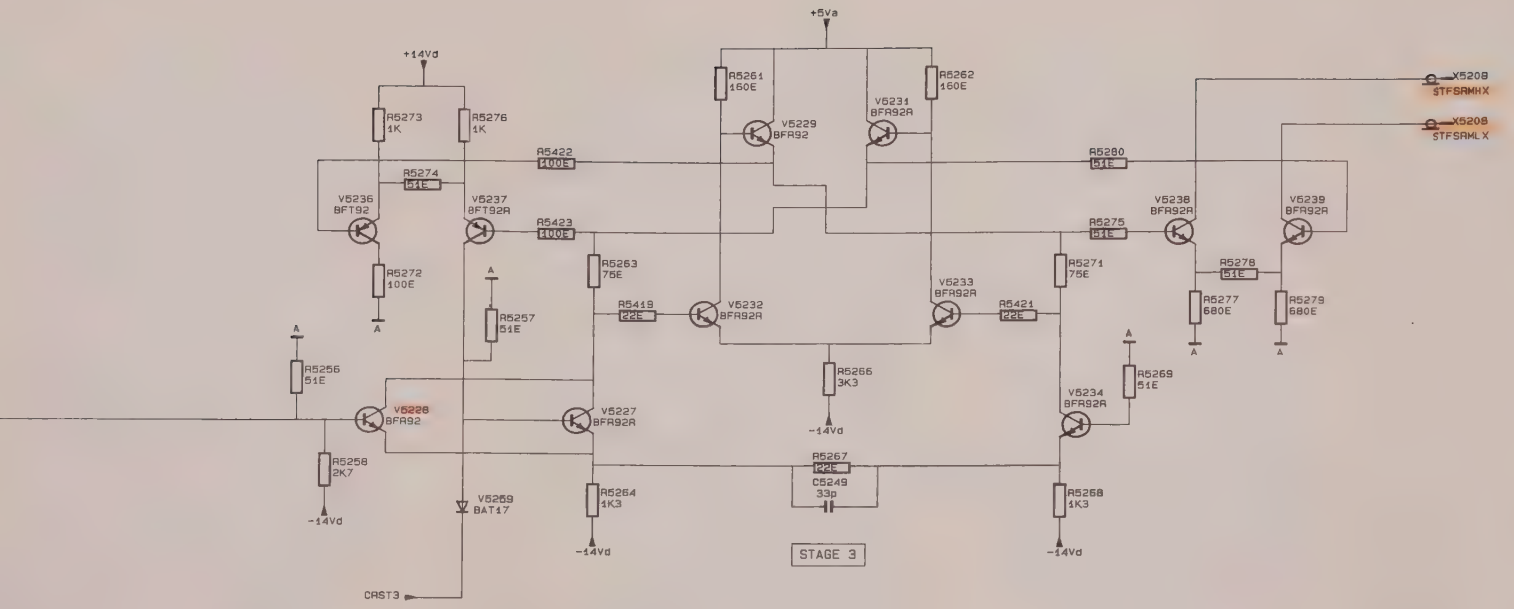
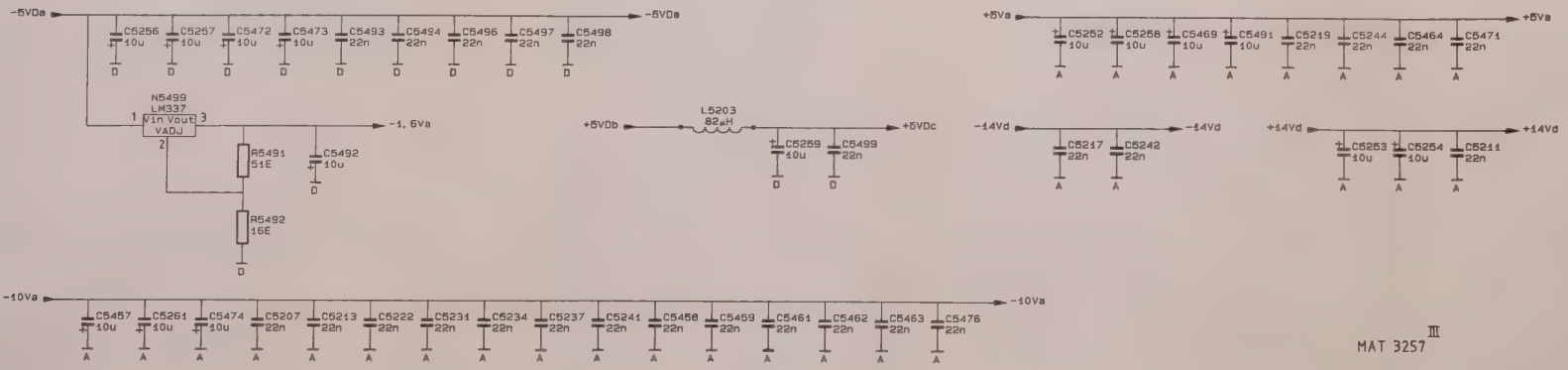


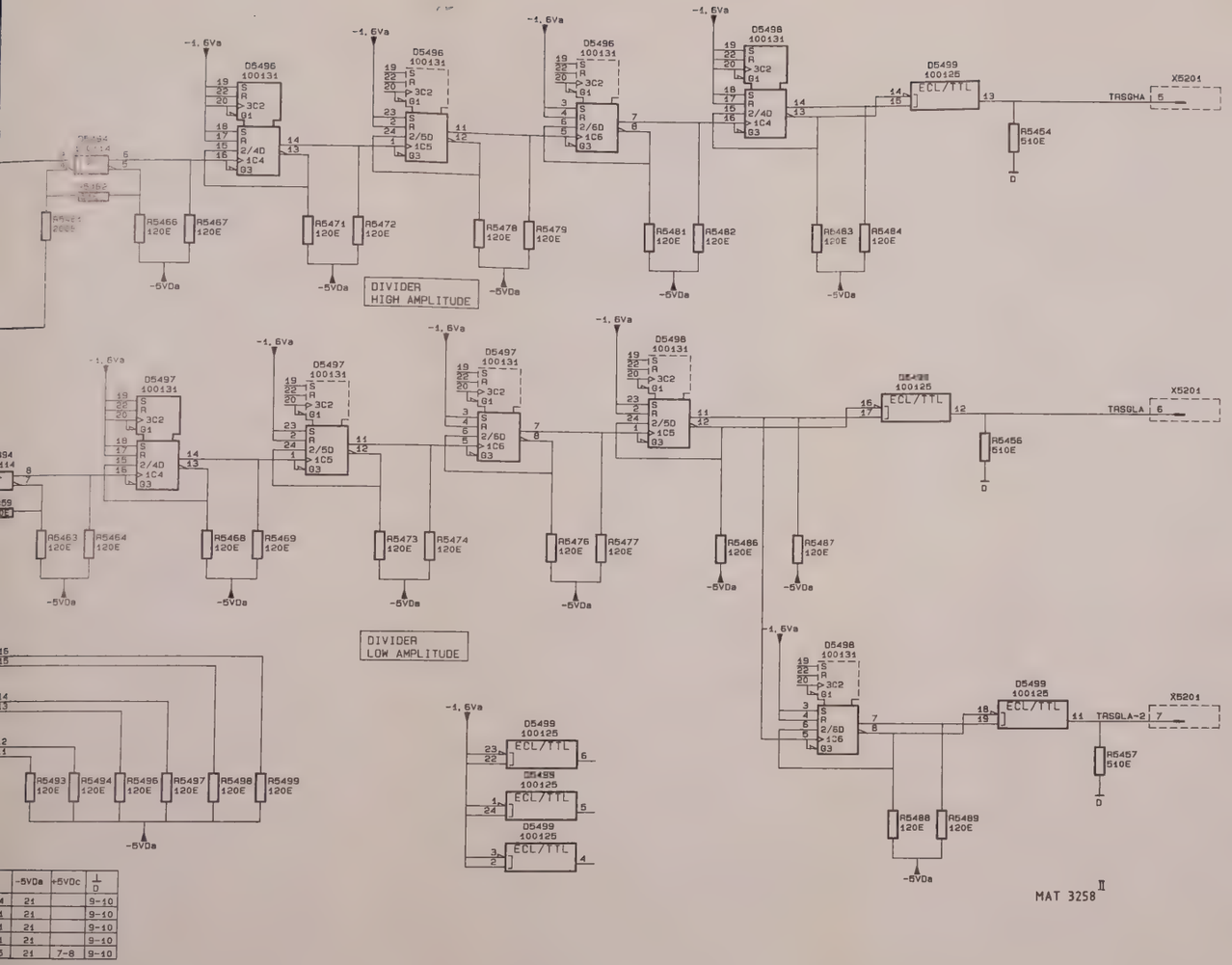
Figure 8.32.5 Unit A32 - THREE STAGE TRIGGER UNIT - circuit diagram.





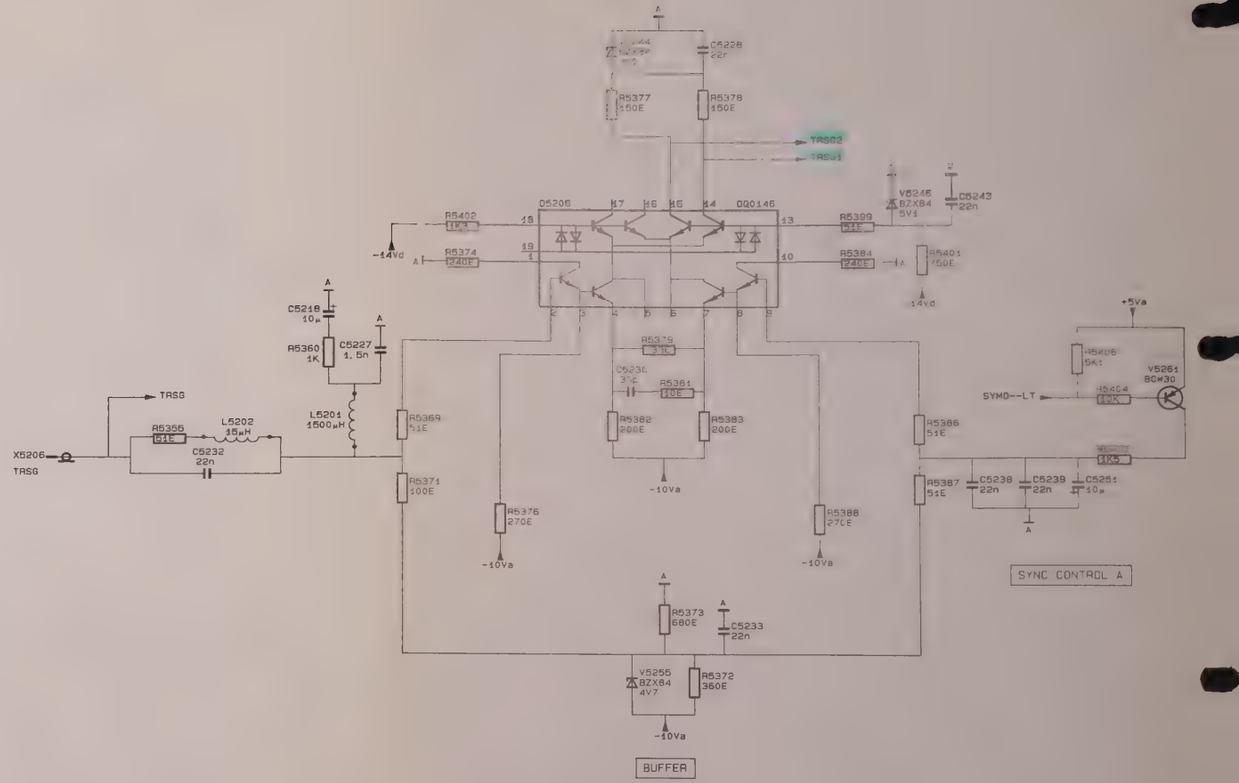
MAT 3257 III

8



	-5VDa	+5VDc	
4	21		9-10
4	21		9-10
1	21		9-10
1	21		9-10
5	21	7-8	9-10

MAT 3258 II



MAT 3259

Figure 8.32.7 Unit A32 - THREE STAGE TRIGGER UNIT - circuit diagram.

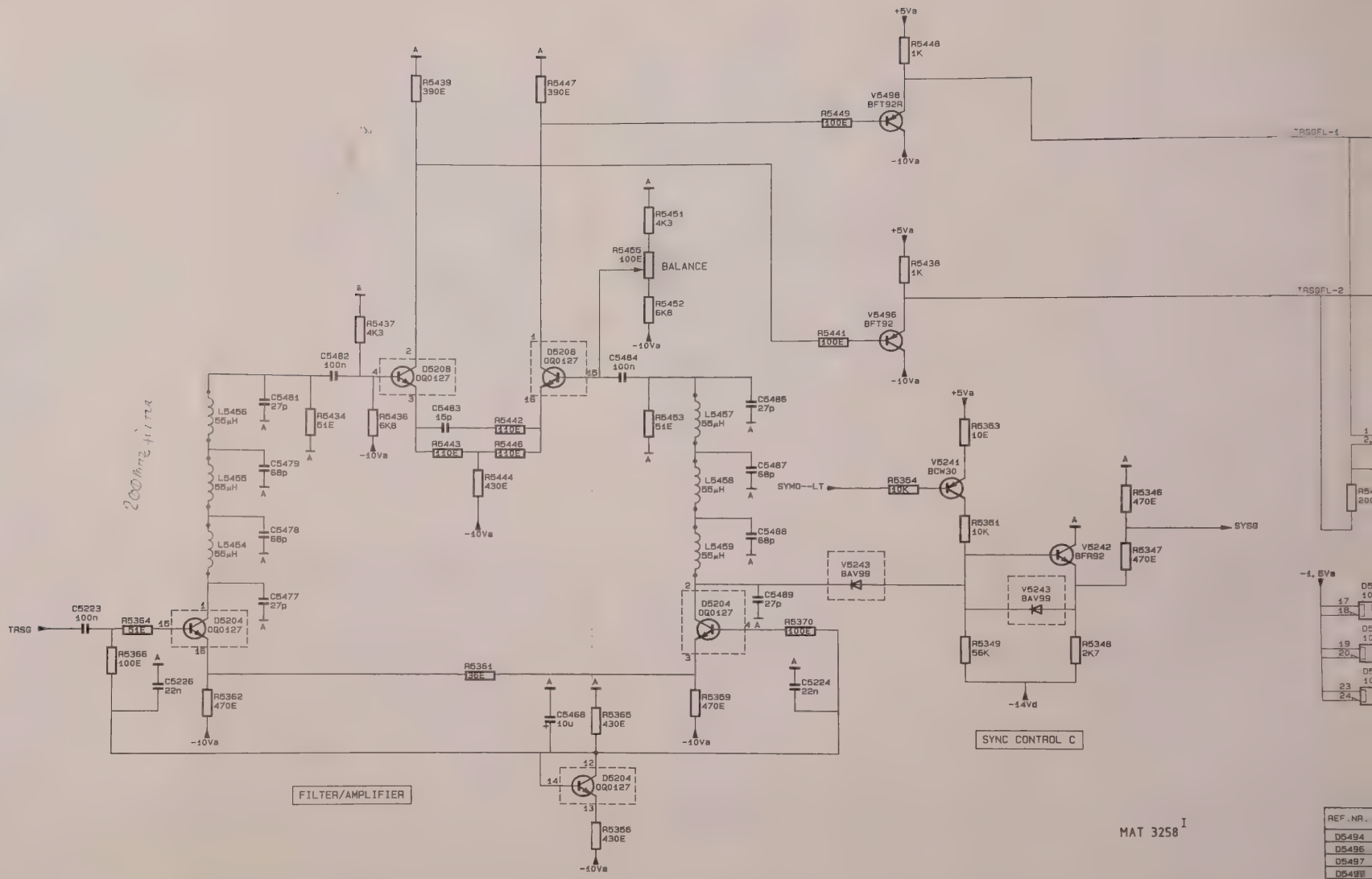
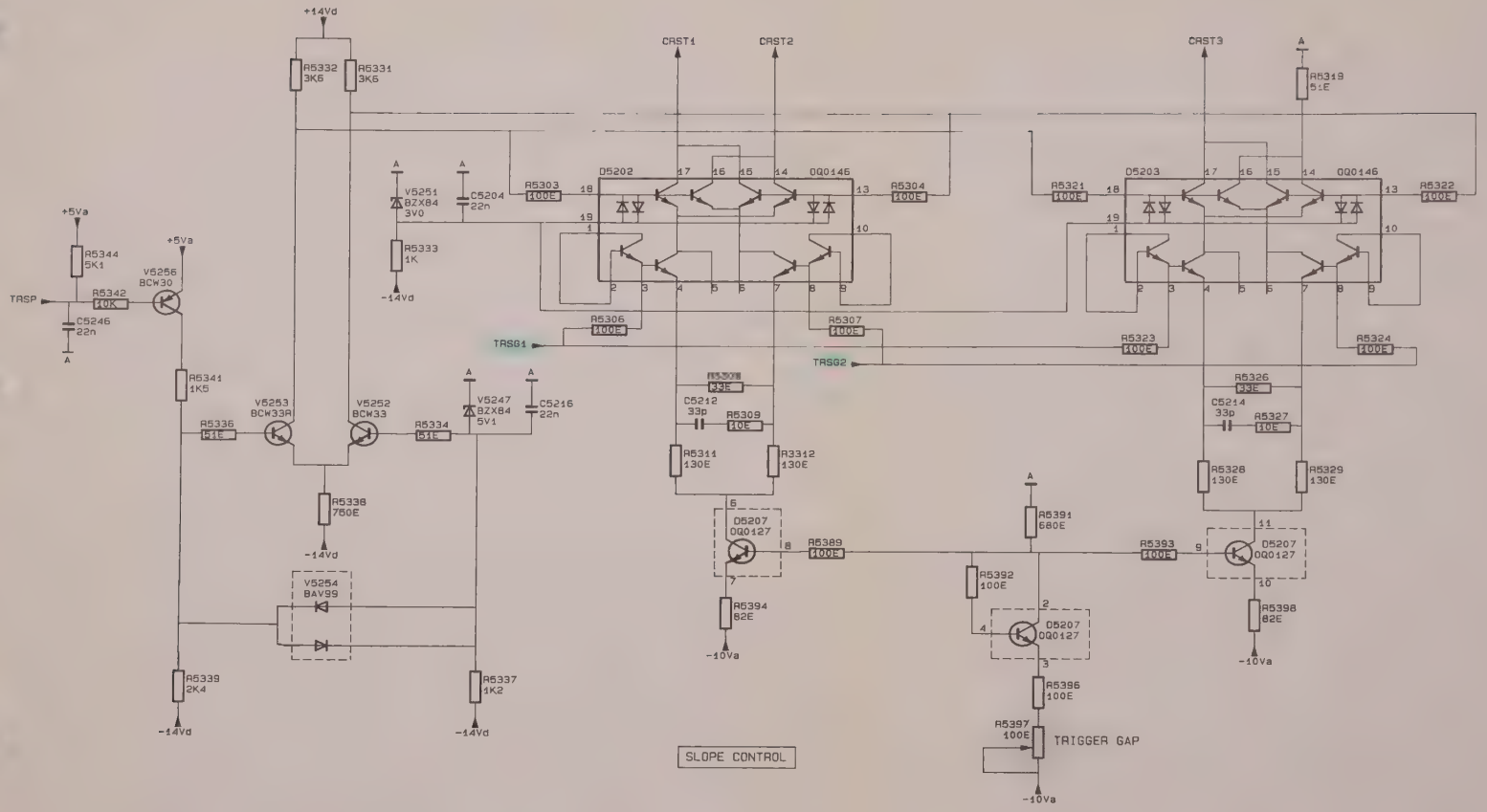


Figure 8.32.6 Unit A32 - THREE STAGE TRIGGER UNIT - circuit diagram.

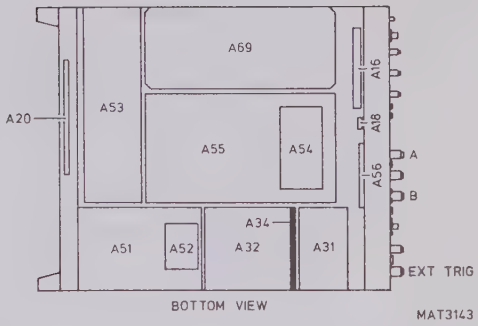


MAT 3260

Figure 8.32.8 Unit A32 - THREE STAGE TRIGGER UNIT - circuit diagram.

8

UNIT A34 TRIGGER CONTROL UNIT



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8.34.2 Principle of operation..... 8.34-1
8.34.3 Circuit description..... 8.34-2
8.34.4 Signal name list..... 8.34-4

8.34.1 General information

This unit controls the various trigger modes in this instrument, as well in manual select as in auto select mode.
Furtheron, this unit contains a trigger level adaption circuit, which is switched between the Management unit and the Three Stage Trigger unit.

8

8.34.2 Principle of operation

Figure 8.34.1 shows the principle of operation of the trigger control.

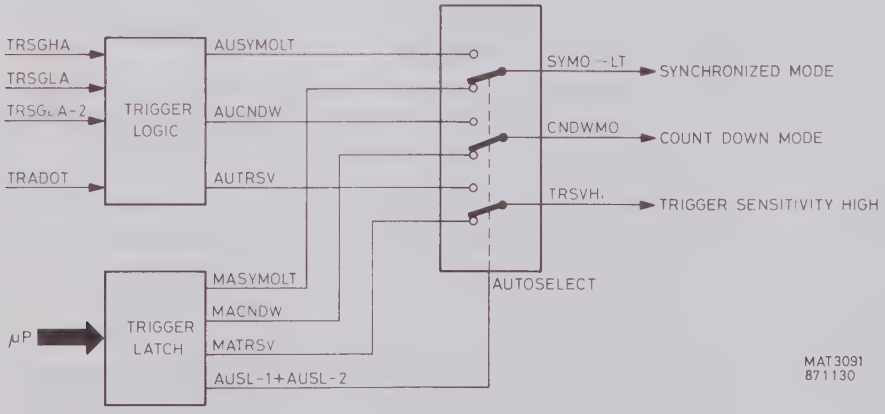


Figure 8.34.1 Principle of trigger control.

Three signals (SYMO--LT, CNDWMO, TRSVHI) control the trigger mode. If AUTO SELECT is not selected, the switch, which is a multiplexer, is in the drawn position. The trigger mode is now determined by the signals from the microprocessor: MASYMOLT, MACNDW and MATRSV.
If AUTO SELECT is selected, the multiplexer is changed over by the microprocessor via the AUSL-1 and AUSL-2 signals. Now the trigger mode is determined by the AUSYMOLT, AUCNDW and AUTRSV signals, which come from the trigger logic.
To detect the desired trigger mode, depending upon the input signal of the instrument, the trigger logic gets 3 signals from Three Stage Trigger unit A32 (TRSGHA, TRSGLA and TRSGLA-2) and the TRADOT signal from the Trigger Input unit A31.

8.34.3 Circuit description

The trigger logic consists of the UPPER FREQUENCY DETECTOR, THE LOWER FREQUENCY DETECTOR, the TRIGGER MODE CONTROL and the COUNTDOWN CONTROL.
If TRIGGER SENSITIVITY HIGH is selected and the input signal has a level of more then 10 mV, then the signal TRSGLA-2 is a square wave with the frequency of the input signal, divided by 32.
In TRIGGERED mode, the signal ENUFD (D2217 pin 6 and D2209 pin 1) is high, so the signal TRSGLA-2 is divided by 25 by the dividers in IC D2211.
So the frequency at pin 9 of D2211 is the frequency of the input signal, divided by 800 (32x25). This signal is applied to the UPPER FREQUENCY DETECTOR. This circuit consists of three monostable multivibrators and some logic. Each monostable multivibrator generates a pulse on its activating edge. If the frequency of the input signal passes above 160 MHz, the signal AUCNDW at pin 3 of D2204 goes high. The frequency determinating elements are C2242, R2212 and R2220. With the latter the frequency limit can be adjusted.
In COUNT DOWN mode the signal TRSGLA-2 is a square wave with the frequency of the input signal divided by 4096. In this mode the signal ENLFD (D2217 pin 5 and D2209 pin 4) is high, so the signal is applied to the LOWER FREQUENCY DETECTOR. This circuit is built up in a similar way as the UPPER FREQUENCY DETECTOR.
If the frequency of the input signal goes below 150 MHz, the signal AUCNDW at pin 3 of D2204 goes low. The frequency determinating elements are C2246, R2216 and R2225. With the latter the frequency limit can be adjusted.
The AUCNDW signal is applied to the COUNT DOWN CONTROL. Depending on the status of AUSL-2 the signal MACNDW or AUCNDW determines CNDWMO. Via transistor V2202, the PRESCALER on the Trigger Input unit A31 is activated in COUNT DOWN mode.
In AUTO SELECT mode, the instrument automatically switches over to COUNT DOWN mode if the frequency of the input signal passes above 160 MHz and switches back if the frequency passes below 150 MHz.
Because the sensitivity in COUNT DOWN mode is lower due to the PRESCALER on the Trigger Input unit A31, there might be no more trigger signal detected (no square wave at TRSGLA-2). Next the instruments switches back to TRIGGERED mode; detects a too high frequency, switches back to COUNT DOWN mode, etc.

This unstable situation is prevented by the circuit around gate D2208 (pin 8, 9 and 10), transistor V2211 and flipflop D2206.
If the instrument switches back to TRIGGERED mode, the flipflop is set and the DICNDWLT signal prevents via D2204 pins 13, 11, 1, 2 and 3 that AUCNDW goes high again. The flipflop is reset via the signal AUSL-2 if AUTO SELECT is deselected or selected again.
The TRIGGER mode control detects if TRIGGERED mode or SYNCHRONIZED mode should be selected in AUTO SELECT mode, depending on the frequency of the input signal. It also detects if the TRIGGER SENSITIVITY should be HIGH or LOW.
If the input signal has a level of more than 10 mV then TRSGLA is a square wave. If the level rises above 20 mV, TRSGHA is also a square wave. In both situations TRIGGER SENSITIVITY is assumed to be HIGH.
If SYMO--LT is low, the signal TRSGHA passes via D2207 pins 12 and 11, else TRSGLA passes via D2202 pins 2 and 3. The following circuit detects if a square wave is present at D2212 pin 3, which results in the signals AUTRSV and AUSYMOLT.
Depending on the status of AUSL-1, the signal MATRSV or AUTRSV determines TRSVHI. Via transistor V2201, the X1/X10 AMPLIFIER on the Trigger Input unit A31 is activated if TRSVHI is high.
The signal AUSL-1 also determines if SYMO--LT is determined by MASYMOLT or AUSYMOLT.

The TRIGGER LATCH is a shift register, which latches a number of trigger status signals, which come from the microprocessor via the Management unit A25.

The TRIGGER LEVEL ADAPTION buffers the trigger level current from the MANAGEMENT unit A25. The output current is applied to the Three Stage Trigger unit A32. With potentiometer R2232, the trigger level offset can be adjusted.

8.34.4 Signal name list

UNIT 34

Signal name	Description	Signal source	Signal destination(s)
AUCNDW	Auto count down mode	A34	A34
AUSL-1	Auto select 1	A34	A34
AUSL-2	Auto select 2	A34	A34
AUSYMOLT	Auto synchronized mode	A34	A34
AUTRSV	Auto trigger sensitivity	A34	A34
CNDWMO	Count down mode	A34	A34, A51-A53-A25
CNDWMOLT	Count down mode	A34	A31
DICNDWLT	Disable count down	A34	A34
ENLFD	Enable lower frequency detector	A34	A34
ENPS--LT	Enable prescaler	A34	A32
ENUFD	Enable upper frequency detector	A34	A34
ETTR	External triggering	A34	A31
LETRST	Latch enable trigger status	A25	-
MACNDW	Manual count down	A34	A34
MASYMOLT	Manual synchronized mode	A34	A34
MATRSV	Manual trigger sensitivity	A34	A34
SECK1	Serial clock 1	A25	-
SEDA1	Serial data 1	A25	-
SYMO--LT	Triggered mode	A34	A32,A51, A51-A53-A25
TR-A	Triggering channel A	A34	A31
TR-B	Triggering channel B	A34	A31
TRADOT	Trigger amplitude detector output	A32	-
TRLV	Trigger level	A34	-
TRLV-1	Trigger level 1	A34	A32
TRMORSLT	Trigger mode reset	A34	A34
TRSGHA	Trigger signal high amplitude	A32	-
TRSGLA	Trigger signal low amplitude	A32	-
TRSGLA-2	Trigger signal low amplitude 2	A32	-
TRSP	Trigger slope	A34	A32
TRSVHI	Trigger sensitivity high	A34	A51-A53-A25
TRSVHILT	Trigger sensitivity high	A34	A31

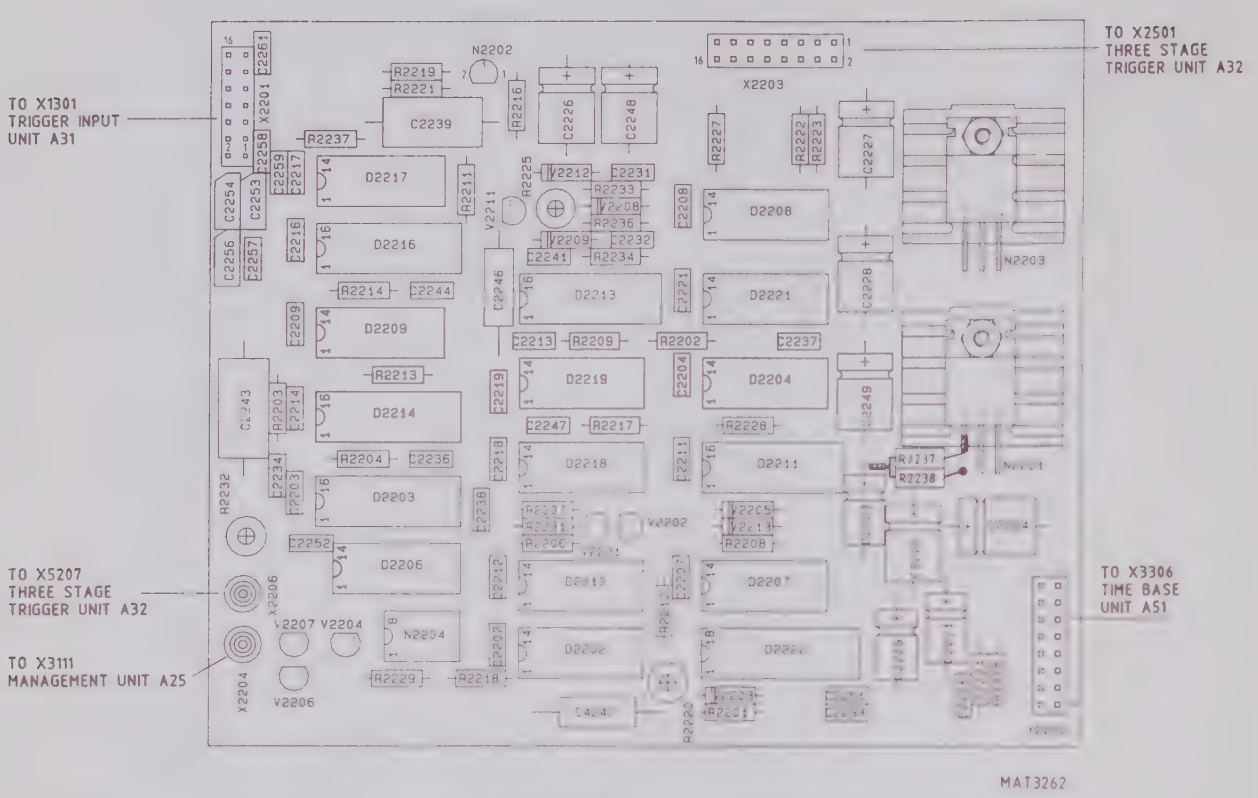
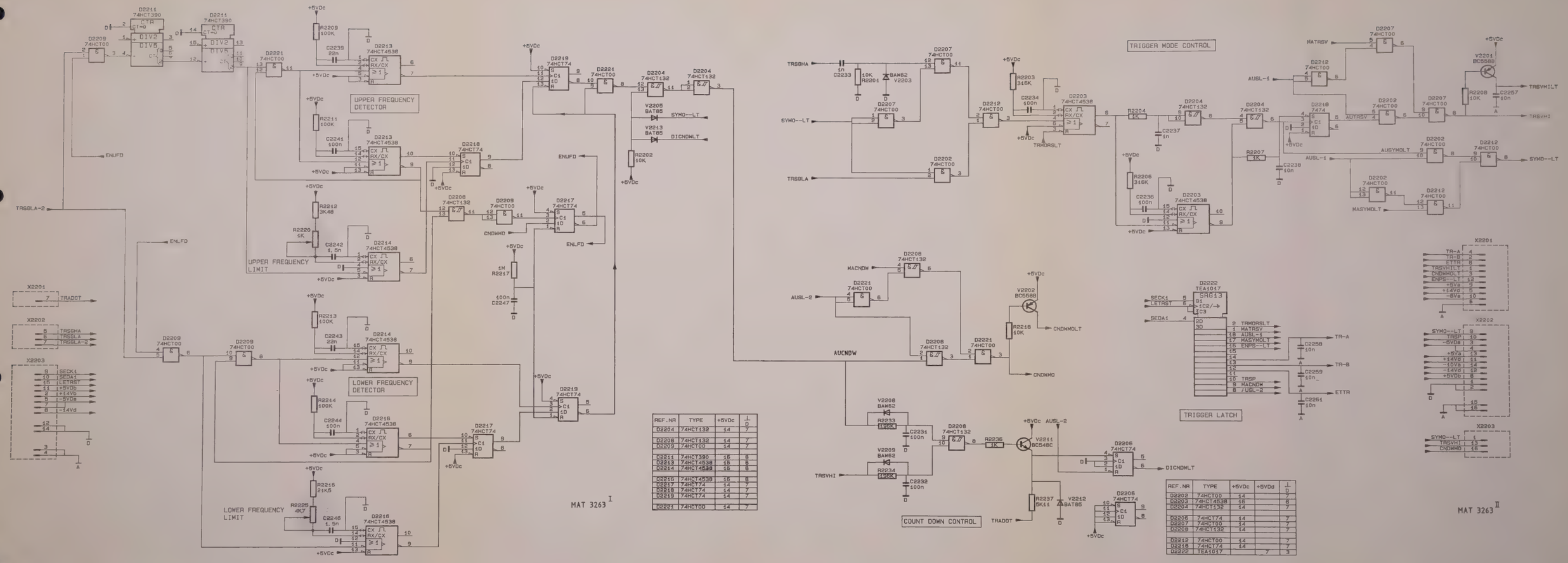


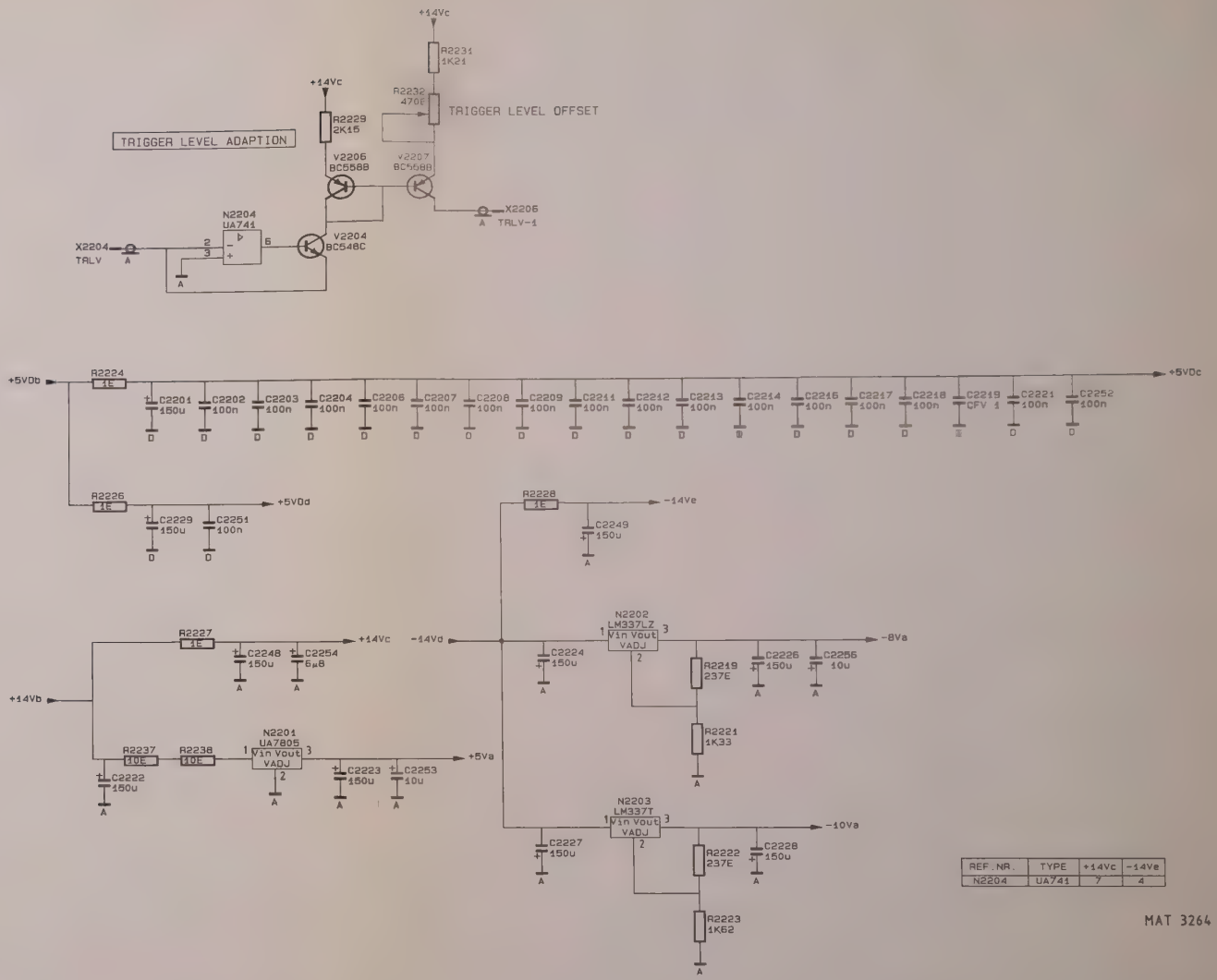
Figure 8.34.2 Unit A34 - TRIGGER CONTROL UNIT - p.c.b. lay-out.



REF.NR	TYPE	+5VDc	⊥
D2204	74HCT132	14	7
D2208	74HCT132	14	7
D2209	74HCT00	14	7
D2211	74HCT390	16	8
D2213	74HCT4538	16	8
D2214	74HCT4538	16	8
D2216	74HCT4538	16	8
D2217	74HCT74	14	7
D2218	74HCT74	14	7
D2219	74HCT74	14	7
D2221	74HCT00	14	7

REF.NR	TYPE	+5VDc	+5VDd	⊥
D2202	74HCT00	14		7
D2203	74HCT4538	16		8
D2204	74HCT132	14		7
D2205	74HCT74	14		7
D2207	74HCT00	14		7
D2209	74HCT132	14		7
D2212	74HCT00	14		7
D2216	74HCT74	14		7
D2222	TEA1017		7	3

Figure 8.34.3 Unit A34 - TRIGGER CONTROL UNIT - circuit diagram.



REF.NR.	TYPE	+14Vc	-14Ve
N2204	UA741	7	4

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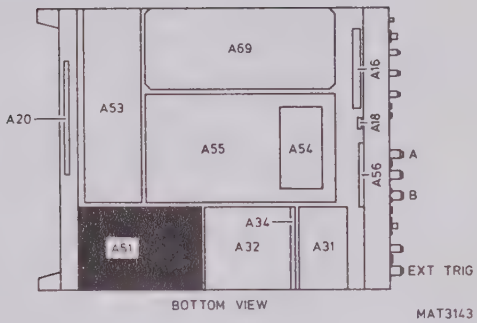
Figure 8.34.4 Unit A34 - TRIGGER CONTROL UNIT - circuit diagram.

UNIT A51 - TIME-BASE UNIT



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8.51.3 Fast ramp generator..... 8.51-2
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8.51.1 General information

In this section the Fast Ramp unit A52 is also described.
The main function of the Time-base unit and the Fast Ramp unit is the generation of sampling pulses for the Gate unit.
The TRIGGER DELAY function and the HOLD OFF function are also performed on these units.
The Fast Ramp unit A52 is built up with S.M.D. technology.

8.51.2 Functional description

Figure 8.51.1 gives a simplified block diagram of units A51 and A52 and their environment.
At the start of a scan the STAIR COUNTER is reset, so the output voltages of the STAIR DAC and the STAIR ATTENUATOR are 0 Volt.
If no trigger delay is selected, the output voltage of the TRIGGER DELAY DAC is 0 volt. So the staircase voltage behind the ADD INVERT circuit (STOT--XA) is 8 volt, because -8 Volt is added.
The TRIGGER DELAY DAC, the STAIR COUNTER, the STAIR DAC, the STAIR ATTENUATOR and the ADD INVERT circuit form the stair generator.
The start level of the FAST RAMP GENERATOR is 8 volt (FSRMOT--XA).
After a trigger this voltage goes down. Now the FAST RAMP/STAIR COMPARATOR will generate immediately a sampling pulse to the SAMPLING GATEs on unit A54 and to the ACQUISITION CONTROL LOGIC (A.C.L.) on unit A5.
The A.C.L. gives on its turn a count pulse to the STAIR COUNTER toincrease the staircase voltage with 8 mV.
Meanwhile the output voltage of the fast ramp generator crosses the final level, which results in a signal from the END OF FAST RAMP COMPARATOR to the HOLD OFF TIMER. Also the FAST RAMP GENERATOR is reset to 8 volt. Because the stroke of the fast ramp is constant, the total hold off time remains constant.

The HOLD OFF TIMER blocks trigger pulses via the Three Stage Trigger unit A32. When the hold off time is passed the trigger pulses are released again and the next incoming trigger pulse will start the fast ramp.
Now the sampling pulse comes later because the stair case voltage is lower than 8 volt. Therefore the sample is taken a while later on the input signal.
When 512 samples are taken the scan is complete and the A.C.L. is reset by the DPU. Next the A.C.L. resets the STAIR COUNTER. Now the output voltage of the stair generator, which was arrived at about 4 volt, is set to zero.
Other time-base settings are realised by adapting the steepness of the fast ramp.
Because the stair generator covers a range of 4 volt only half the fast ramp voltage range is used.
To obtain a trigger delay, the TRIGGER DELAY DAC gives for example a voltage of 4 volt, which results in a stair case voltage of 4 volts at the start of a scan. Because the fast ramp starts at 8 volts, a trigger delay of 10 divisions is obtained.
To obtain longer trigger delays, the output voltage of the STAIR DAC is attenuated by the STAIR ATTENUATOR and the steepness of the fast ramp voltage is decreased.

8.51.3 Fast ramp generator

Figure 8.51.2 shows a simplified diagram of the FAST RAMP GENERATOR.

The FAST RAMP GENERATOR is built around the time-base capacitors C3504 and C3506.
It consists of three current sources, which are in a closed loop.
The fast ramp current from transistor V3324 on unit A51 is led into the resistors R3361 and R3362. The resulting voltage controls two current sources, one around opamp N3317 and one around opamp N3318.
Because R3361, R3362, R3364, R3366 and R3371 have all the same value, the transistor V3509 sinks 4x the fast ramp current and V3327 sinks 2x the fast ramp current.
The latter current is doubled in a similar way as just described by the current source around opamp N3319, because R3372, R3373 and R3374 have the same value. So transistor V3506 supplies 4x the fast ramp current.
To stabilise the loop, a set current is sinked by a current source around transistor V3328. Transistor V3513 will sink 2x this set current to achieve a stable situation.
The balanced pair transistors V3513 and V3514 will make the voltages on their bases equal. The voltage on the base of V3513 is equal to the voltage on the time-base capacitors C3504 and C3506 via the buffer consisting of FET V3512 and transistor V3505. In this way the start level of the time-base capacitors is controlled by potentiometer R3384.

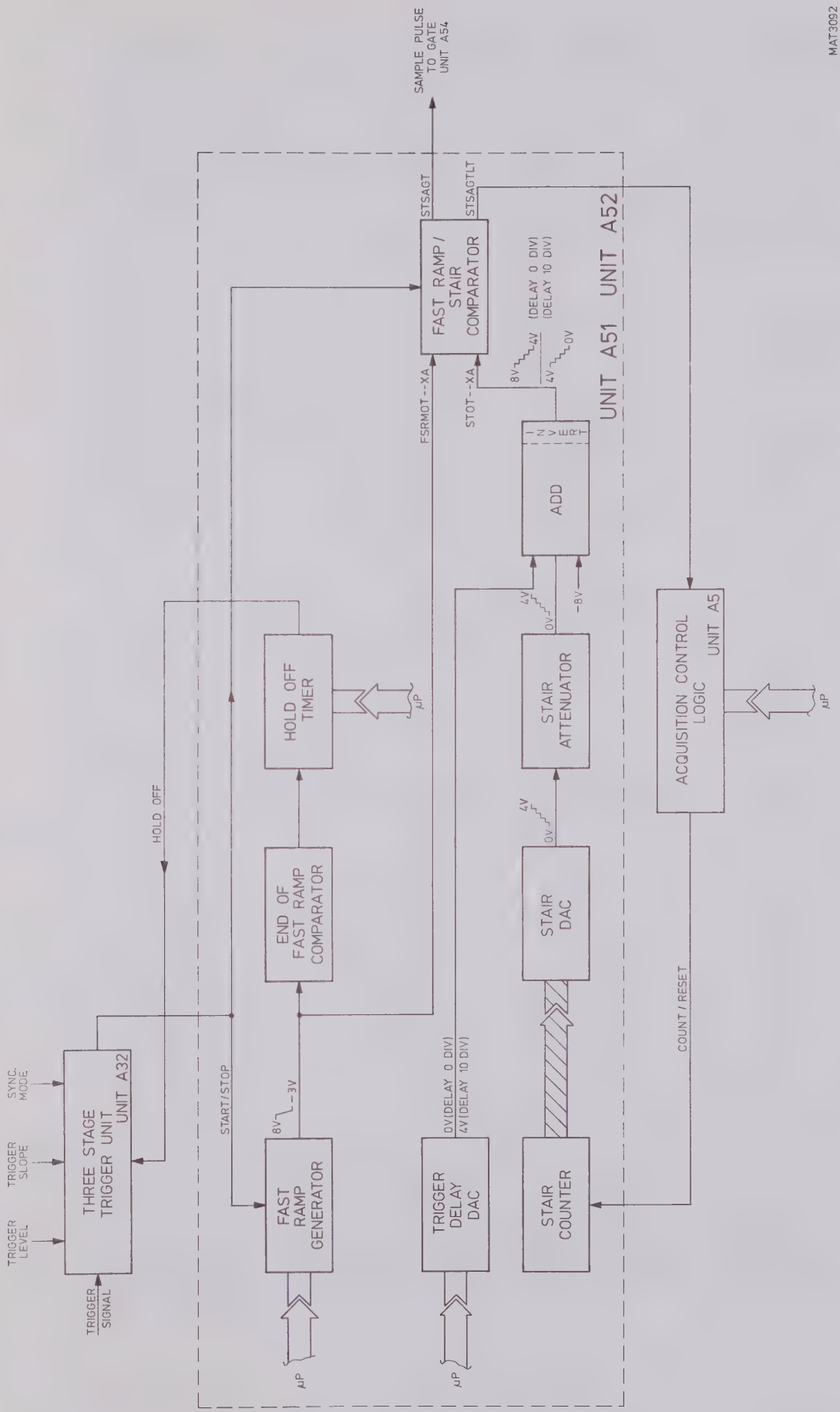


Figure 8.51.1 Block diagram of Time-base unit and Fast Ramp unit.

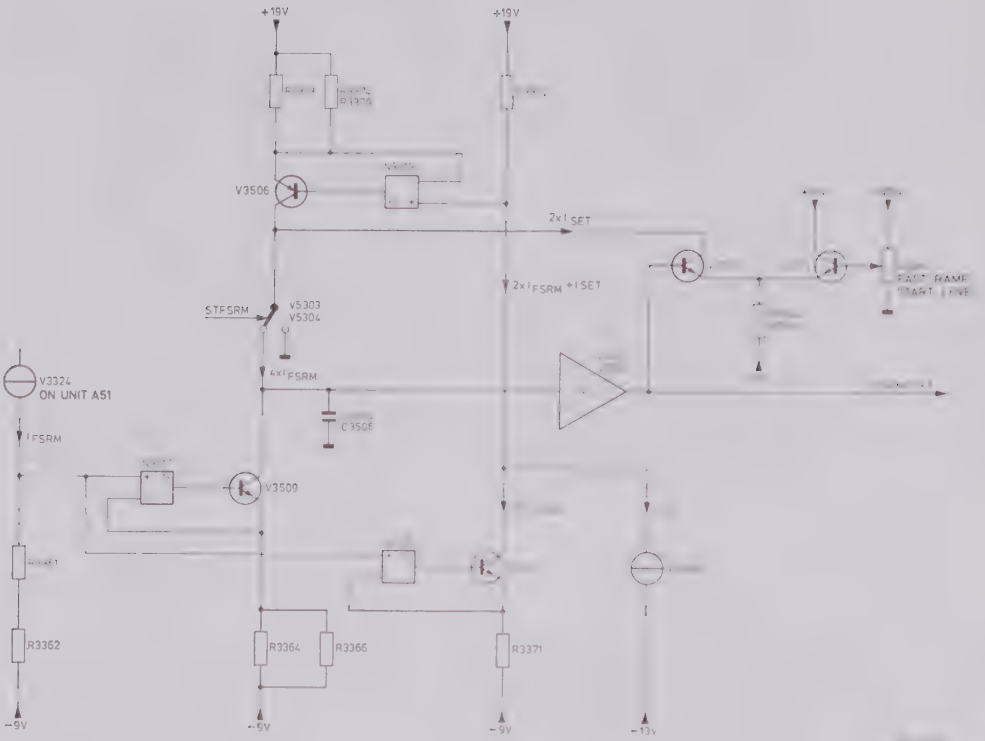


Figure 8.51.2 Block diagram fast ramp generator.

After a trigger, the STFSRM signal changes over the switch, consisting of transistors V3503 and V3504.
Now the current from transistor V3506 is led to ground and the current, which is sinked by transistor V3509 discharges the time-base capacitors linearly.
The signal FSRMOTXA is a decreasing fast ramp. When the signal crosses the end level, the hold off time starts. Now the switch of transistors V5303 and V3504 is reset via the THREE STAGE TRIGGER unit A32 and the time-base capacitors are charged again to the start level.

8.51.4 Circuit description

The FAST RAMP DAC is a serial DAC (N3313), which gets its data from the microprocessor via the Management unit A25. The output current at pin 22 is amplified by the circuitry around opamps N3314, N3316 and transistors V3323 and V3324.
The output current FSRMCU controls the steepness of the fast ramp of the FAST RAMP GENERATOR, which is described in the previous section. The slope of the fast ramp can be fine adjusted with C3506.

In the time-base settings 200 ns/div...20 us/div, capacitors C3508, C3509 and C3510 are switched parallel to the capacitors C3504 and C3506 by transistor V3511. This transistor is used in a reverse way to get a lower on-resistance.

The FAST RAMP/STAIR COMPARATOR compares the output voltage of the fast ramp generator (FSRMOTXA) with the output voltage of the STAIR ATTENUATOR (STOT--XA). It is a fast symmetrical schmitt trigger circuit, consisting of transistors V3541, V3542, V3538, V3539, V3536, V3537 and associated circuitry. The transistors V3543 and V3544 form an output buffer.
If the fast ramp voltage goes below the stair voltage then transistor V3536 blocks and V3537 conducts. Now transistor V3543 conducts, which makes STSAGT high. STSAGT is applied to the Gate unit A54 and causes that a sample of the input signal is taken. The STSAGTLT signal informs the A.C.L. on unit A5 that a sample is taken.
If the first sample of a scan is to be taken and the FAST RAMP GENERATOR is waiting for a start signal, then STOT--XA is just a bit lower as FSRMOTXA. To avoid the change over of the FAST RAMP/STAIR COMPARATOR, due to interference, the circuit around transistors V3350,V3351 and transformer T3501 decreases the voltage at the base of transistor V3537 in this situation.

The END OF FAST RAMP COMPARATOR detects the crossing of the end level of the fast ramp voltage. If the FSRMOTXA voltage goes below -3 Volt, which is determined by zenerdiode V3520, then transistor V3517 conducts and sets the HOLD OFF FLIPFLOP via transistor V3519, which starts the hold off time.

The HOLD OFF FLIPFLOP is a fast flipflop consisting of transistors V3521, V3522, V3523, V3526, V3527,V3529 and associated circuitry. The transistors V3528, V3568 and V3569 are output buffers.
During the hold off time the status of the transistors is as given in the table below.

Conducts	Blocks
V3523	V3522
V3526	V3527
V3529	V3528
V3569	V3568
V3521	

The output signal HDOF is applied to the Three Stage Trigger unit A32, where trigger pulses are blocked during the hold off time.
At the end of the hold off time the EOHDOF signal resets the HOLD OFF FLIPFLOP via transistor V3524. Now the RSHDOF signal resets the hold off timer circuit.

The SYNC SWITCH switches capacitor C3517 between the HDOF signal and ground in SYNCHRONIZE mode. So the edges of the HDOF signal are made less steep. The capacitor is switched by transistor V3533 on the SYMO--LT signal. The transistor is used in a reverse way to obtain a low on-resistance.

The HOLD OFF DAC, the HOLD OFF INTEGRATOR and the HOLD OFF COMPARATOR form the hold off timer.
The HOLD OFF DAC is a serial DAC (N3309), which gets its data from the microprocessor via the Management unit A25. The output current at pin 22, which determines the hold off time, is applied to the HOLD OFF INTEGRATOR, which consists of opamps N3311, N3312 and transistors V3317 and V3314. The output current of transistor V3317 charges capacitor C3387. This capacitor can be discharged by transistor V3314, to reset the integrator.
In some lower resolution modes the DPU needs more time to calculate interpolated samples. Therefore capacitor C3390 can be switched parallel by transistor V3316 to obtain longer hold off times. This transistor is used in reversed way to get a lower on-resistance.

The HOLD OFF COMPARATOR determines if the voltage from V3317/C3387 exceeds a level determined by the resistors R3412 and R3413. If this happens EOHDF goes high, which resets the HOLD OFF FLIPFLOP. This resets the HOLD OFF INTEGRATOR via the RSHDOF signal by discharging C3387 via transistor V3316. The integrator is also reset by RSSTCNHT if the STAIR COUNTER is reset at the end of a scan.

The TIME-BASE LATCH is a shift register (D3304), which latches a number of time-base status signals, which come from the microprocessor via the Management unit A25.

The TRIGGER DELAY DAC is a serial DAC, which gets its data from the microprocessor via the MANAGEMENT unit A25. The output current at pin 22 of N3306 is converted into a voltage by opamp N3307 and amplified by opamp N3302 and associated circuitry. Next this voltage is added to the STAIR ATTENUATOR output voltage together with -8 Volt, which comes via R3310 and R3311, and inverted by opamp N3308 (ADD+INVERT). The RC combination R3324 and C3329 is a low pass anti-noise filter.
Opams N3301 and N3302 and associated components form a highly stable reference voltage source for the STAIR DAC and the start level of the FAST RAMP GENERATOR.

The stair voltage is generated via the STAIR COUNTER, the STAIR DAC and the STAIR ATTENUATOR.
The STAIR COUNTER (D3302) gets its counting pulses (CNSTCNLT) and its reset signal (RSSTCNLT) from the A.C.L. on unit A5.
By removing jumper X3301 the count pulses can be blocked, which is used for adjustment purposes.
The output lines go to a parallel DAC, the STAIR DAC (N3304). The output currents of the DAC are converted into a voltage by opamp N3303. When the STAIR COUNTER receives count pulses, the voltage at pin 7 of N3303 is a stair case voltage, ranging from 0 to 4 volt in steps of 8 mV.
This stair case voltage can be attenuated by a resistor network, the STAIR ATTENUATOR. The output voltage is applied to the ADD INVERT circuit.
The relays, which determine the attenuation factor, are controlled by the TIME-BASE LATCH.

Note: These units forms together with the Three Stage Trigger unit A32 a closed loop (see figure (8.51.1). When a unit hangs up, the loop can be opened by disconnecting the coax cable at X5202 on unit A32 (HDOF).
By applying a square wave of 1 kHz with an amplitude of 400 mVp-p symmetrically around zero to X5202 the correct operation of these units can be checked, if an input signal is present to generate triggers.

8.51.5 Signal name list

UNIT 51 (including UNIT A52)

Signal name	Description	Signal source	Signal destination(s)
CNDWMO	Count down mode	A34	-
CNSTCNLT	Count stair counter	A5	-
EOHDOF	End of hold off	A51	A52
FSRMCU	Fast ramp current	A51	A51
FSRMOTXA	Fast ramp output	A52	A52
HDOF	Hold off	A52	A32
LEFSRM	Latch enable fast ramp	A25	-
LEHDOF	Latch enable hold off	A25	-
LETBST	Latch enable time-base status	A25	-
LETRDL	Latch enable trigger delay	A25	-
LETRST	Latch enable trigger status	A25	-
RSHDOF	Reset hold off	A52	A51
RSSTCNHT	Reset stair counter	A51	A51
RSSTCNLT	Reset stair counter	A5	-
RVCUSO	Reference voltage current sources	A51	A51,A52
RVDA	Reference voltage DAC	A51	A51
SECK1	Serial clock 1	A25	-
SECK2	Serial clock 2	A25	-
SEDA1	Serial data 1	A25	-
SEDA2	Serial data 2	A25	-
STOT--XA	Stair output	A51	A52
STFSRMHX	Start fast ramp	A32	-
STFSRMLX	Start fast ramp	A32	-
STSAGT	Start sampling gate	A52	A55-A54
STSAGTLT	Start sampling gate	A52	A51-A53-A25-A12-A5
SWFSRM	Switch fast ramp	A51	A52
SWHDOF	Switch hold off	A51	A51
SYMO--LT	Synchronized mode	A34	-
TRSVHI	Trigger sensitivity high	A34	-

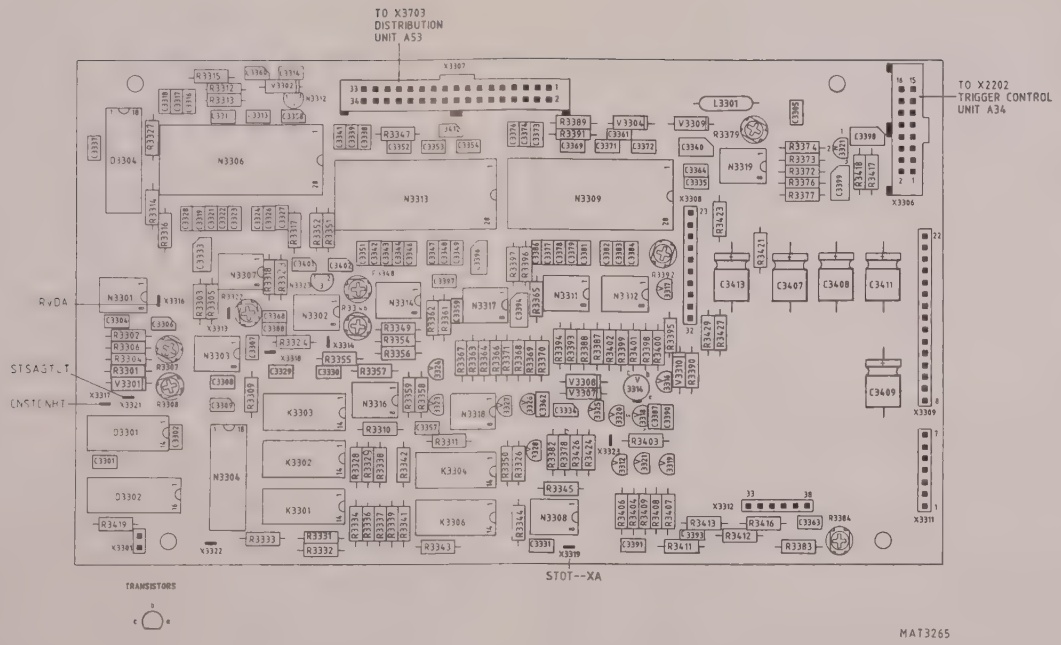


Figure 8.51.3 Unit A51 - TIME-BASE UNIT - p.c.b. lay-out.

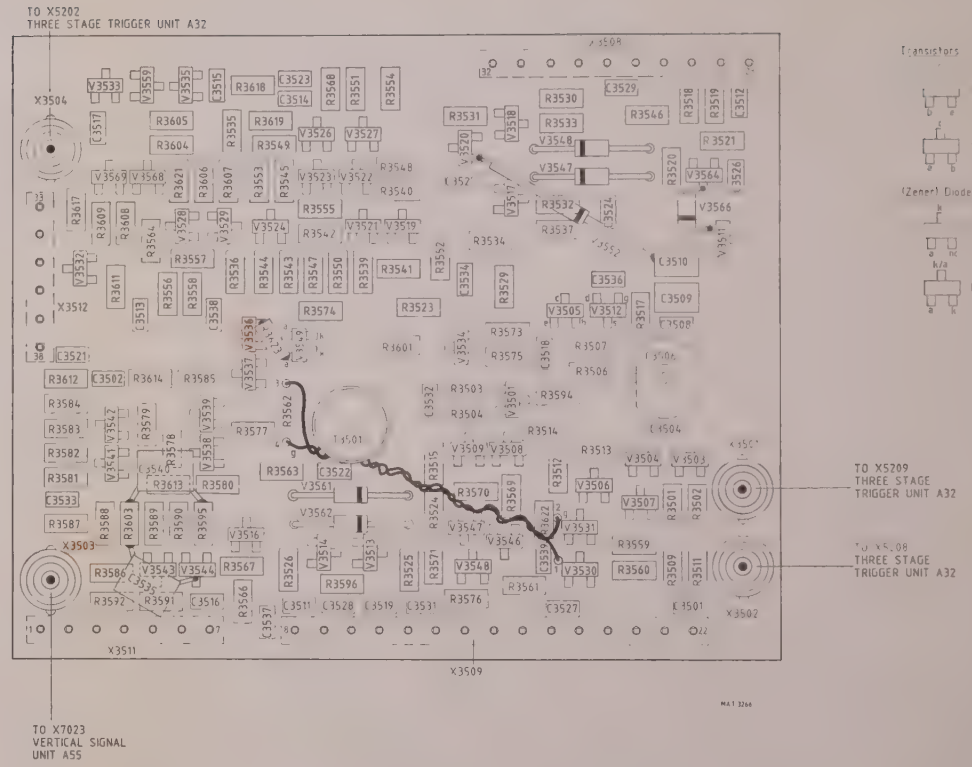
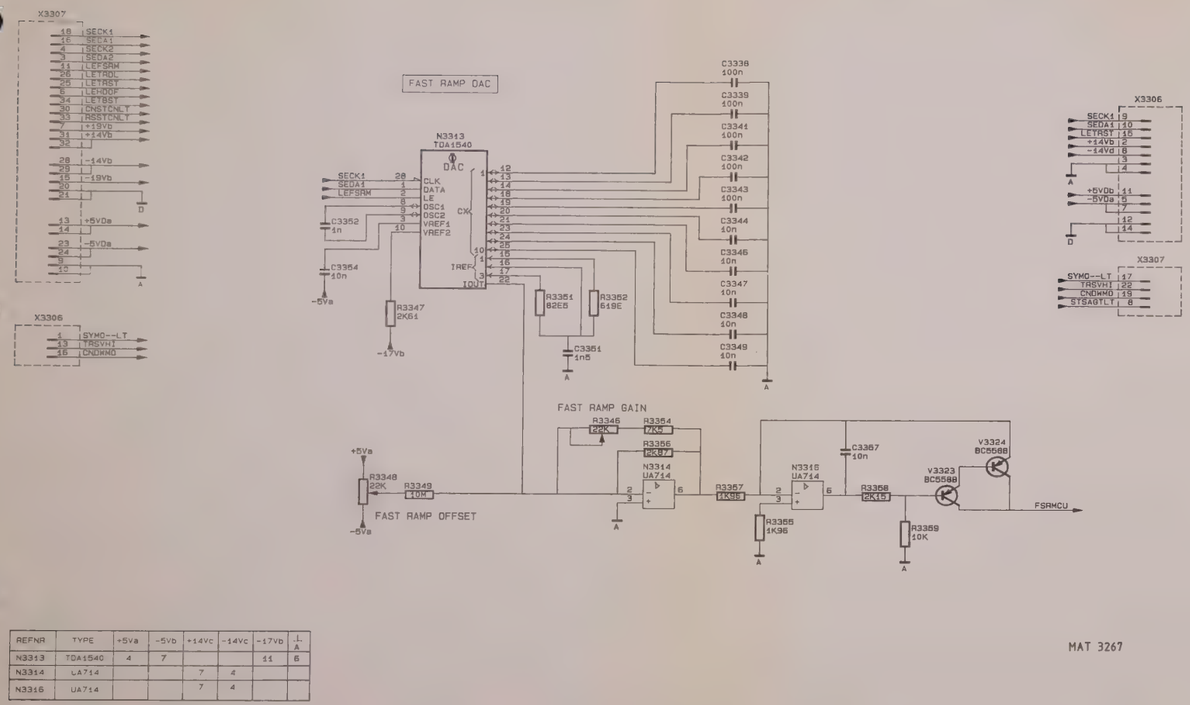
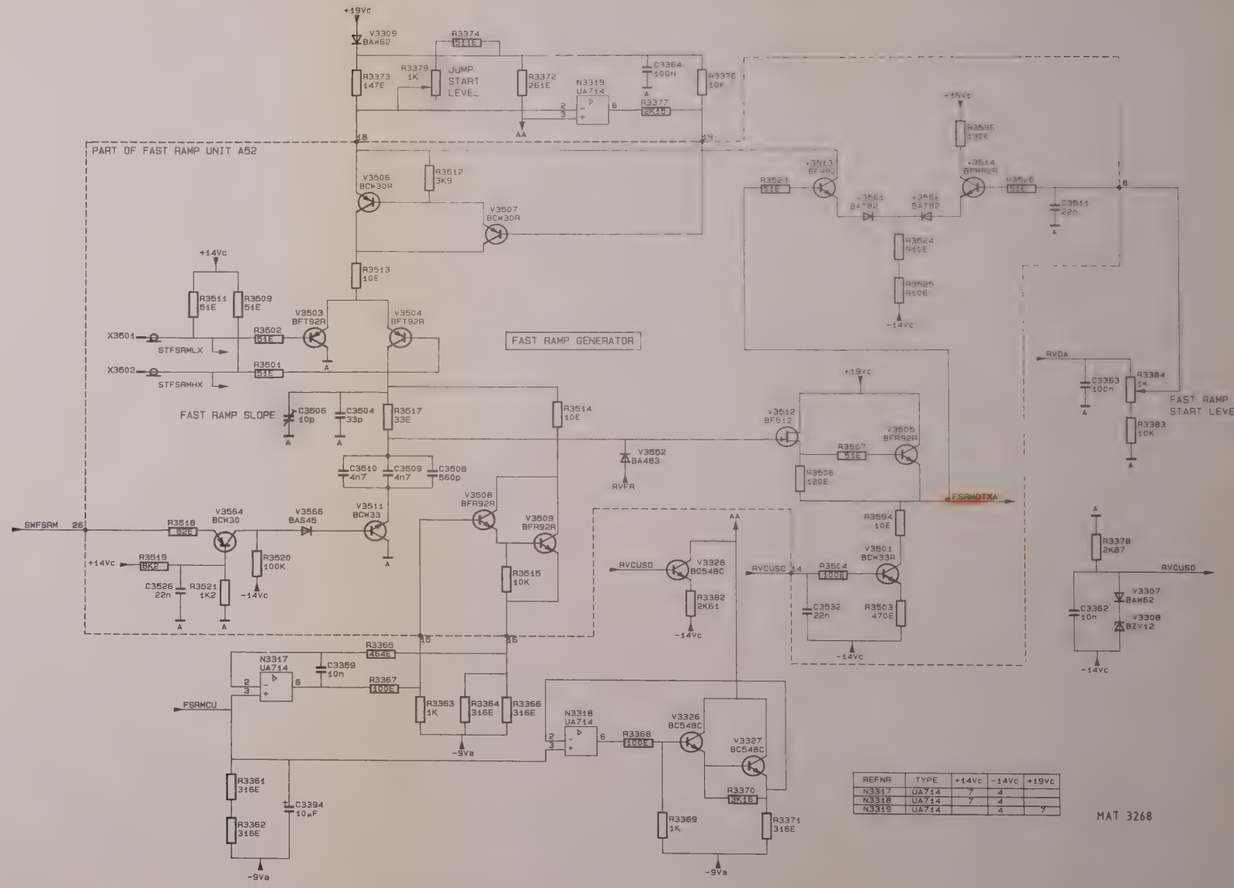


Figure 8.51.4 Unit A52 - FAST RAMP UNIT - p.c.b. lay-out.



REFNR	TYPE	+5Va	-5Vb	+14Vc	-14Vc	-17Vb	⊥ A
N3313	TDA1540	4	7			11	6
N3314	UA714			7	4		
N3315	UA714			7	4		

Figure 8.51.5 Unit A51 + A52 - TIME-BASE UNIT + FAST RAMP UNIT
Circuit diagram.



REFNR	TYPE	+14Vc	-14Vc	+19Vc
N3317	UA714	7	4	
N3318	UA714	7	4	
N3319	UA714		4	7

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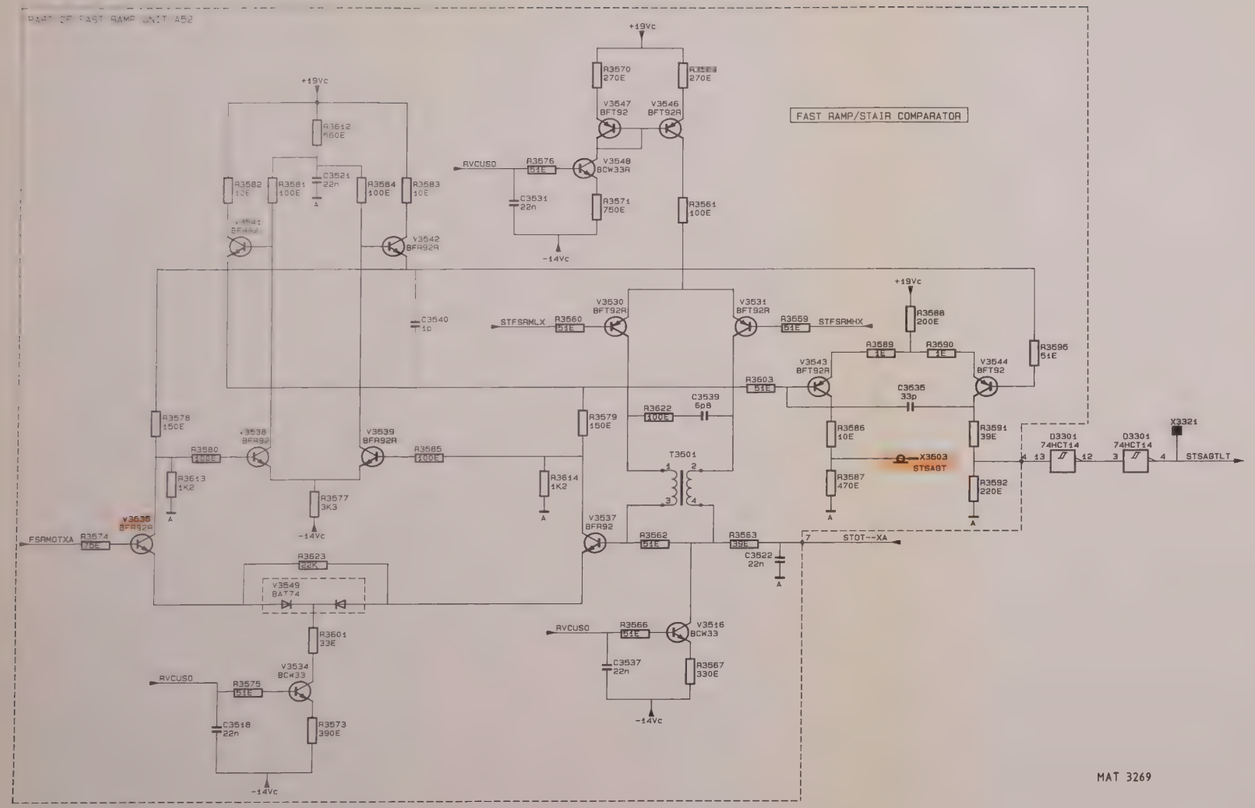


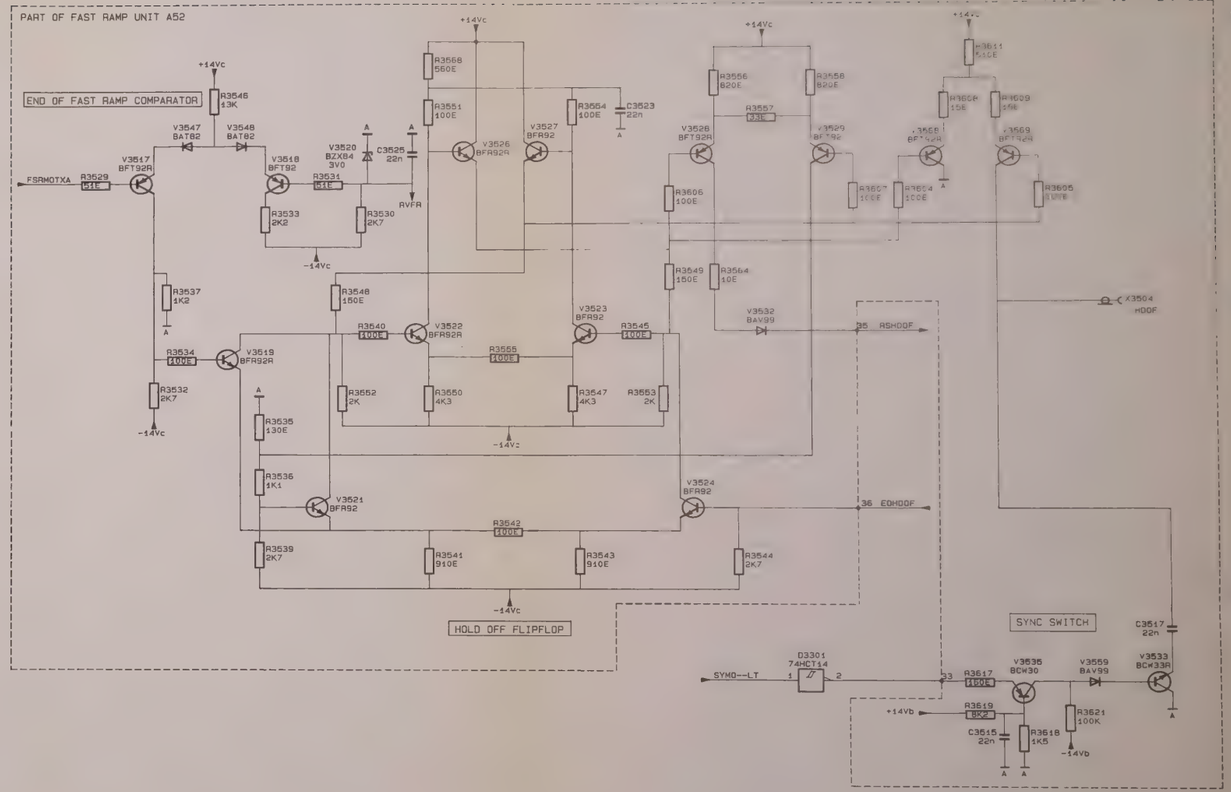
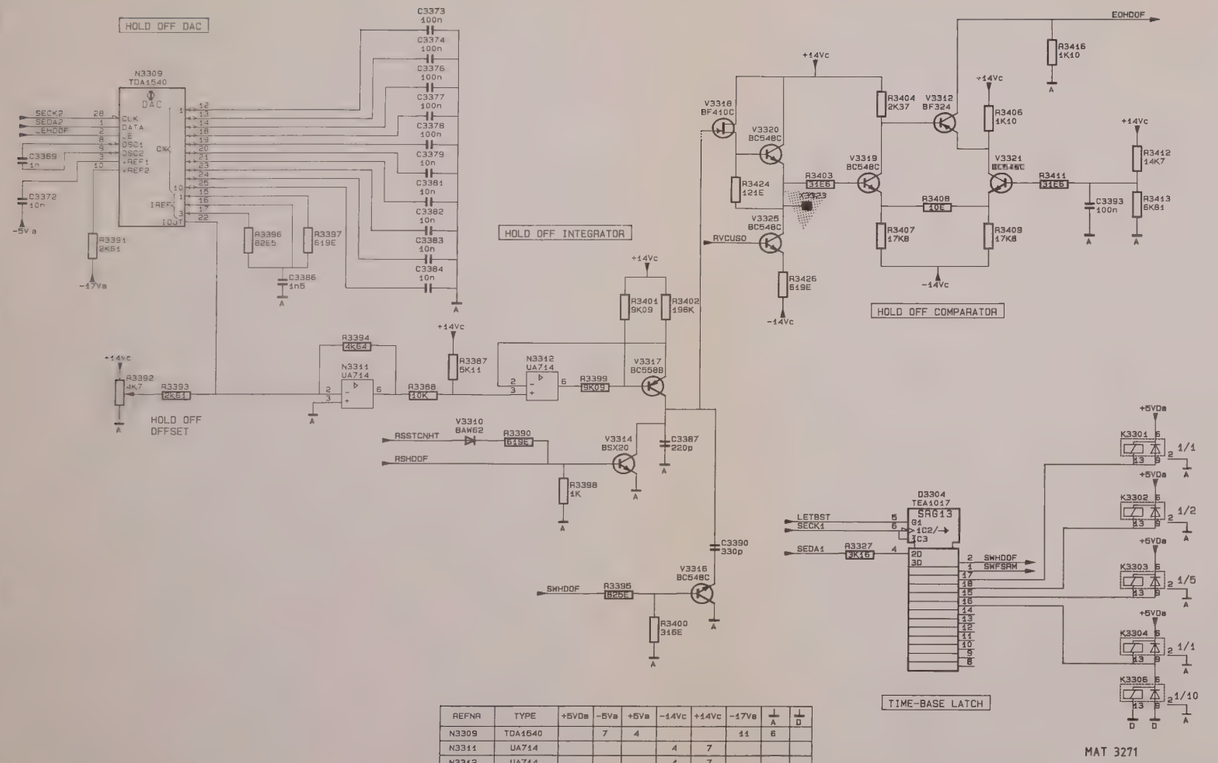
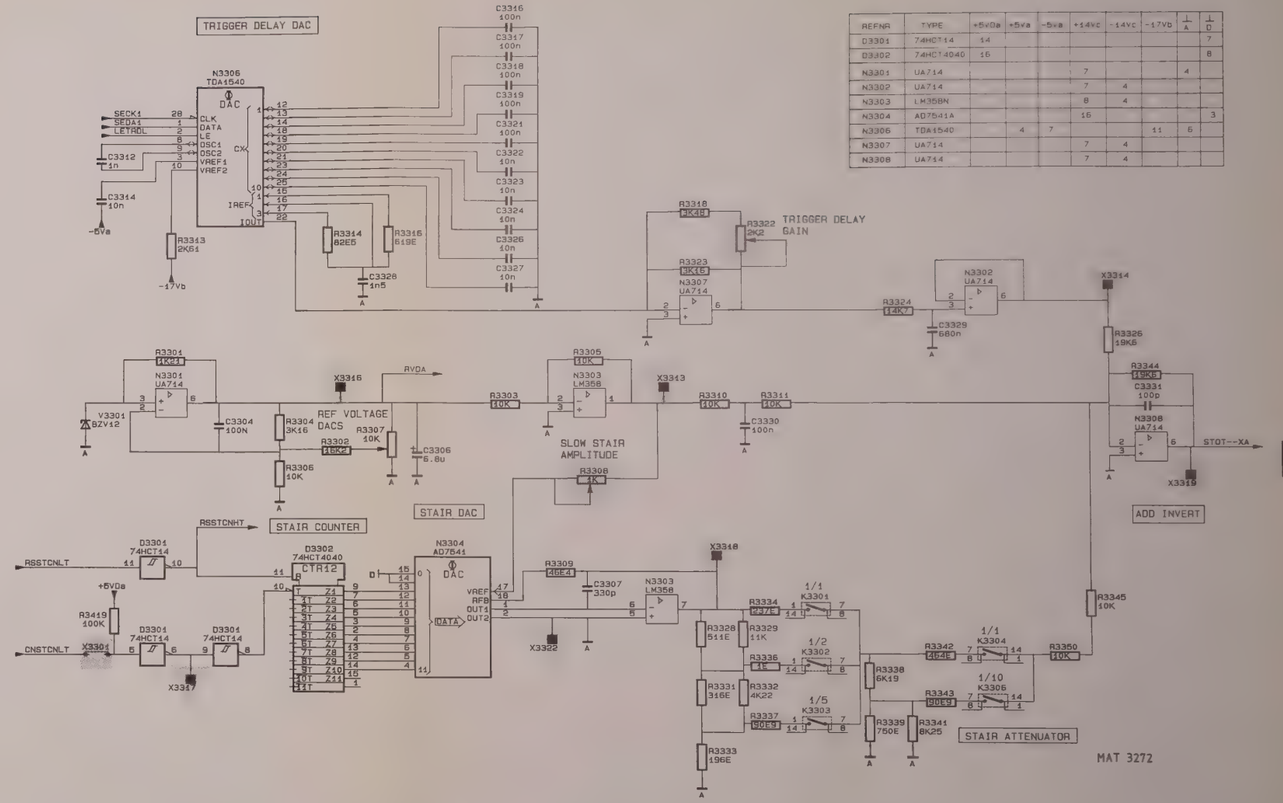


Figure 8.51.6 Unit A51 + A52 - TIME-BASE UNIT + FAST RAMP UNIT
Circuit diagram.



REFNR	TYPE	+5VDa	-5Va	+5Va	-14Vc	+14Vc	-17Va	⊥ A	⊥ D
N3309	TDA1540		7	4			11	6	
N3311	UA714				4	7			
N3312	UA714				4	7			
D3304	TEA1017	7							3

Figure 8.51.7 Unit A51 + A52 - TIME-BASE UNIT + FAST RAMP UNIT
Circuit diagram.



REFNR	TYPE	+5VDa	+5Va	-5Va	+14Vc	-14Vc	-17Vb	⊥ A	⊥ D
D3301	74HCT14	14							7
D3302	74HCT4040	16							8
N3301	UA714				7			4	
N3302	UA714				7	4			
N3303	LM358N				8	4			
N3304	AD7541A				16				3
N3305	TDA1540		4	7			11	6	
N3307	UA714				7	4			
N3308	UA714				7	4			

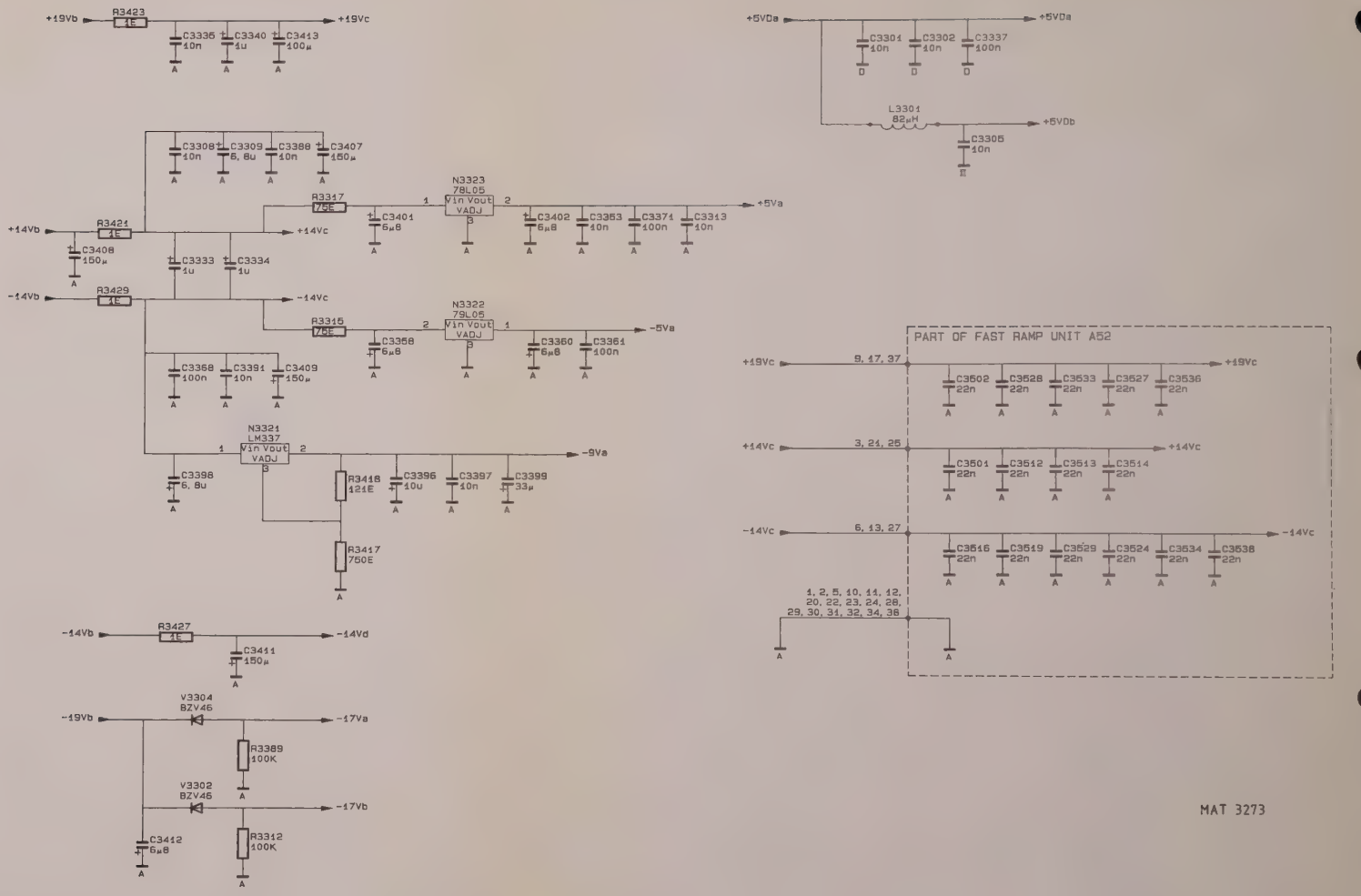
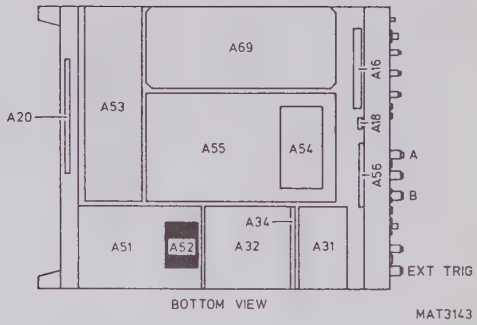


Figure 8.51.8 Unit A51 + A52 - TIME-BASE UNIT + FAST RAMP UNIT
Circuit diagram.

UNIT A52 - FAST RAMP UNIT



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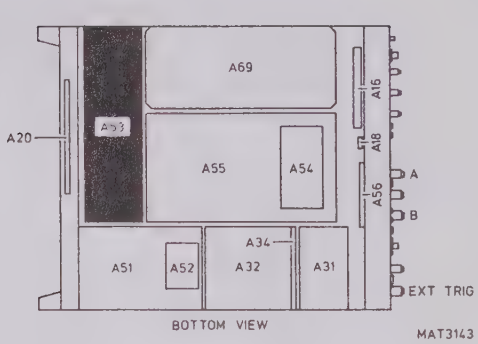
8.52.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.51.

UNIT A53 - DISTRIBUTION UNIT



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8.53.3 Signal name list..... 8.53-2

8.53.1 General information

This unit consists of three parts:

- a probe detection circuit
- a calibrator
- a power supply distribution circuit

8.53.2 Circuit description

The PROBE DETECTION circuit detects the attenuation factor of the probe(s) via the signal PRIFA-XA for channel A and PRIFB-XA for channel B.
This current is converted by the ADC D3702 to binary data according the following table:

	Channel A		Channel B	
Probe	PRIFA1	PRIFA2	FRIPB1	PRIFB2
No detection ring	1	1	1	1
1:10 (50 Ohm)	0	1	0	1
1:100 (50 Ohm)	1	0	1	0

The digital probe information signals are led to the INPUT PORT on the Management unit A25, where they can be read by the microprocessor.

The CALIBRATOR consists of a 4 MHz crystal controlled oscillator (G3701) with 2 internal dividers.
The 1 MHz output (pin 6) is led to a divide-by-10 stage (D3701). The output signal is led to a buffer consisting of transistors V3703 and V3704 and associated circuitry. The amplitude of the output signal CAL is controlled by adjusting the power supply voltage (+12Va) of the CALIBRATOR by means of potentiometer R3724.
This signal (100 kHz, 1 Vpp into 50 ohm) is applied to the CAL output socket on the front panel.

The POWER SUPPLY DISTRIBUTION consists of a number of power decoupling networks and a stabilized power supply for the CALIBRATOR.
Furtheron, it distributes the power supply lines coming from unit A19 via A20 to the various units in this instrument.

8.53.3 Signal name list

UNIT 53

Signal name	Description	Signal source	Signal destination(s)
CAL	Calibrator	A53	FRONT
CHSW-1	Channel switch 1	A25	-
CNDWMO	Count down mode	A34	-
CNSTCNLT	Count stair counter	A5	-
LEFSRM	Latch enable fast ramp	A25	-
LEHDOF	Latch enable hold off	A25	-
LETBST	Latch enable time-base status	A25	-
LETRDL	Latch enable trigger delay	A25	-
LETRST	Latch enable trigger status	A25	-
LEVEA	Latch enable vertical A	A25	-
LEVEB	Latch enable vertical B	A25	-
LEVGFA	Latch enable variable gain forward A	A25	-
LEVGFB	Latch enable variable gain forward B	A25	-
PRIFA-XA	Probe information A	A54	-
PRIFA1	Probe information A1	A53	A25
PRIFA2	Probe information A2	A53	A25
PRIFB-XA	Probe information B	A54	-
PRIFB1	Probe information B1	A53	A25
PRIFB2	Probe information B2	A53	A25
RSSTCNLT	Reset stair counter	A5	-
SECK1	Serial clock 1	A25	-
SECK2	Serial clock 2	A25	-
SEDA1	Serial data 1	A25	-
SEDA2	Serial data 2	A25	-
STSAGTLT	Start sampling gate	A52	-
SYMO--LT	Synchronized mode	A34	-
TRSVHI	Trigger sensitivity high	A34	-

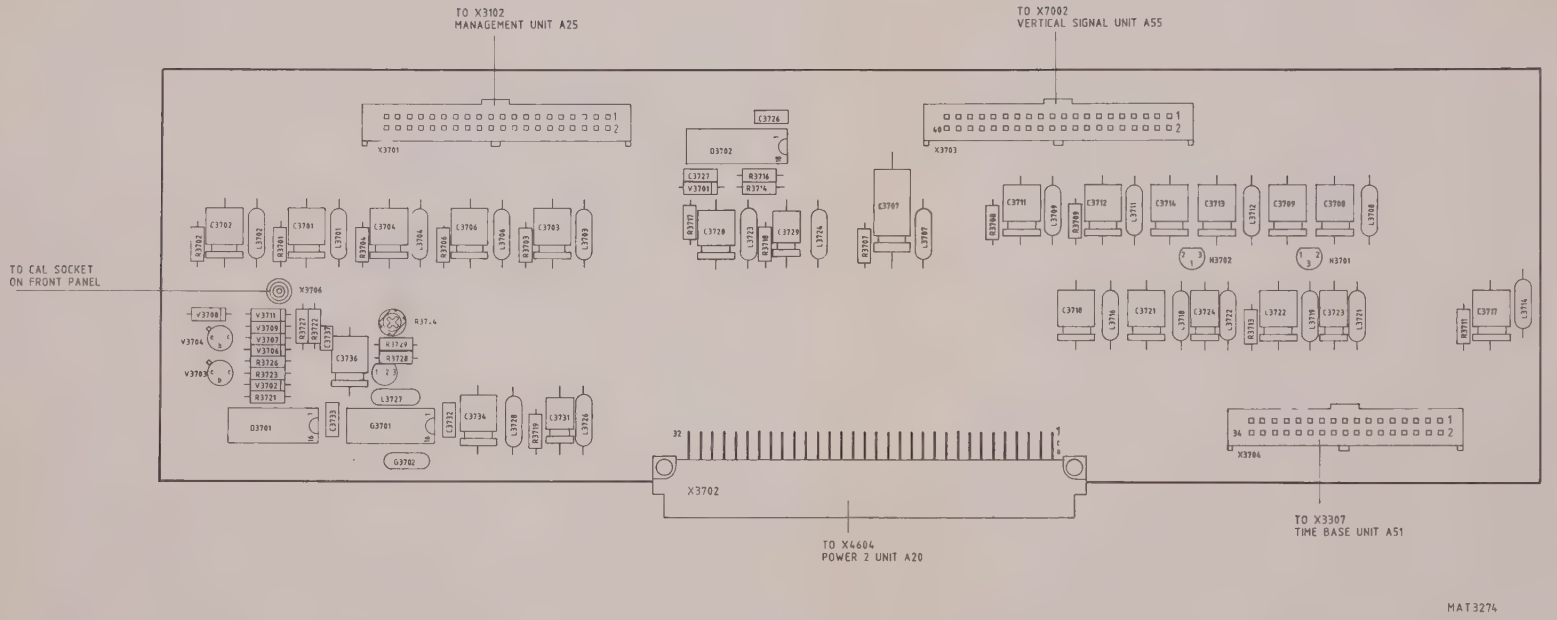
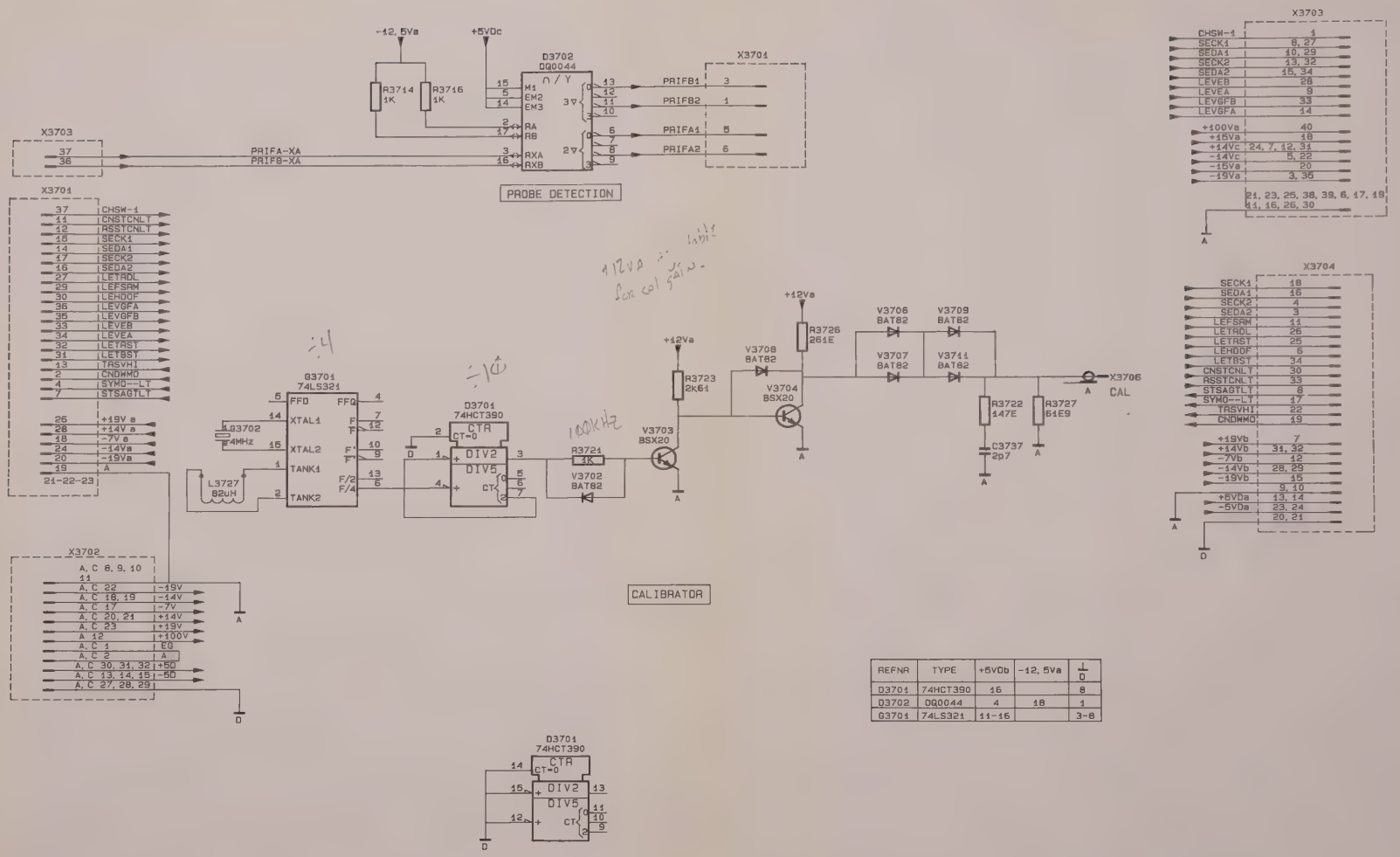


Figure 8.53.1 Unit A53 - DISTRIBUTION UNIT - p.c.b. lay-out.



REFNR	TYPE	+5VDb	-12,5Va	1/D
D3701	74HCT390	16		8
D3702	0Q0044	4	18	1
G3701	74LS321	11-16		3-8

Figure 8.53.2 Unit A53 - DISTRIBUTION UNIT - Circuit diagram.

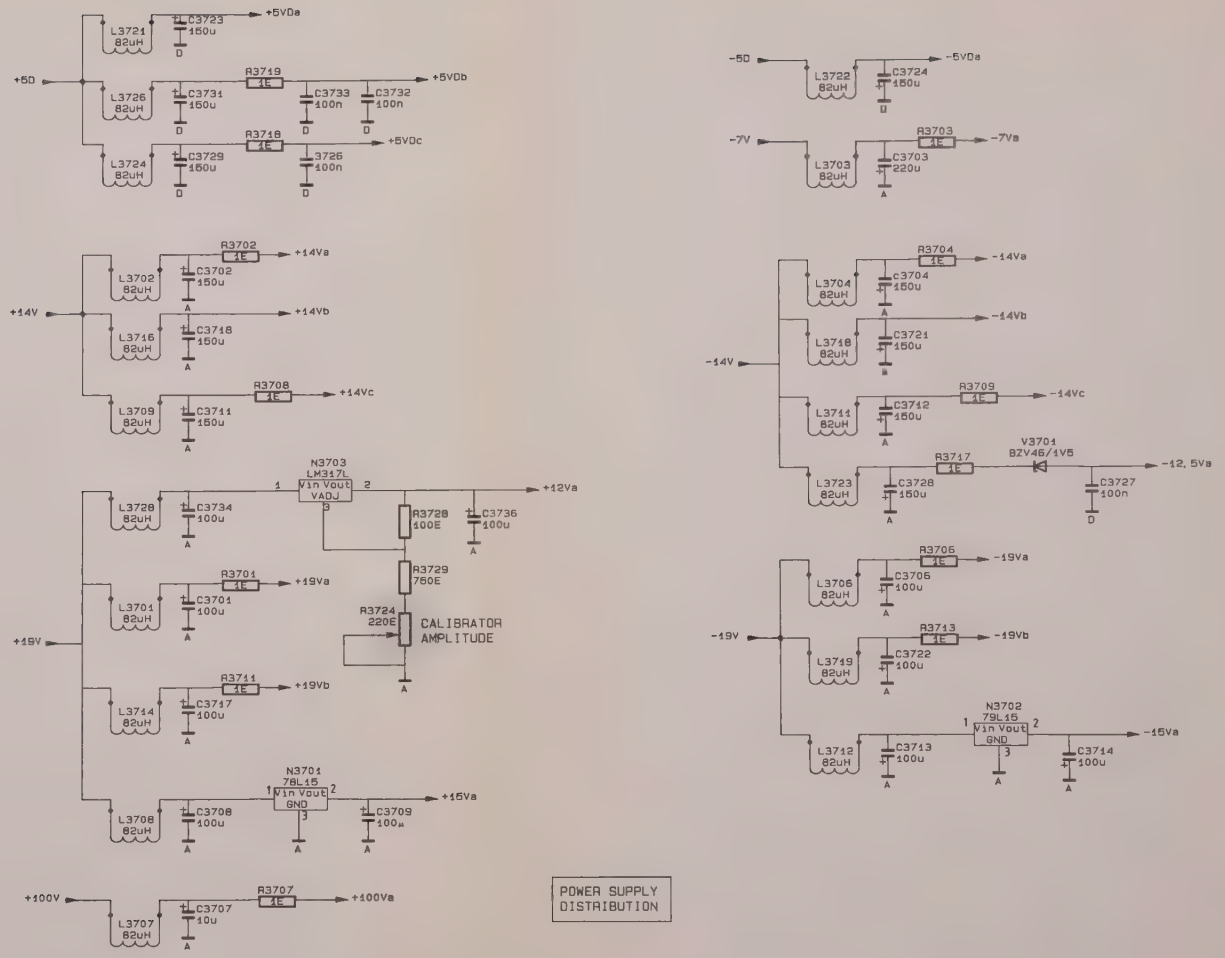
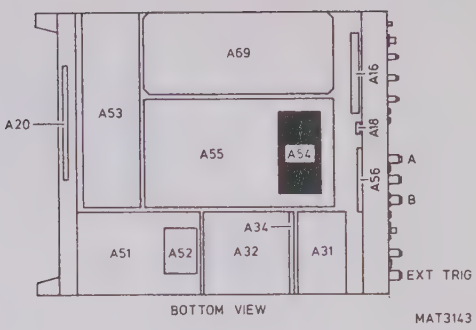


Figure 8.53.3 Unit A53 - DISTRIBUTION UNIT - Circuit diagram

UNIT A54 - GATE UNIT



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8.54.2 Circuit description..... 8.54-1
8.54.3 Signal name list..... 8.54-2

8.54.1 General information

In this section, the Trigger Pick Off unit A56 and the Delay Line unit A69 are also described.
The Gate unit, which is a part of the sampling system, takes samples of the input signals on both channels on receipt of a sampling pulses. The unit is fitted on the Vertical signal unit A55, on which further processing of the samples is done.

8.54.2 Circuit description

The input signals from channels A and B are applied to the TRIGGER PICK-OFFs. The picked off trigger signals have an amplitude of about one tenth of their corresponding input signals. They are applied to the Trigger Input unit A31.
Via 30 nsec DELAY LINEs (unit A69) the input signals from the TRIGGER PICK OFFs are applied to the Gate unit.
This unit consists of a SAMPLING DRIVER, SAMPLING GATE A and SAMPLING GATE B.
The SAMPLING DRIVER receives sampling pulses (STSAGT) from the Fast Ramp unit A52 and splits them in equal, symmetrical sampling pulses for SAMPLING GATE A and SAMPLING GATE B.
These sampling pulses are applied to the sampling diodes (V907 for ch. A and V908 for ch. B) via the clipping lines.
For a further description of the sampling system see section 8.55.2.

The input signals are terminated with 50 ohm by means of R901, R902, R904, R906 for ch. A and R932, R933, R929 and R931 for ch. B.
A part of the input signal (LFCOA for ch. A, LFCOB for ch. B) is applied to the Vertical Signal unit A55 for LF-compensation.

IMPORTANT: The component layout of this unit is rather critical. Therefore it is recommended to replace the complete p.c.b. in case of a failure.
The components which may burn out in case of a too high input voltage can be replaced anyway.
These components are V907, R901, R902, R904, R906 for ch. A and V908, R929, R931, R932, R933 for ch. B.

Notes: - This board is made of a special material, which is suitable for very high frequencies. This material can be bended easily; so please handle carefully.
- When a board is replaced, please take care that the resistors R913 and R923 are not clamped between the board and the connectors on the Vertical Signal unit.

8.54.3 Signal name list

UNIT 54 (including UNITS A56 and A69)

Signal name	Description	Signal source	Signal destination(s)
A	Channel A	A57	-
AVVO	Avalanche voltage	A55	-
B	Channel B	A57	-
BIDHA	Bias diode high A	A55	-
BIDHB	Bias diode high B	A55	-
BIDLA	Bias diode low A	A55	-
BIDLB	Bias diode low B	A55	-
LFCOA	LF compensation A	A54	A55
LFCOB	LF compensation B	A54	A55
SOCUA	Snap-off current A	A55	-
SOCUB	Snap-off current B	A55	-
STSAGT	Start sampling gate	A52	-
TRPO-A	Trigger pick off A	A56	A31
TRPO-B	Trigger pick off B	A56	A31

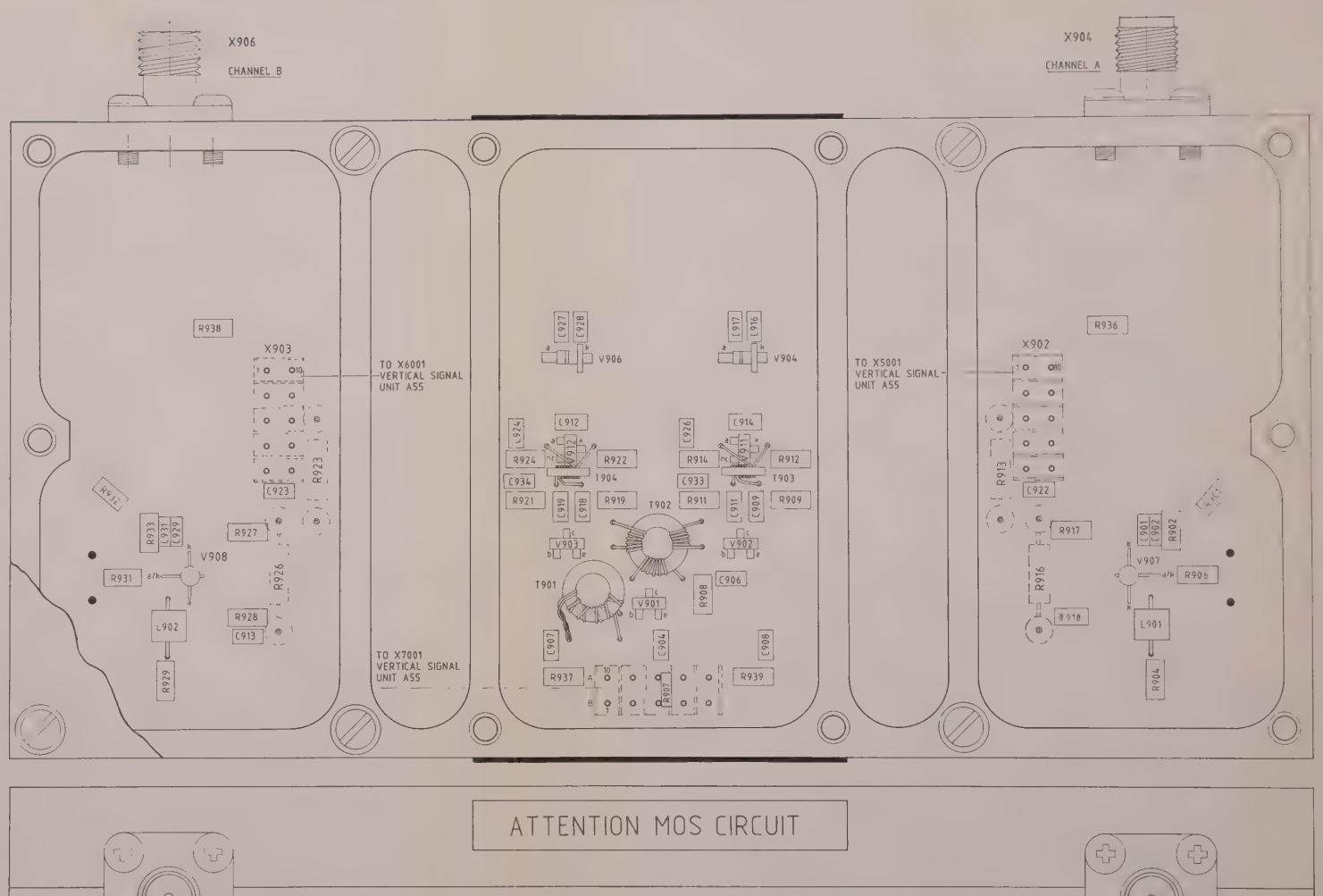


Figure 8.54.1 Unit A54 - GATE UNIT - p.c.b. lay-out.

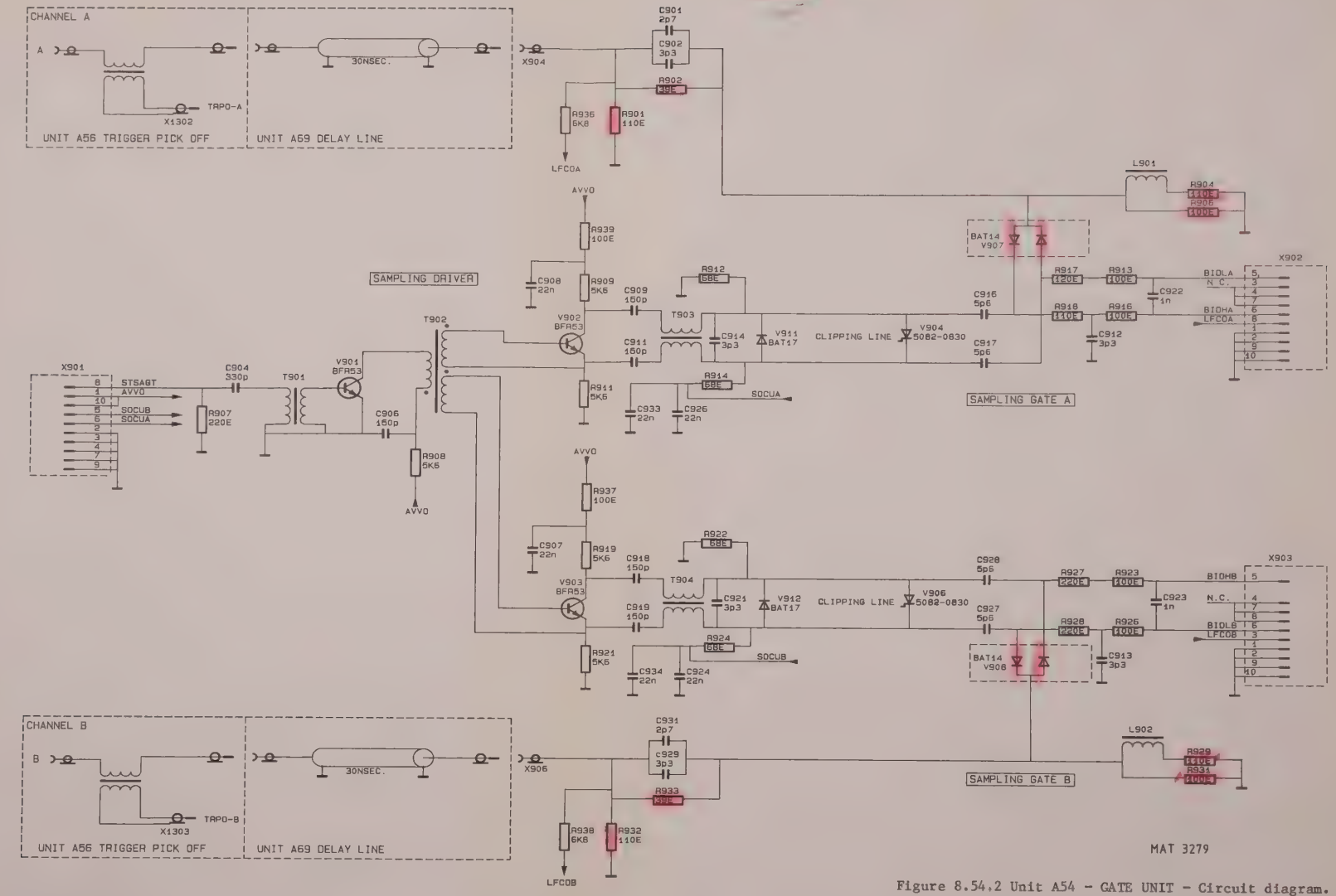
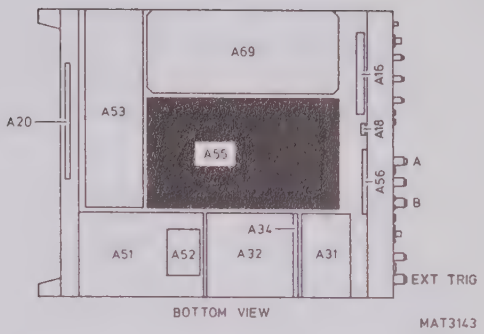


Figure 8.54.2 Unit A54 - GATE UNIT - Circuit diagram.

UNIT A55 - VERTICAL SIGNAL UNIT



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8.55.2 Sampling system..... 8.55-1
8.55.3 Circuit description..... 8.55-2
8.55.4 Signal name list..... 8.55-4

8.55.1 General information

This unit processes the samples of both channels until they are ready to be accepted by the ADC and T&H unit A11.
Also some auxiliary circuits for the Gate unit are on this unit.
Samples on both channels are taken synchronuously and processed synchronuously until the channel switch on this unit.

8.55.2 Sampling system

The sampling system consists for each channel of a SAMPLING GATE on unit A54 and a BRIDGE on unit A55. Figure 8.55.1 shows a simplified diagram of the sampling system of channel A.
Both current sources in the BRIDGE A supply an equal bias current. If the inputsignal (A), the feedback signal (FBOTA) and the offset signal (OSOTA) are all at ground level, then the system is symmetrical.
When sampling pulses occur, the sampling diodes (V907) are in conductance and a part of the bias current of the upper current source will flow through T5001, winding 2-5, R916, R918, V907, R913, R917 and T5001, winding 4-3.
Due to the symmetry, the current through winding 2-5 is equal to the current through winding 4-3. Now the effects of both currents compensate each other, due to the winding sense of both windings. This results in no output voltage from winding 7-8 to the PRE-AMPLIFIER A.
If the input voltage (A) is not equal to zero, then the currents at sample moments through the windings 2-5 and 4-3 will be different, resulting in voltage pulses (samples) from winding 7-8, which are proportional to the input voltage.
If the signals FBOTA and OSOTA are not zero, then the voltages of the BRIDGE A will shift up and down with them. This causes different currents through the windings 2-5 and 3-4 at sample moments, which on their turn result in sample voltages from winding 7-8, which are proportional to FBOTA and OSOTA.

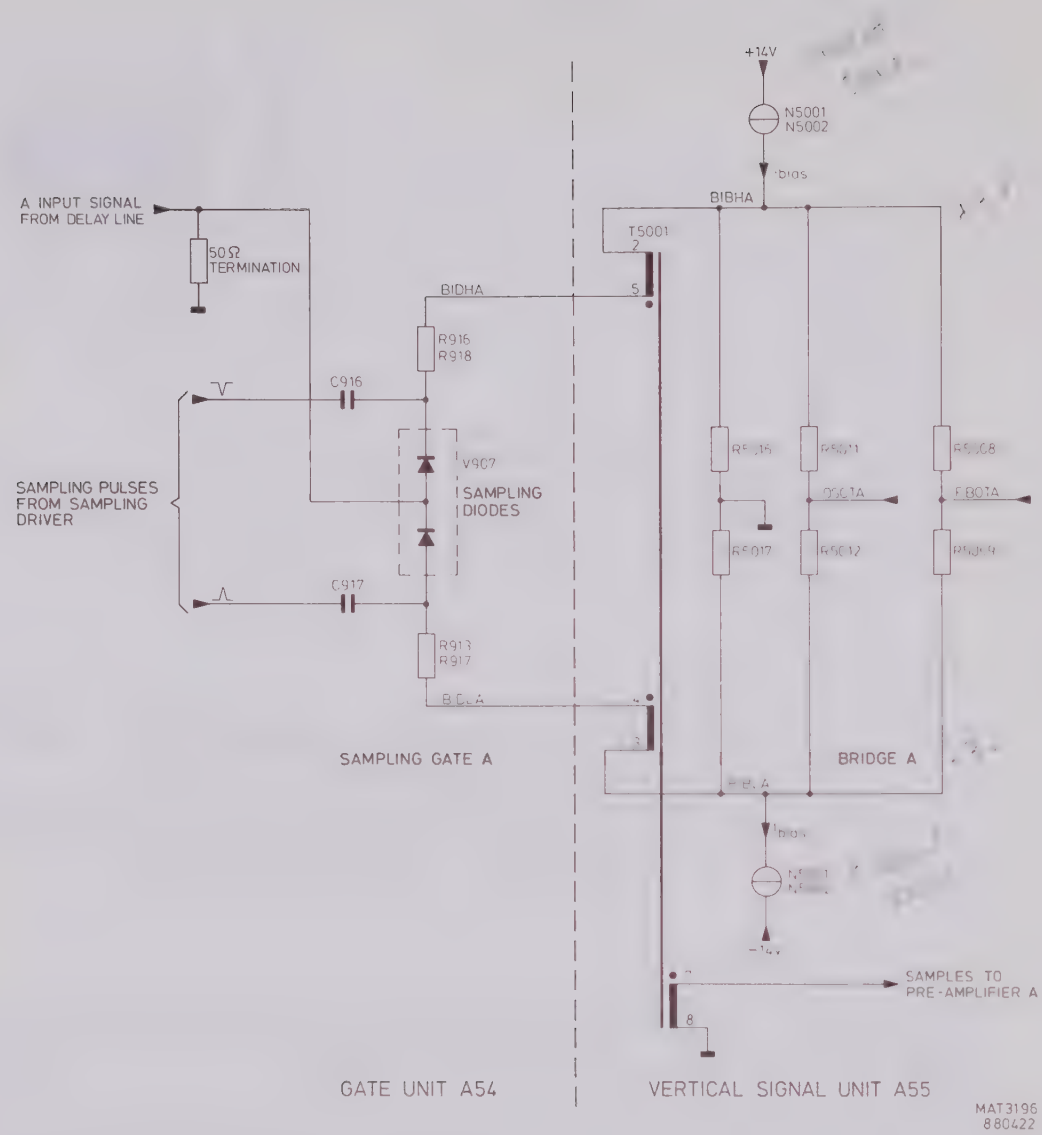


Figure 8.55.1 Sampling system.

8.55.3 Circuit description

As both channels are identical only channel A is described.

The BRIDGE A consists of 2 current sources, a resistor network (R5008...R5017) and pulse transformer T5001.
The 2 current sources consist of opamp N5001 and transistor array N5002. The upper current source supplies the bias current for the bridge via pin 15 of N5002. Via a current-mirror circuit, consisting of the remaining transistors of N5002, an equal current is sunk from the bridge via pin 9.

The OFFSET A circuit consists of a number of opamp circuits, which add the offset course (OSCRA) and the offset fine (OSFIA) signals. The output signal OSOTA is applied to the BRIDGE A.
The slide switches S5002A...S5003B are used for adjustment purposes.

The analoge feedback signal VBOTA from the Management unit A25 is attenuated by the circuitry around opamp N5004, depending on the selected vertical input sensitivity. The attenuation factor is controlled by the microprocessor. The output signal FBOTA is applied to the BRIDGE A.

The samples from winding 7-8 of transformer T5001 are applied to the PRE-AMPLIFIER A. On a number of nodes an LF-compensation signal (LFCOA) from the Gate unit is applied.
Next the amplified samples (PAOTA) are applied to the AMPLIFIER A. The amplification factor is microprocessor controlled and depends on the selected vertical input sensitivity.
Next the samples are applied to the TRACK&HOLD A circuit around IC N5006, where they are held on the top of the sample voltage, which enables the ADC on unit A11 to convert the samples of both channels behind each other.
The T&H is controlled by the A.C.L. on unit A5 via the T&H SWITCH.

The VERTICAL LATCH is a shift register, which holds the amplification factors and the attenuation factors. It gets its data from the microprocessor via the Management unit A25.

The samples from the TRACK&HOLD A are applied to a multiplying DAC (N5013) in the VARIABLE A circuit. The digital code to the DAC comes from a shift register (D5002), which gets its data from the microprocessor via the Management unit. The output current of the DAC (pin 1) is converted to a voltage by opamp N5014. Next this voltage is applied to the CHANNEL SWITCH, which switches between samples of both channels.

The samples at the output (THINAN) are applied to T&H and ADC unit A11, where they are a converted into digital codes.

Furtheron, the unit contains three circuits, which are common for both channels.
The AVALANCHE VOLTAGE circuit is a stabilised voltage supply which supplies the avalanche voltage for the Gate unit.

The SNAP-OFF CURRENT circuit is a current source, which supplies the snap-off current for the Gate unit.

The T&H SWITCH is a buffer between the HDSA-1 signal from the A.C.L. on unit A5 and the T&H circuits on this unit.
The hold moments for both channels can be adjusted separately with R7011 and R016.
This circuit is mounted on an add-on p.c.b. which is fitted on socket X7007.

Notes: - As the Vertical Signal unit has a feedback loop, the accuracy of the gain factors is determined by the accuracy of the attenuation factors of the feedback loop.
- Looking at the bottom side of th oscilloscope, when it is standing on its rear feet, the A-input connector is at the left side of the B-input connector.
However on the p.c.b. the right half is used for channel A and the left half for channel B. This is caused by the equal lengths of the delay lines.

8.55.4 Signal name list

UNIT A55

Signal name	Description	Signal source	Signal destination(s)
AM2A	Amplifier x2 A	A55	A55
AM2B	Amplifier x2 B	A55	A55
AM4A	Amplifier x4 A	A55	A55
AM4B	Amplifier x4 B	A55	A55
AM1ØA	Amplifier x10 A	A55	A55
AM1ØB	Amplifier x10 B	A55	A55
AT1A	Attenuation x1 A	A55	A55
AT1B	Attenuation x1 B	A55	A55
AT2A	Attenuation x2 A	A55	A55
AT2B	Attenuation x2 B	A55	A55
AT4A	Attenuation x4 A	A55	A55
AT4B	Attenuation x4 B	A55	A55
AT1ØA	Attenuation x10 A	A55	A55
AT1ØB	Attenuation x10 B	A55	A55
AT1ØØA	Attenuation x100 A	A55	A55
AT1ØØB	Attenuation x100 B	A55	A55
AVVO	Avalanche voltage	A55	A54
BIBHA	Bias bridge high A	A55	A55
BIBHB	Bias bridge high B	A55	A55
BIBLA	Bias bridge low A	A55	A55
BIBLB	Bias bridge low B	A55	A55
BIDHA	Bias diode high A	A54	-
BIDHB	Bias diode high B	A54	-
BIDLA	Bias diode low A	A54	-
BIDLB	Bias diode low B	A54	-
CHSW-1	Channel switch 1	A25	-
FBOTA	Feedback output A	A25	-
FBOTB	Feedback output B	A25	-
HDSA-1	Hold sample 1	A5	-
LEVEA	Latch enable vertical A	A25	-
LEVEB	Latch enable vertical B	A25	-
LEVGFA	Latch enable variable gain forward A	A25	-
LEVGFB	Latch enable variable gain forward B	A25	-
LFCOA	LF compensation A	A54	-
LFCOB	LF compensation B	A54	-
OSCRA	Offset course A	A25	-
OSCRB	Offset course B	A25	-
OSFIA	Offset fine A	A25	-
OSFIB	Offset fine B	A25	-
OSOTA	Offset output A	A25	-
OSOTB	Offset output B	A25	-
PAOTA	Pre-amplifier out A	A55	A55
PAOTB	Pre-amplifier out B	A55	A55
PRIF-A	Probe information A	A57	-
PRIF-B	Probe information B	A57	-
PRIFA-XA	Probe information A	A55	A53-A25
PRIFA-XB	Probe information B	A55	A53-A25

Signal name	Description	Signal source	Signal destination(s)
SOCUA	Snap off current A	A55	A54
SOCUB	Snap off current B	A55	A54
STSAGT	Start sample gate	A52	-
THINA	Track & Hold input A	A55	A55
THINAN	Track & Hold in analogue	A55	A11
THINB	Track & Hold input B	A55	A55
THMOA	Track & Hold mode A	A55	A55
THMOB	Track & Hold mode B	A55	A55
THOTA	Track & Hold output A	A55	A55
THOTB	Track & Hold output B	A55	A55
SECK1	Serial clock 1	A25	-
SECK2	Serial clock 2	A25	-
SEDA1	Serial data 1	A25	-
SEDA2	Serial data 2	A25	-
VBOTA	Variable backward output A	A25	-
VBOTB	Variable backward output B	A25	-
VFOTA	Variable forward output A	A55	A55
VFOTB	Variable forward output B	A55	A55

TRANSISTORS
TOP VIEW

BC549
BC559

BF422

BF494

BSV78

BFW11

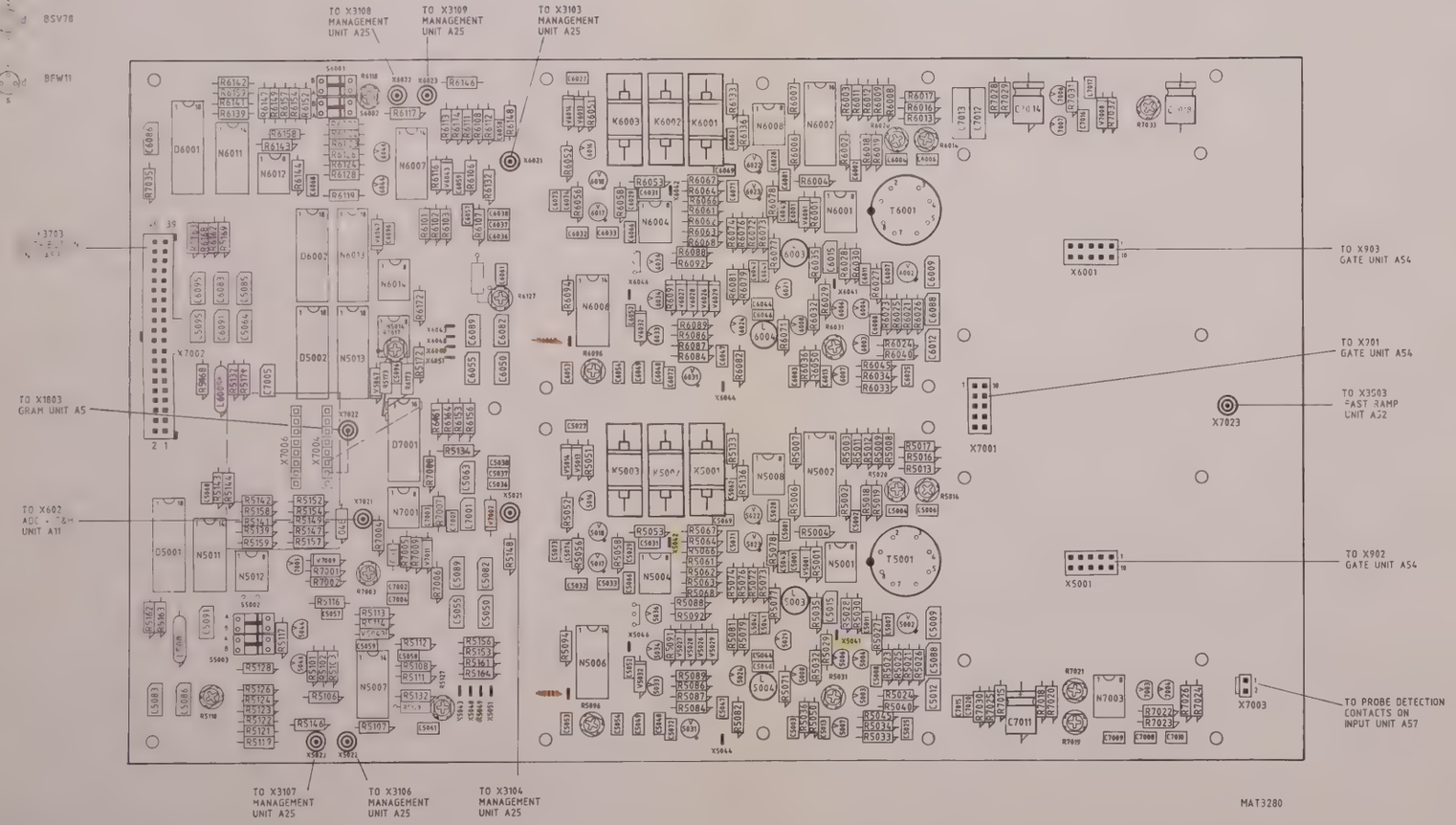


Figure 8.55.2 Unit A55 - VERTICAL SIGNAL UNIT - p.c.b. lay-out.

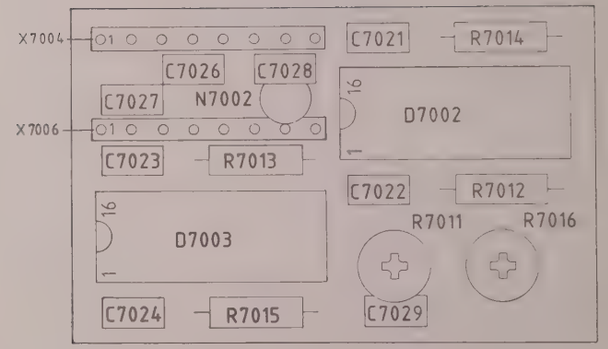
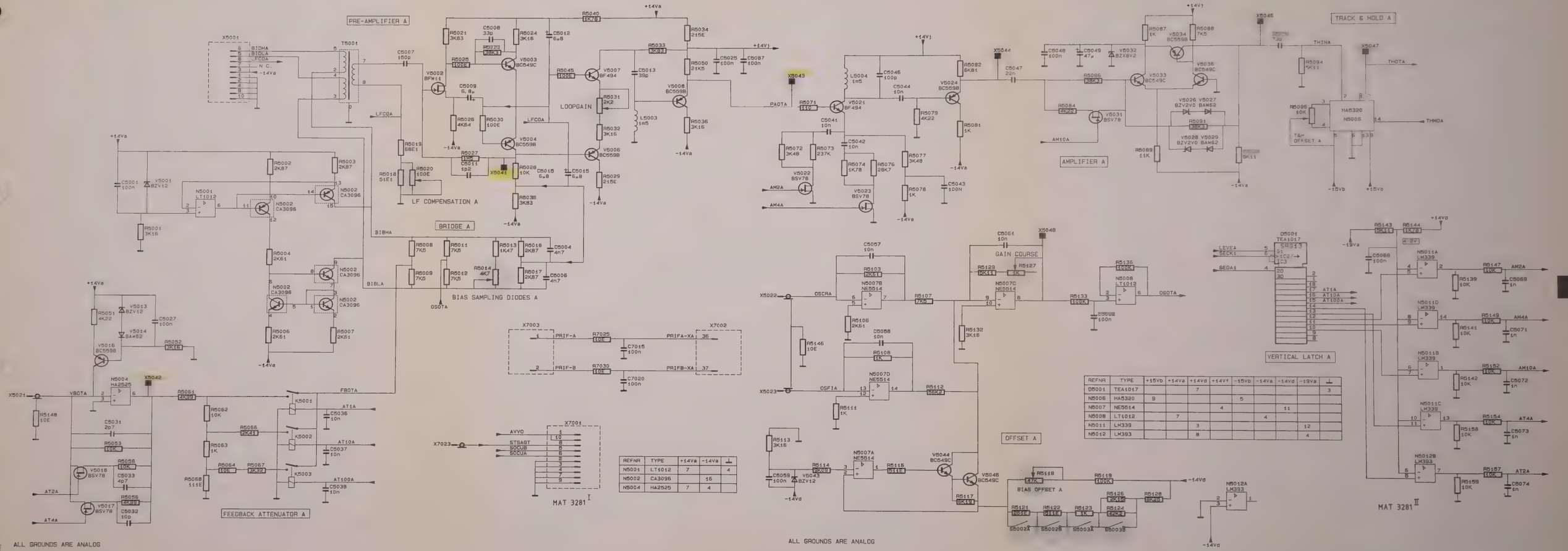


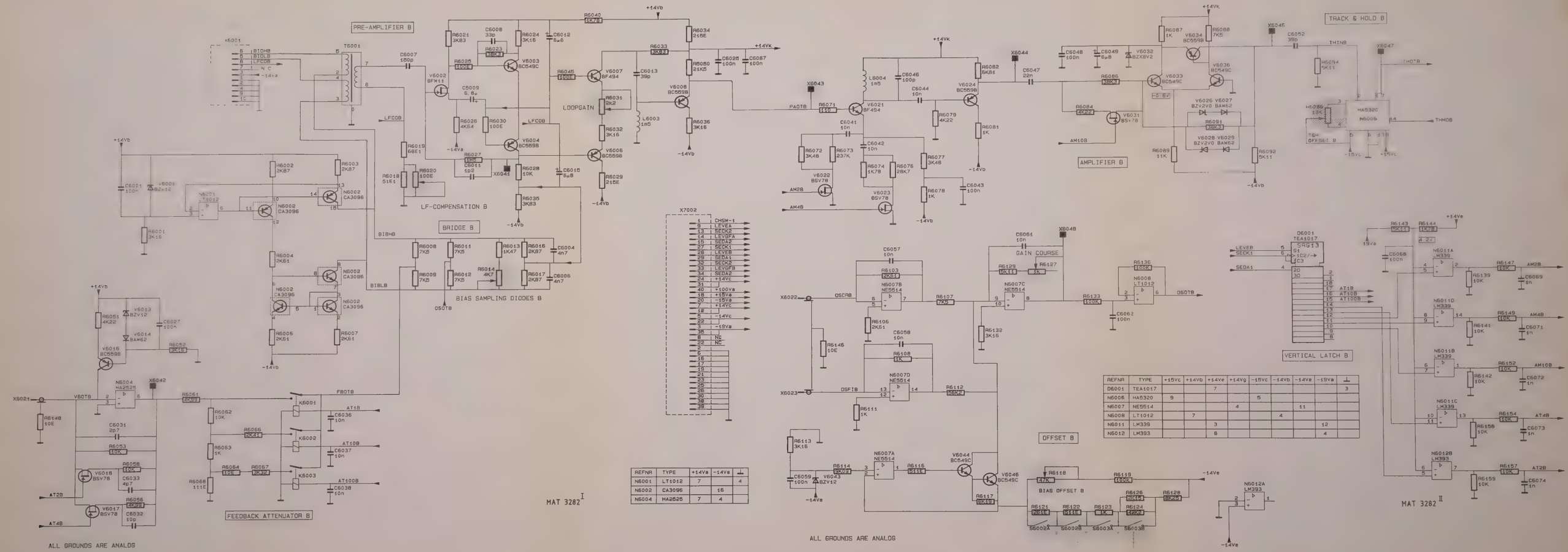
Figure 8.55.3 Unit A55 - VERTICAL SIGNAL UNIT
P.c.b. lay-out of add-on p.c.b.



REFNR	TYPE	+14Va	-14Va	⊥
N5001	LT1012	7		4
N5002	CA3096		16	
N5004	HA2525	7	4	

REFNR	TYPE	+15Vb	+14Va	+14Vd	+14Vf	-15Vb	-14Va	-14Vd	-19Va	⊥
D5001	TEA1017			7						3
N5008	HA5320	9				5				
N5007	NE5514				4			11		
N5008	LT1012		7				4			
N5011	LM339			3					12	
N5012	LM393			8					4	

Figure 8.55.4 Unit A55 - VERTICAL SIGNAL UNIT - Circuit diagram.



REFNR	TYPE	+14Va	-14Va	⊥
N6001	LT1012	7		4
N6002	CA3096		16	
N6004	HA2525	7	4	

REFNR	TYPE	+15Vc	+14VD	+14Ve	+14Vg	-15Vc	-14VD	-14Ve	-19Va	⊥
D6001	TEA1017			7						3
N6006	HA5320	9				5				
N6007	NE5514				4			11		
N6008	LT1012		7				4			
N6011	LM339			3					12	
N6012	LM393			8					4	

Figure 8.55.5 Unit A55 - VERTICAL SIGNAL UNIT - Circuit diagram.

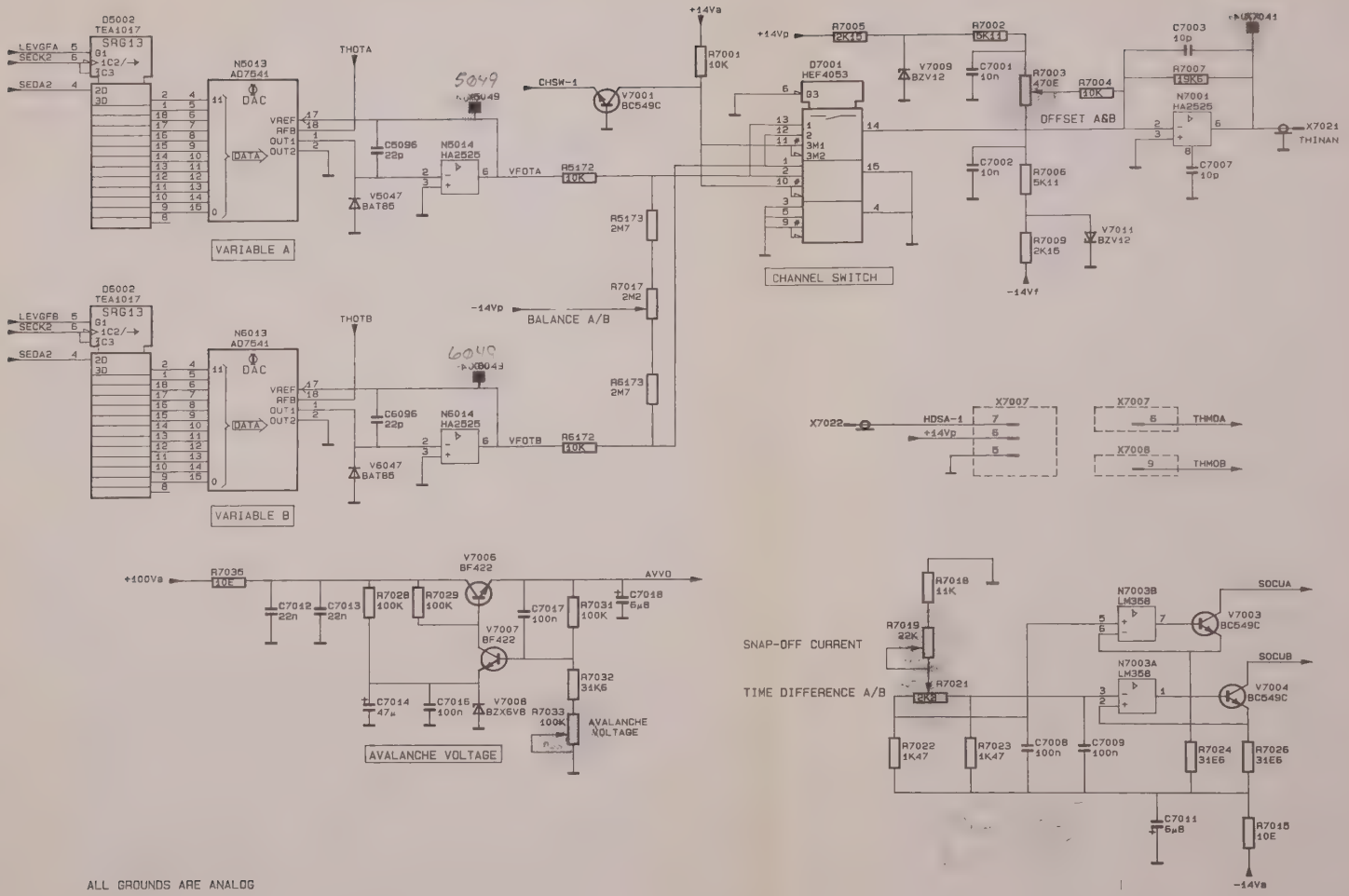


Figure 8.55.6 Unit A55 - VERTICAL SIGNAL UNIT - Circuit diagram.

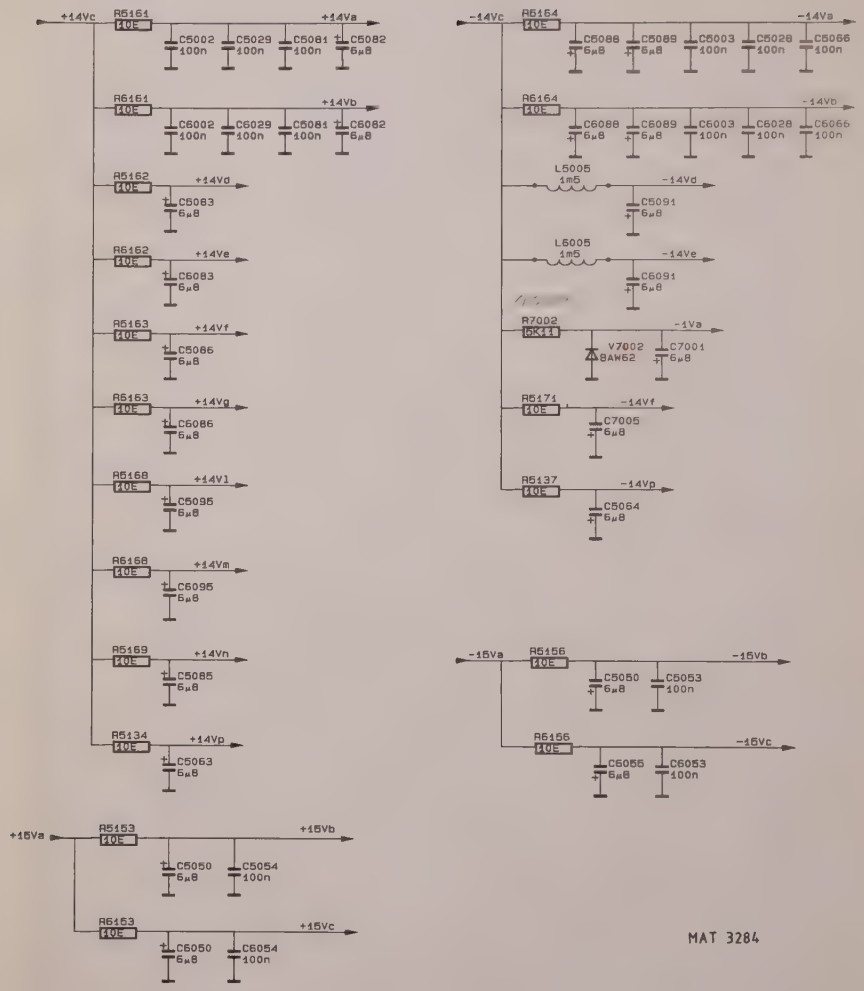
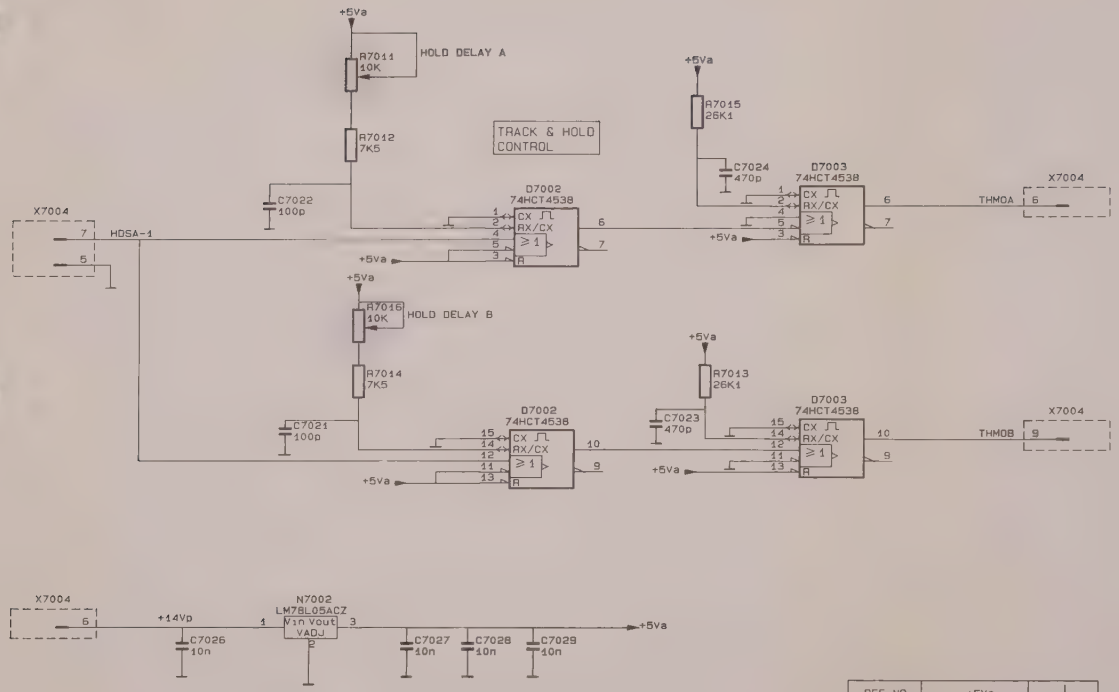


Figure 8.55.7 Unit A55 - VERTICAL SIGNAL UNIT - Circuit diagram.



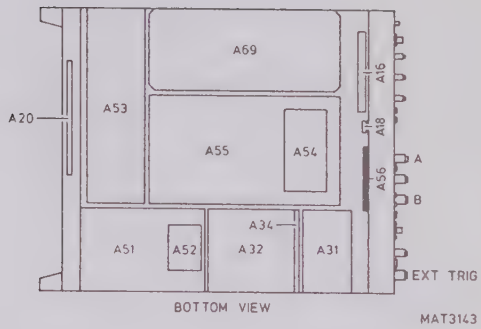
REF.NR	+5Va	⊥ A
D7002	16	8
D7003	16	8

MAT 3286

ALL GROUNDS ARE ANALOG

Figure 8.55.8 Unit A55 - VERTICAL SIGNAL UNIT
Circuit diagram of add-on p.c.b.

UNIT A56 - TRIGGER PICK OFF UNIT



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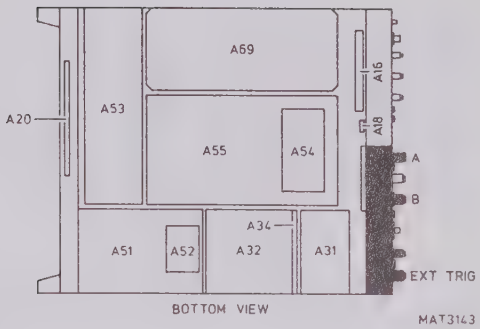
8.56.1 General information..... 8.56-1

8.56.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.54.

UNIT A57 - INPUT UNIT



CONTENTS

8.57.1 Description..... 8.57-1
8.57.2 Signal name list..... 8.57-1

8.57.1 Description

This unit consists of a metal profile on which the following input connectors are fitted:

Description	Connector type	Ref.nr.
A	N	X1
B	N	X2
EXT	BNC	X5
Ground	4 mm banana	X4

Next to the A and B connectors, the probe detection contacts are fitted. They are connected to X7003 on the Vertical signal unit A55. The two trigger pick-offs (unit A56) are fitted on the input connectors.

8.57.2 Signal name list

UNIT 57

Signal name	Description	Signal source	Signal destination(s)
A	Channel A	A57	A57-A69-A54
B	Channel B	A57	A56-A69-A54
EXT	External trigger	A57	A31
PRIF-A	Probe information A	A57	A55
PRIF-B	Probe information B	A57	A55

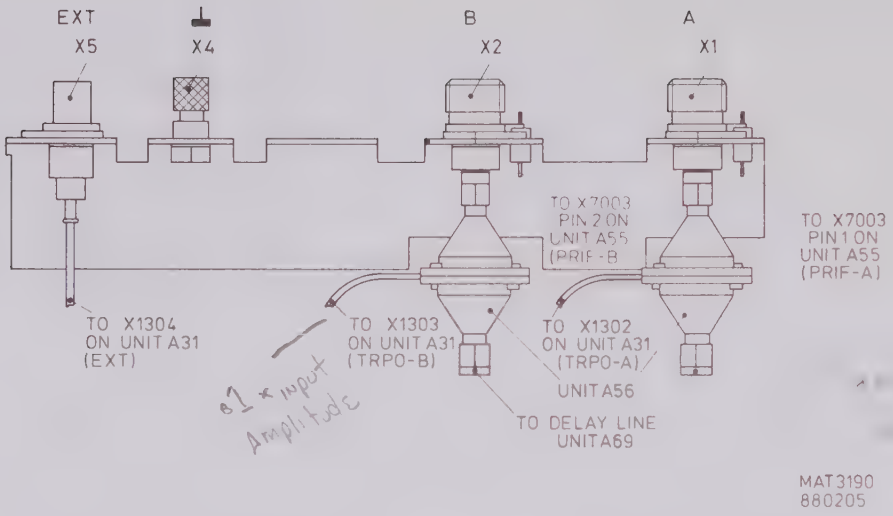
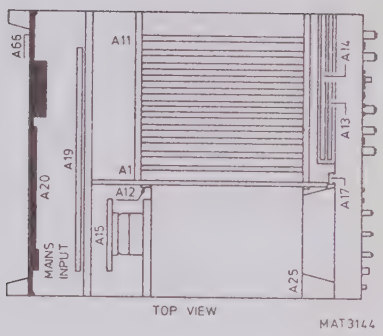


Figure 8.57.1 Unit A57 - INPUT UNIT - Lay-out.

UNIT A66 - ASSY FRAME REAR



CONTENTS

8.66.1 Description..... 8.66-1
8.66.2 Signal name list..... 8.66-1

8.66.1 Description

The assy frame rear module consists of a rear plate on which the following parts are mounted:

- power 2 unit (A20)
- mains entrance with fuseholder and fuse
- mains switch
- fan
- battery pack
- several input/output connectors

The circuit diagram can be found in the drawings of the power 1 unit (A19) and the power 2 unit (A20). It needs no further explanation.

WARNING: To avoid any electrical shock, it is strongly recommended to read section 10.1 first.

The rear plate is connected to the chassis of the oscilloscope with an earth cable. For security this cable should never be removed when the rear plate is taken away from the chassis.

8.66.2 Signal name list

UNIT A66

Signal name	Description	Signal source	Signal destination(s)
BAVO	Battery voltage	A66	A20-A19-A12-A6
FRUVP	Fast reset undervoltage protection	A19	-
FS	Fan supply	A20	-
M1	Mains 1	A66	A19
M2	Mains 2	A66	A19
PE	Protective earth	A66	A19
X-PL	X plot	A1	-
Y-PL	Y plot	A1	-
PENLIFT	Penlift	A1	-

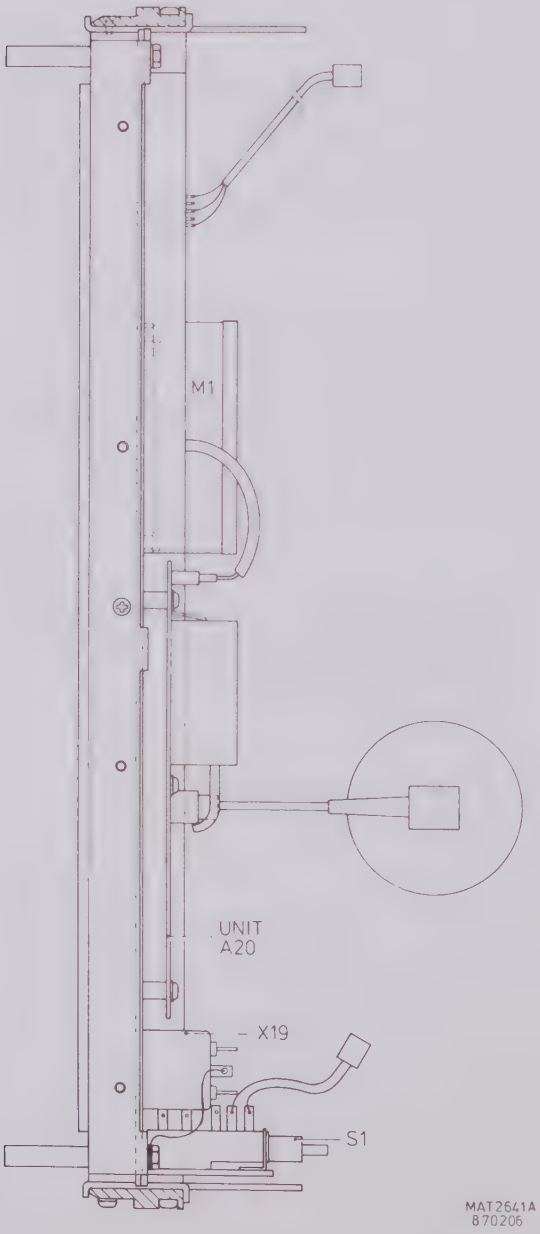


Figure 8.66.1 Unit A66 - ASSY FRAME REAR - p.c.b. lay-out.

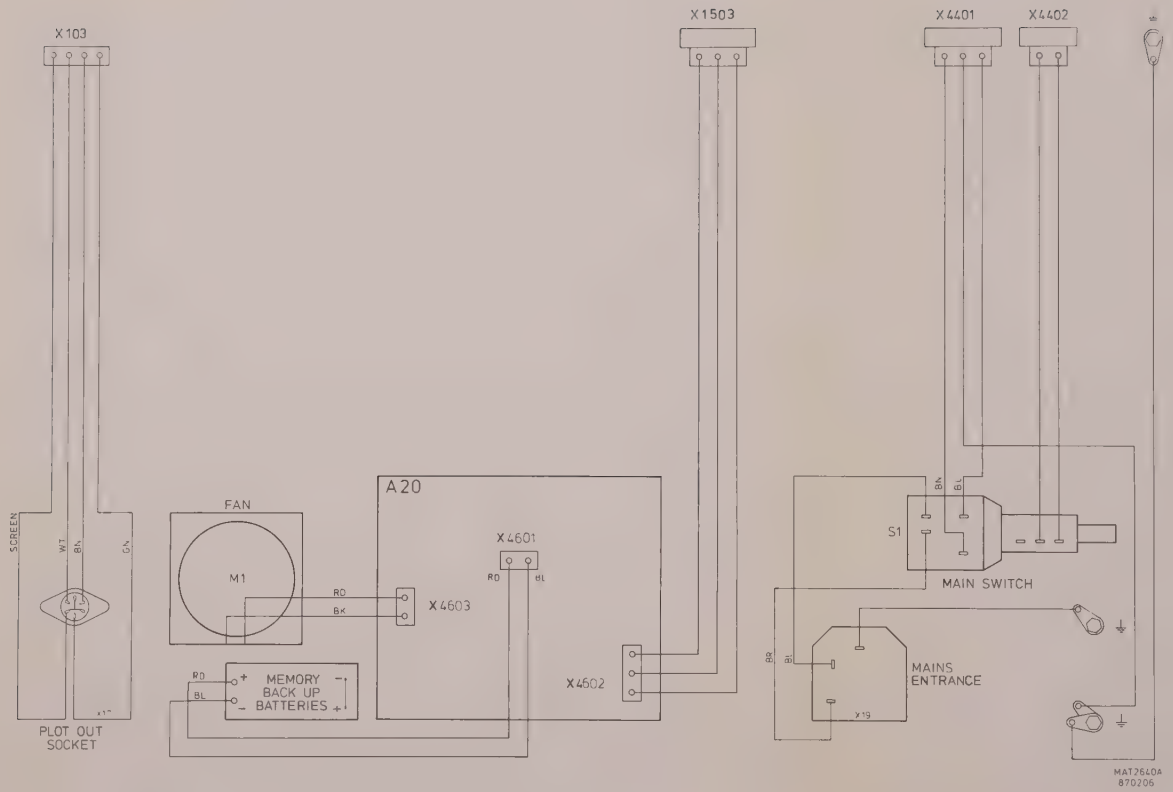
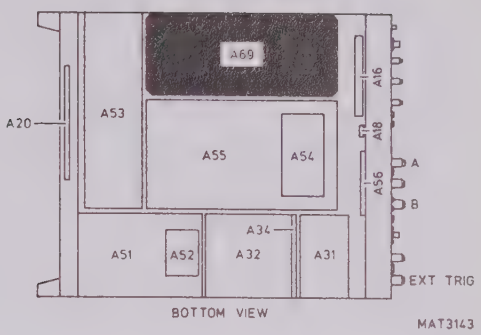


Figure 8.66.2 Unit A66 - ASSY FRAME REAR - circuit diagram.

UNIT A69 - DELAY LINE UNIT



CONTENTS

8.69.1 General information..... 8.69-1

8.69.1 General information

For the circuit description, signal-name list, p.c.b. lay-out and circuit diagram of this unit refer to section 8.54.

ADJUSTING PROCEDURE 9

ADJUSTING PROCEDURE

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9.1 General information.....9-1
9.2 Recommended test and calibration equipment.....9-2
9.3 Adjusting procedure.....9-7

9.0 ADJUSTING PROCEDURE

9.1 GENERAL INFORMATION

The following information provides the complete adjusting procedure for the instrument. As various control functions are interdepedent, a certain order of adjustment is necessary.
The procedure is, therefore, presented in a sequence which is best suited to this order, cross-reference being made to any circuit which may affect a particular adjustment.

Before any adjustment, the instrument must attain its normal operating temperature.

- Warming-up time under average conditions is 30 minutes.
- Where possible, the instrument performance should be checked before any adjustment is made.
- All limits and tolerances given in this section are calibration guides, and should not be interpreted as instrument specifications unless they are also published in chapter 3.
- Tolerances given are for the instrument under test and do not include test equipment error.
- The most accurate display adjustments are made with a stable, well-focused low intensity display.
- All controls which are mentioned without item numbers are located on the outside of the instrument.

WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts, and also accessible terminals may be live. The instrument shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair during which the instrument will be opened. If afterwards any adjustment, maintenance or repair of the opened instrument under voltage is inevitable, it shall be carried out only by a qualified person who is aware of the hazard involved. Bear in mind that capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.

9.2 RECOMMENDED TEST AND CALIBRATION EQUIPMENT

Type of instrument	Specification	Used for	Example of required instruments
1. Constant amplitude sine-wave generator.	Freq. 50kHz.. 1000MHz Voltage 10mV.. 5Volt	Bandwidth check of vertical channels and triggering	Tektronix SG503 + SG504
2. Frequency doubler	Input voltage 2 ... 5V. Input freq. 100 ... 1000 MHz	Checking bandwidth and trigger sensitivity	HP 11721 A
3. Time marker generator	Repetition rate 20us ... 1ns	Checking and adjusting of time base	Tektronix TG501.
4. Square-wave calibration generator	Output voltage into 1 M.ohm 10mV ... 2V. Halves into 50 ohm. Duty cycle 50%	Checking and adjusting of vertical sensitivity.	Tektronix PG506
5. Fast-rise square-wave generator	Output voltage 200mV/rise time 70 ps or less. Frequency 50kHz	Checking the sq. wave response.	Tektronix 284
6. BNC coax cables, attenuators (6, 14, 20 and 26 dB), adaptors between N, GR and BNC	Good quality types that are applicable up to 2GHz	Checking the sq. wave response and trigger bandwidth	

Type of instrument	Specification	Used for	Example of required instruments
7. LF sine-wave /sq.-wave generator	Sine-wave Freq.: 1Hz... 1MHz Voltage: 0... 5 volt Square-wave Freq.: 1Hz... 1MHz Voltage: 0... 5 volt	Checking various specification points	Philips PM5131
8. Trimming tool kit	--	Adjustments	Philips SBC317 (ord. number 4822 310 50095)
9. Variable mains transformer.	Well-insulated Output voltage 90...264VAC	Checking influence of mains voltage variations and adjustment of power supply.	Philips ord. number 2422 529 00005
10. Oscilloscope	The bandwidth must be 100 MHz or more	Checking the instrument under test	Philips PM3267
11. Digital multimeter	Wide voltage, current and resistance ranges. Required accuracy 0,1%	Checking and adjusting of the instrument	Philips PM2718
12. Power splitter+ 2 equal coax cables	Equal output voltages. Bandwidth 2GHz or more	Checking and adjusting of time difference and common mode rejection ratio.	
13. 3 miniature coax cables	Length > 20cm. Type such as used internally in this oscilloscope	Adjustment of frequency detector	For ordering numbers refer to chapter 15.3

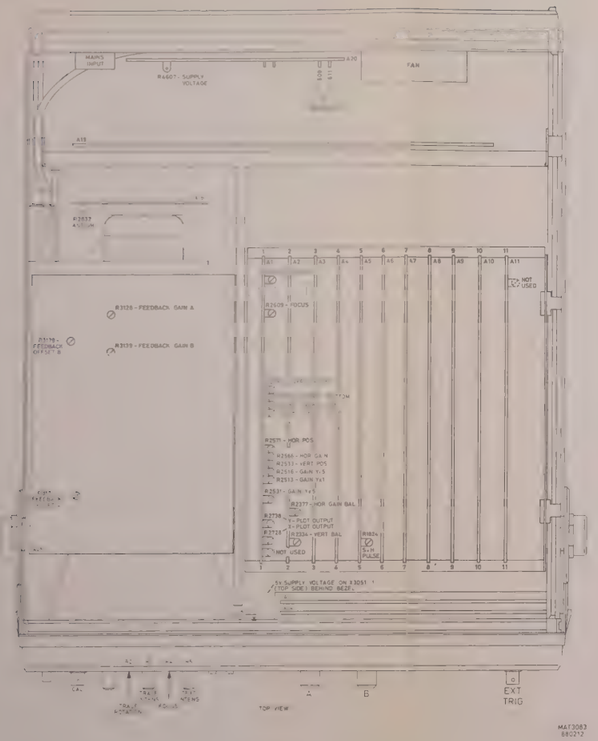


Figure 9.1 Adjustment points, top view.

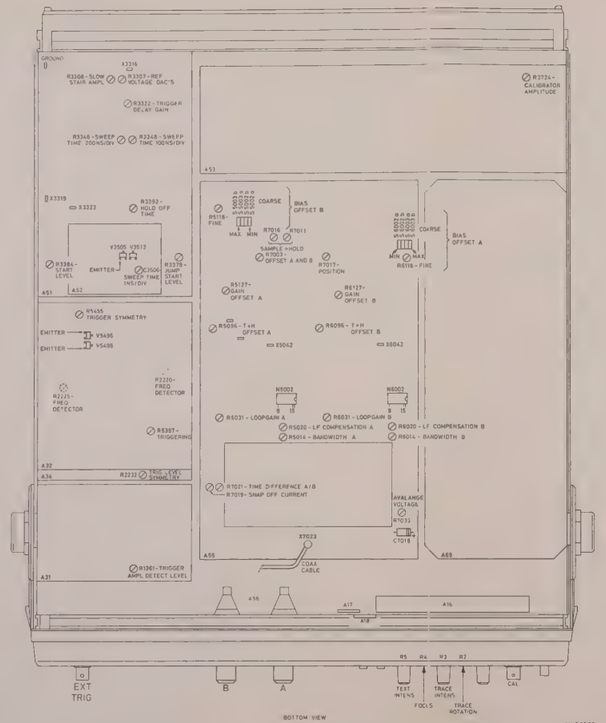


Figure 9.2 Adjustment points, bottom view.

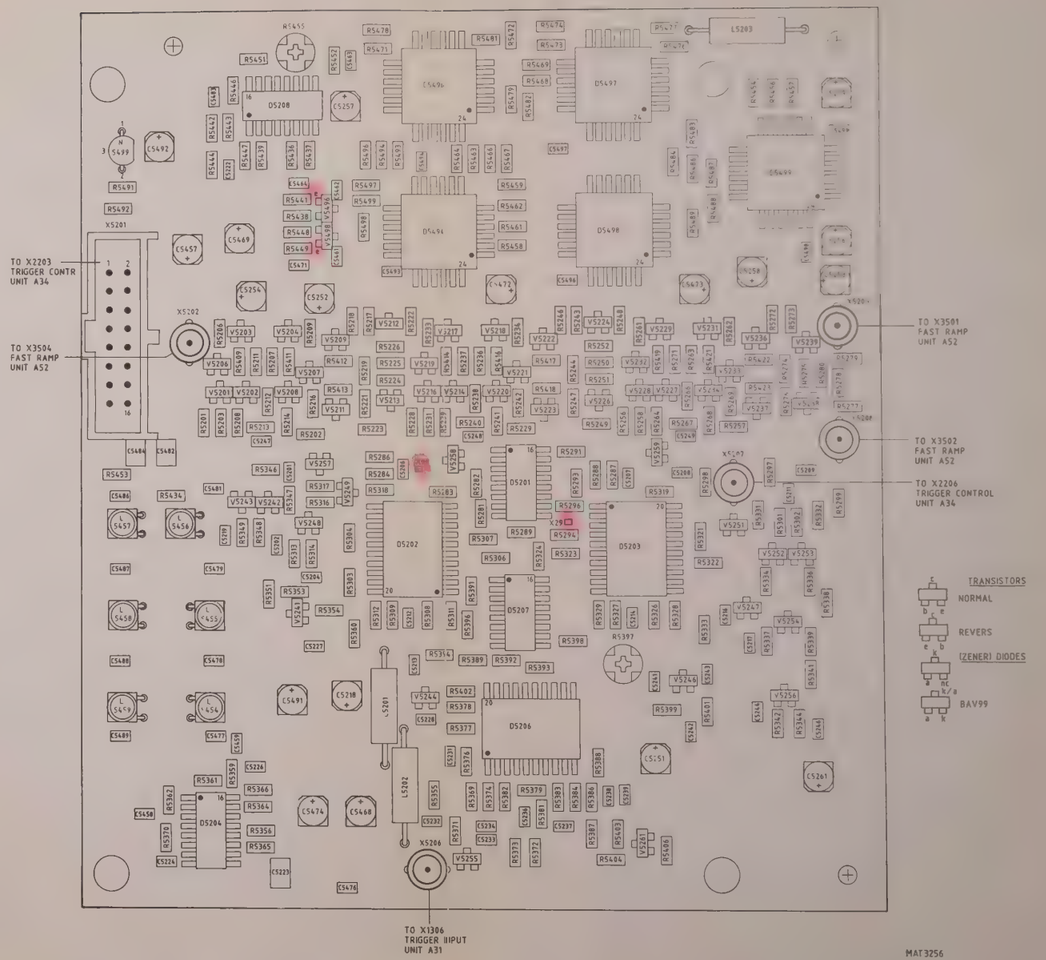


Figure 9.3 Measuring points on three-stage trigger unit (unit A32).

9.3 ADJUSTING PROCEDURE

9.3.1 Preparation and list of abbreviations.

Some of the adjustments are done with the use of the service menu. This menu can be switched-on by depressing the top and bottom softkeys together at the same moment. After this action you must select CHECK & ADJ. You are now in the part of the service menu that must be used during certain adjustments. Now you can for instance select the part that helps to adjust the display section.
This part is called DISPLAY. By means of the softkeys NEXT and PREVIOUS you are able to scroll downwards or upwards through the steps of the DISPLAY menu. These steps are DISPLAY 1, DISPLAY 2, ... and so on. During the adjustment procedure it is assumed that the operator knows how to select a certain part of the service menu.
The following abbreviations are used in the adjustment procedure:

bal.	= balance
cal.sq.wave	= calibrated square wave
div	= division of the measuring graticule
DVM	= digital voltmeter
hor.	= horizontal
SM	= service menu (followed by the step that must be selected)
M.OSC	= measuring oscilloscope; measurements via 10:1 probe, given scope sensitivity does not incorporate probe attenuation factor
sq.wave	= square wave

Note: generator output voltages are peak-to-peak values.

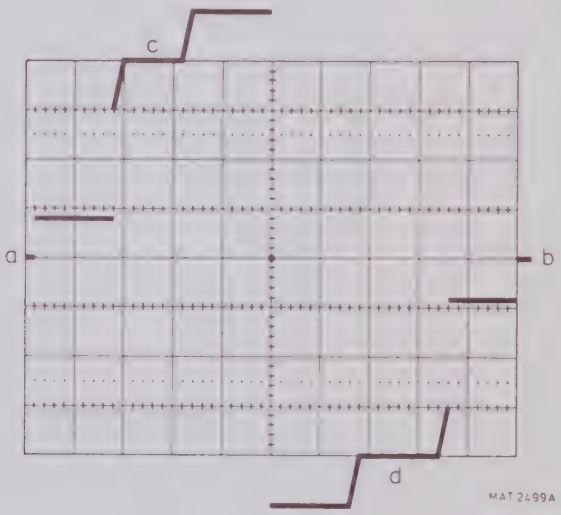
Important: Use always an isolated adjustment tool.

9.3.2 POWER SUPPLY + CAL VOLTAGE

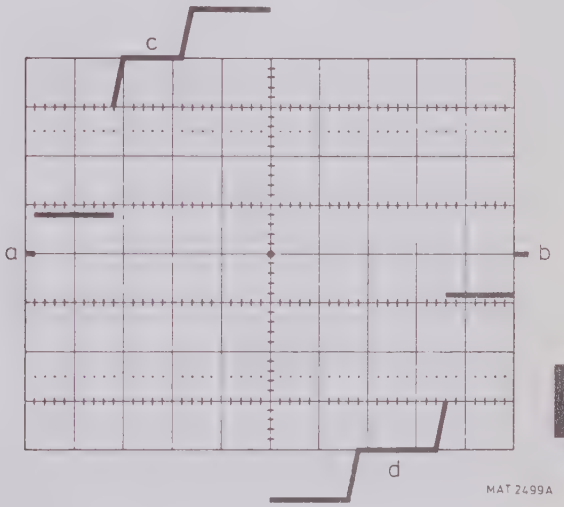
Adjustment	Adj. point/ unit	Settings + requirement
-Supply voltage	R4607/A20	10.00 V (+/- 0,1V) between X4609 and X4611 with d.c. voltage range of DVM.
-Calibrator amplitude	R3724/A53	Terminate CAL output with BNC into banana adaptor. Connect the DVM (dc-voltage range) with the adaptor outputs. Adjust R3724 to 1000 mV (+/- 2mV) read-out on DVM.

9.3.3 DISPLAY SECTION

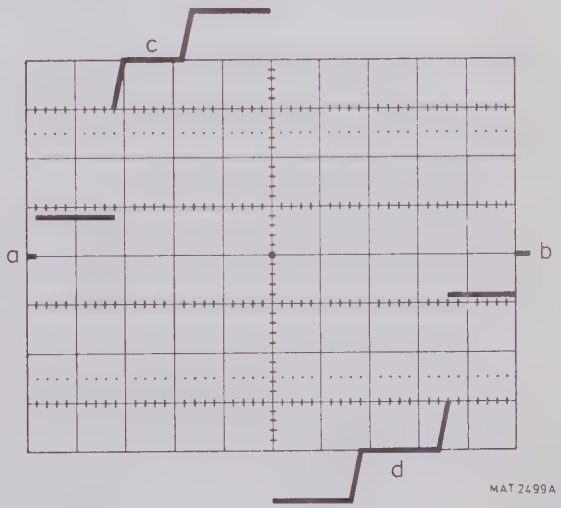
-Intensity	R2637/A1 R3/front R5/front	SM: DISPLAY Ø, R3 and R5 (INTENS) 90° from counter clockwise stop. Adjust R2637 for test pattern + text just visible

Adjustment	Adj. point/ unit	Settings + requirement
-Focus + astig-matism	R2609/A1 R2832/A15	SM: DISPLAY Ø, R3/R5/R4 (FOCUS) at front panel in mid position. Text + test pattern must be equallysharp across screen, also if intensity is changed.
-Trace rotation	R2/front	SM: DISPLAY Ø. Horizontal line must be in parallel with graticule.
-Presets necessary in case that oscilloscope is totally misadjusted	R2682/A1 R2658/A1 R2659/A1 R2678/A1	}All adjustments fully counter }clockwise } }
	R2513/A1 R2533/A1 R2566/A1 R2571/A1	}Adjust roughly for a correct }position of the text on the }screen }
-Vertical balance	R2334/A2	SM: DISPLAY 1 (see figure below).  Adjust for minimal vertical jump of the lines a and b.
-Hor. gain balance	R2377/A2	SM: DISPLAY 2. Adjust for minimal jump of dot in screen centre.

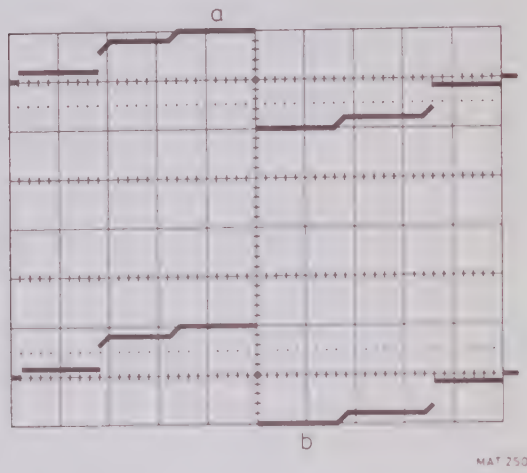
Adjustment	Adj. point/ unit	Settings + requirement
-Hor. position + Vert. position	R2571/A1 R2533/A1	SM: DISPLAY 3. Position the dot in the graticule centre. Allowed deviation +/- 0,1 div in hor. and vert. direction. Can be used to compensate for small shifts of the centre dot under SM DISPLAY 4, 5 and 6 so that the gain adjustments become more accurate.
-Gain Yx5	R2531/A1	SM: DISPLAY 4. Adjust for 8 div vertical distance between the two horizontal lines.
-Gain Yx1	R2513/A1	SM: DISPLAY 5 (see fig. above). Adjust for 8 div vertical distance between the lines c and d.



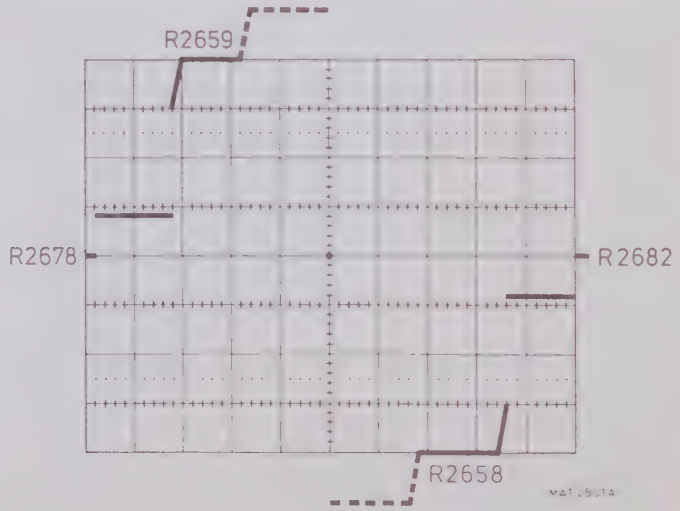
-Hor. gain	R2566/A1	SM: DISPLAY 5 (see fig. below)



Adjustment	Adj. point/ unit	Settings + requirement
		Adjust to 10 div vertical distance between starting point of the small lines a and b.
-Gain Y/5	R2516/A1	SM: DISPLAY 6 (see fig. below)



		Adjust for 8 div vertical distance between the lines a and b.
-Overscan suppression	R2678/A1	SM: DISPLAY 7 (see fig. below) Turn R2678 in clockwise direction until left-hand test pattern does not become longer anymore.
	R2682/A1	Turn R2682 in clockwise direction until right-hand test pattern does not become longer anymore.
	R2658/A1	Bottom test pattern 0,1 div outside graticule.
	R2659/A1	Top test pattern 0,1 div outside graticule.



9.3.4 HORIZONTAL SECTION

Adjustment	Adj. point/ unit	Settings + requirement
-Reference voltage DAC´s	R3307/A51 X3316/A51	Adjust for 8,92V (+/- 90 mV) between X3316 and mass. Voltage measured with DVM.
-Slow stair amplitude	R3308/A51 X3319/A51	Trig.MODE: SYNC´ED Time/div: 1 ns Trig. DELAY: Ø Adjust the signal amplitude at X3319 to 4 V peak-to-peak. Measured with oscilloscope (M.OSC).
-Hold off time	R3392/A51 X3323/A51	A input: no signal Time/div: 20 ns Trig. MODE: SYNC´ED Trig. DELAY: Ø HOLD OFF: MINimal Hor. resolution: 512 samples Connect M.OSC with X3323. Adjust the duration of the hold-off sawtooth on the screen of the M.OSC to 45us (+/- 2us). Select a horizontal resolution of 64 (via softkey ACQ MODE). Check for a duration of the hold-off sawtooth of approximately 150 us.
-Start level	R3384/A51	Ch. A input: CAL voltage. Turn R3384 fully clockwise. Press AUTO SET. TIME/DIV: 500ns. Adjust X POSITION so that start of trace is within screen. Adjust R3384 so that signal slope is 0,06 div (+/- 0,04 div) from start of trace.
-Jump start level	R3379/A51 V3505E/A52 X3316/A51	SM: FAULT FIND, DAC TEST, FAST RAMP. Ch. A input: CAL voltage. M.OSC: Ch. A (50mV/div., DC coupl.) to V3505/emitter; Ch. B (50mV, DC coupl, INVERT, ADD) to X3316, position top level of the signal within the screen area of the M.OSC Adjust R3379 for minimal jump of this sawtooth. The jump is well visible if the M.OSC is not triggered. Remove the probes and press AUTO SET to leave the SM. Note: check the start level again. If necessary, readjust R3384 slightly.

Adjustment	Adj. point/ unit	Settings + requirement
-Sweep time 200 ns/div	R3346/A51	A input: 0,2 us time markers. Vertical: Ch. A, 200 mV/div, Time/div: 200 ns. Trigger mode: TRIG. Trig. DELAY: Ø Adjust the time markers on the screen.
-Sweep time 10 ns/div	C3506/A52	A input: 10 ns time markers Time/div: 10 ns. Trig mode: COUNT DOWN. Adjust the time markers on the screen
-Sweep time 100 ns/div	R3348/A51	A input: 0,1 us time markers Time/div: 100 ns/div. Trig. mode: TRIGGER. Adjust the time markers on the screen.
-Trig. delay gain	R3322/A51	Ch. A: 1 us time markers. Trig. mode: TRIGGER. TIME/DIV: 100ns. Trigger delay: Ø. Align signal slopes with 1th and 11th graticule line with X POSITION. New trigger delay: 10 div. Adjust R3322 to previous signal slope position.
9.3.5 VERTICAL SECTION		
-Bandwidth A(B)	R5014/A55 N5002/9,15 (R6014/A55 N6002/9,15)	Unplug coax cable X7023 on A55 and remove 2 screening boxes from A55. Adjust voltage between pin 9 and 15 of N5002 (N6002) to 4V (+/- 10 mV) measured with a DVM. Reinstall the coax cable again.
-Avalanche voltage & snap-off current	R7033/A55 R7019/A55 C7018/A55	Put R7019 in mid position. Ch. A: CAL voltage. Press AUTO. TIME/DIV: 1 us. Position signal inside graticule with OFFSET. Adjust R7033 to 21V (+/- 0,5V) across C7018.

Adjustment	Adj. point/ unit	Settings + requirement
-Time difference Ch. A, B	R7021/A55	Ch. A and B input: HF sq.wave 200mV /50kHz/rise-time <70ps via power splitter and 2 identical coax cables. Press AUTO. TIME/DIV: 1 us. Adjust LEVEL so that display starts at leading edge of signal. TIME/DIV 1 ns. Select via MAGN/DELAY menu TB sweep speed 100 ps/div and keep leading edge in graticule center by adjusting the DELAY value. Select DISPLAY MAGNIFY to *2. Adjust R7021 to a time difference of <0,1 div between A and B trace. If necessary correct vertical shift with OFFSET and make amplitudes equal with VARIABLE control.
-Sample + hold pulse A(B)	R7011/A55 (R7016/A55)	Ch. A(B) input: sq.wave 100kHz/300 mV. Ch. A(B) on, 50mV/div, EYE PATTERN. TIME/DIV: 1 us. Adjust R7011 (R7016) to maximum signal amplitude on the screen.
-Feedback gain A(B)	R3128/A25 (R3139/A25)	A(B) input: calibrated d.c. voltage 0,2V into 1 M.ohm (halves into 50 ohm. Generator adjusted to d.c. mode via switch in left-hand side panel. EYE PATtern: off. Ch. A(B): 20 mV/div. Position time base line on lower graticule line without input signal. Connect generator and check for vertical shift of time base line of 5 div. If necessary readjust R3128 (R3139). Note: this adjustment influences the vertical offset of the signal so that the optimal calibration is obtained after repeatedly performing the adjustment.
-Feedback offset A(B)	R3171/A25 (R3179/A25) X5042/A55 (X6042/A55)	A(B) input: no signal Vertical: EYE PAT A(B) Adjust voltage at X5042 (X6042) on unit A55 to 0 V (+/-50mV) with DVM. Note: reinstall the screening boxes on unit A55 again.
-LF compensation A(B)	R5020/A55 (R6020/A55)	A(B) input: CAL voltage. Vert. mode: EYE PAT, ch. A(B) on, 100 mV/div. TIME/DIV: 2 us. Adjust for a straight pulse top.

Adjustment	Adj. point/ unit	Settings + requirement
-Loop gain A(B)	R5031/A55 (R6031/A55)	A(B) input: calibrated d.c. voltage 0,5V into 1 M.ohm (halves into 50 ohm). Generator adjusted to d.c. mode via switch in left-hand side panel. EYE PATtern: on. Ch. A(B): 50 mV/div. Position time base line on lower graticule line without input signal. Connect generator and check for vertical shift of time base line of 5 div. If necessary readjust R5031 (R6031). Note: this adjustment influences the vertical offset of the signal so that the optimal calibration is obtained after repeatedly performing the adjustment. Note: switch the generator back from d.c. to 1 kHz sq.wave mode.
-T&H offset A(B) & channel switch	R5096/A55 (R6096/A55) X7023/A55	A(B) input: no signal Vert. mode: EYE PAT, A AND B, 200 mV/div Time/div: 200 ns Trig. mode: SYNC´ED. Unplug the coax cable from X7023. Put the Y-POSITION in CALIBRATE via the DISPLAY menu. Adjust R5096 (R6096) for minimal trace jump when operating VARIABLE control A(B) between min and max.
	R7017/A55	Position both lines upon each other with R7017.
	R7003/A55	Position both lines in vertical mid of screen. Reinstall X7023 again.
-Gain offset A(B)	R5127/A55 (R6127/A55)	Ch. A(B): on, 50mV/div, no input signal. TIME/DIV: 200ns. Trig. mode: SYNCHRONIZE. Via OFFSET menu A(B): ADJUST, then ZERO and then DIV. Adjust R5127 (R6127) to a trace shift of 1 div when operating UP/DOWN.

	Adjustment	Adj. point/ unit	Settings + requirement
	-Bias offset A(B)	R5118/A55 (R6118/A55)	Adjust Offset to ZERO via the OFFSET menu. Adjust R5118 (R6118) so that trace is as close as possible to vertical mid of screen. Check this for increasing input sensitivity (AMPL/DIV).
		S5002a,b/A55 S5003a,b/A55 (S6002a,b/A55) (S6003a,b/A55)	If this cannot be adjusted, put R5118 (R6118) in mid position. AMPL/DIV: 200mV. Adjust the 4 switches S5002a (smallest effect) ... S5003b (biggest effect) so that the channel A line is as close as possible to vertical mid of screen. Do this successively for increasing input sensitivity (AMPL/DIV). Do finally the fine adjustment with R5118. Do the same for ch. B with the 4 switches S6002a (smallest effect) .. S6003b (biggest effect). Do the fine adjustment with R6118.
9.3.6	TRIGGERING		
	-Trig.level symmetry	R2232/A34 X29/X30/A32	A,B input: no signal Press AUTO SET. Select trig. MODE SYNC´ED (functions as LEVEL reset) and then TRIG. Adjust the voltage between X29 and X30 to 0V (+/-1mV) with a DVM.
	-Trigger symmetry	R5397/A32 R5455/A32	Ch. A input: sine-wave 100MHz/8mV Ch. A: on and at 5mV/div. Trig mode : TRIGGER and HIGH SENSE. Source: A TIME/DIV: 5ns. Turn R5397 clockwise. Then turn it counterclockwise until signal is triggered and just free from distortion. This is well visible at high intensity. Trig. mode: SYNCHRONIZE. Remove the input signal. Adjust R5455 to 0V (+/- 5mV) between the emitters of V5496 and V5498 with a DVM.

Adjustment	Adj. point/ unit	Settings + requirement
		Trig mode: TRIGGER. Ch. A input: sine-wave 150 kHz/11,3 mV (= 8 mV + 3 dB). TIME/DIV: 5 us. Check if signal is correctly triggered (adjust LEVEL if necessary). Check if signal is free from distortion (turn intensity high): if not, turn R5397 slightly counterclockwise. Do the above check with a sine-wave 150 kHz/113 mV (=80 mV + 3 dB) with trigger mode LOW SENS and AMPL/DIV 50 mV. If necessary, readjust R5397 slightly in counterclockwise direction.
-Trigg. amplifier detection level	R1361/A31	A input: sine wave, 1GHz, 40 mV. Vert.mode: A, 10 mV/div. Trig.mode: COUNT DOWN, HIGH SENSE. Signal must be triggered. Switch to AUTO SELECT. Turn R1361 fully counterclockwise. Turn R1361 clockwise to the point that signal is just not triggered. Turn R1361 slightly counterclockw. Push COUNT DOWN and then AUTOSELECT and check for a triggered display: if not, turn R1361 again slightly counter-clockwise. Check for correct triggering between COUNT DOWN and AUTO SELECT across the bandwidth range 0,2 .. 2GHz while keeping the signal amplitude at 4 div on screen. If this is not good, turn R1361 again slightly counter-clockwise.

Adjustment	Adj. point/ unit	Settings + requirement
-Switching of frequency detector	R2220/A34 R2225/A34	Ch. A input: sine-wave 120MHz/500 mV. Vertical: ch. A on and at 200 mV/div. Trig. source: A. Trig. mode AUTO SELECT. TIME/DIV: 5ns. Increase generator frequency and check that triggering switches from TRIGGER to COUNTDOWN at 160MHz. Decrease generator frequency and check that triggering switches from COUNTDOWN to TRIGGER at 150MHz. If the above figures are not met: detach unit A32 so that R2220 and R2225 can be reached. Three coaxial cables must be replaced by types longer than 20 cm in order to make enough space between the units A32 and A34. Turn R2220 fully clockwise, R2225 fully counterclockwise. Select signal frequency of 160MHz. Adjust R2220 towards the position that trigger switches from TRIGGER to COUNTDOWN. Select signal frequency of 150MHz. Adjust R2225 towards the position that triggering switches from COUNT DOWN to TRIGGER. Install A32 again.
-Triggering	R5397/A32	Ch. A input: sq.wave 120mV/100Hz .. 1MHz. Vertical: ch. A on and 20 mV/ div. Trig. source: A. Trig mode: TRIGGER, HIGH SENSE. TIME/DIV: adjust for good signal display. Check that the displayed sq.wave is free from noise/distortion across given frequency range. If not, turn R5397 slightly clockwise. Repeat the above procedure with a sq.wave 1,2V/100Hz .. 1MHz and trig. mode: LOW SENS.

9.3.7 PLOT OUTPUTS

Adjustment	Adj. point/ unit	Settings + requirement
-Plot output voltage	R2738/A1 R2728/A1	Plug plot cable into DIN socket at rear panel. Banana plugs: red: Y-output, blue: X-output, black: mass. A and B input: sq.wave, 10 kHz, 1,2 V. Press AUTO. Position the two square wave signals in the vertical mid of the screen. Ch. A,B AMPL/DIV: 100 mV so that signal amplitude is higher then the 10 div vertical input range. TIME/DIV: 10 us. Select A VERSUS B via DISPLAY mode and switch register RØ on. Select 20 ms/DT via menus SAVE/PLOT SELECT and ANALOG. Connect a DVM with the plot Y-output and press SAVE/PLOT and then softkey ANALOG. The plot function is active as long as a dot moves from left to right on bottom graticule line. The plot action can be stopped inbetween with softkey STOP. Adjust R2738 for a max. DVM reading of 1.000 V. Connect DVM with the plot X-output and press softkey ANALOG. Adjust R2728 for a max. DVM-reading of 1.000 V.

DISASSEMBLING AND ASSEMBLING 10

DISASSEMBLING AND ASSEMBLING

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10.0 DISASSEMBLING AND ASSEMBLING

10.1 REMOVING THE INSTRUMENT COVERS

See chapter 5, section 5.2.

WARNING: The opening of the covers exposed live parts and also accessible terminals may be live.
The instrument shall be disconnected from all voltage sources before any replacement or maintenance or repair, during which the instrument will be opened.
Capacitors inside the instrument may still be charged, even if the instrument has been separated from all voltage sources.

To avoid shocks the high voltage capacitor C4616 on POWER 2 unit A20 at the inner side of the rearpanel has to be discharged. This can be done by connecting a 1 Mohm resistor from the node of capacitor C4616 and the EHT transformer D4601 to the chassis of the oscilloscope. This node is marked with an X in figure 10.1.

The E.H.T. cable is permanently connected to the E.H.T. unit (disconnection at C.R.T.).
When the E.H.T. cable to the post-acceleration anode of the C.R.T. is disconnected at the C.R.T. end, the E.H.T. cable must be discharged immediately by shortening it to the chassis of the oscilloscope.

10.2 REPLACEMENTS

Standard parts

Electrical and mechanical replacement parts can be obtained through your local Philips organisation or representative. However, many of the standard electronic components can be obtained from other local suppliers.
Before purchasing or ordering replacement parts, check the parts list for value tolerance, rating and description.

NOTE: Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special parts

In addition to the standard electronic components, some special components are used.
These components are manufactured or selected by Philips to meet specific performance requirements.

Transistors and integrated circuits

Transistors and integrated circuits should not be replaced unless they are actually defective. If removed from their sockets during routine maintenance return them to their original sockets. Unnecessary replacement or switching of semiconductor devices may affect the calibration of the instrument.
When a transistor is replaced, check the operation of the part of the instrument that may be affected.

WARNING: Handle silicone grease with care. Avoid getting silicone grease in the eyes. Wash hands thoroughly after use.

Any replacement component should be of the original type or a direct replacement. Bend the leads to fit the socket and cut the leads to the same length as on the component being replaced.

10.3 REMOVING THE PLUG-IN PRINTED CIRCUIT BOARDS

The plug-in boards are:

A1 Final amplifier
A2 Display dac
A3 Display control
A4 Display memory
A5 GRAM
A6 UP board
A7 Option (Interface)
A8 DPU control
A9 DPU
A10 Option
A11 ADC + T&H

These plug-in units can easily be removed (after removing the bracket and the various cables) with the aid of the red handles.

If a plug-in board is removed it can be placed on an extension board to do measurements.
For more information about the extension board see section 13.3.3.

WARNING: The plug-in boards have to be replaced at the correct locations to prevent damage.

10.4 REMOVING AND MOUNTING THE REAR PANEL

- Take security measures (see section 10.1).
- Unscrew the four screws marked with A in figure 10.1.
- Unscrew the four opposite screws at the bottom side.

WARNING: If the screws are removed the oscilloscope may not stand on its rear side.

- Unscrew the two screws marked with B.
- Unscrew the remaining opposite screw at the bottom side.
- Pull the rear panel out of the oscilloscope and lay it down. It may be necessary to shift through the E.H.T. cable to the C.R.T.

In this situation the oscilloscope can operate and measurements can be done.
Because connector X4604 of unit A20 is disconnected, the high voltage is not present, so nothing can be seen on the screen.
Also the power supply is not fully loaded, because the distribution unit A53 is not connected.
To test the power supply under full load, the extension board for the plug in units can be used as shown in figure 10.2.
It is also possible to use a dummy load.
This is specified in section 13.2.

WARNING: If the osciloscope is operating, parts of POWER 1 unit A19 are at mains potential.

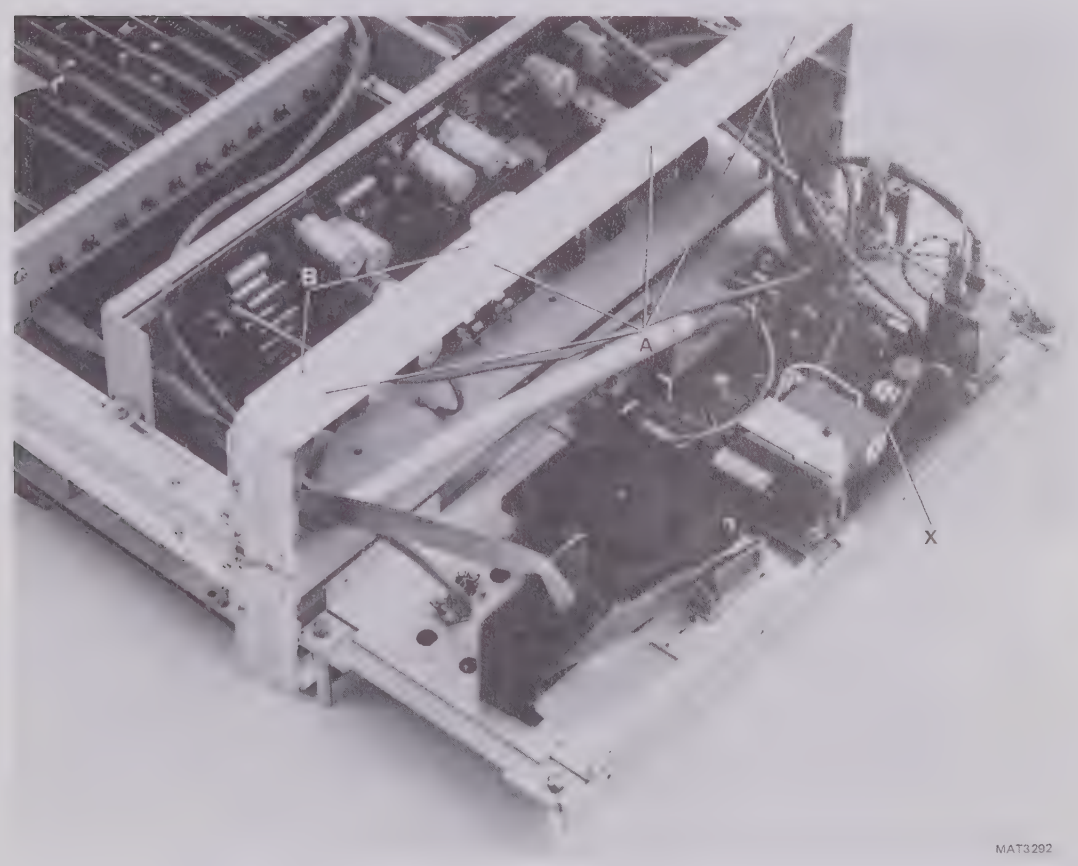

Figure 10.1 Removing the rear panel.

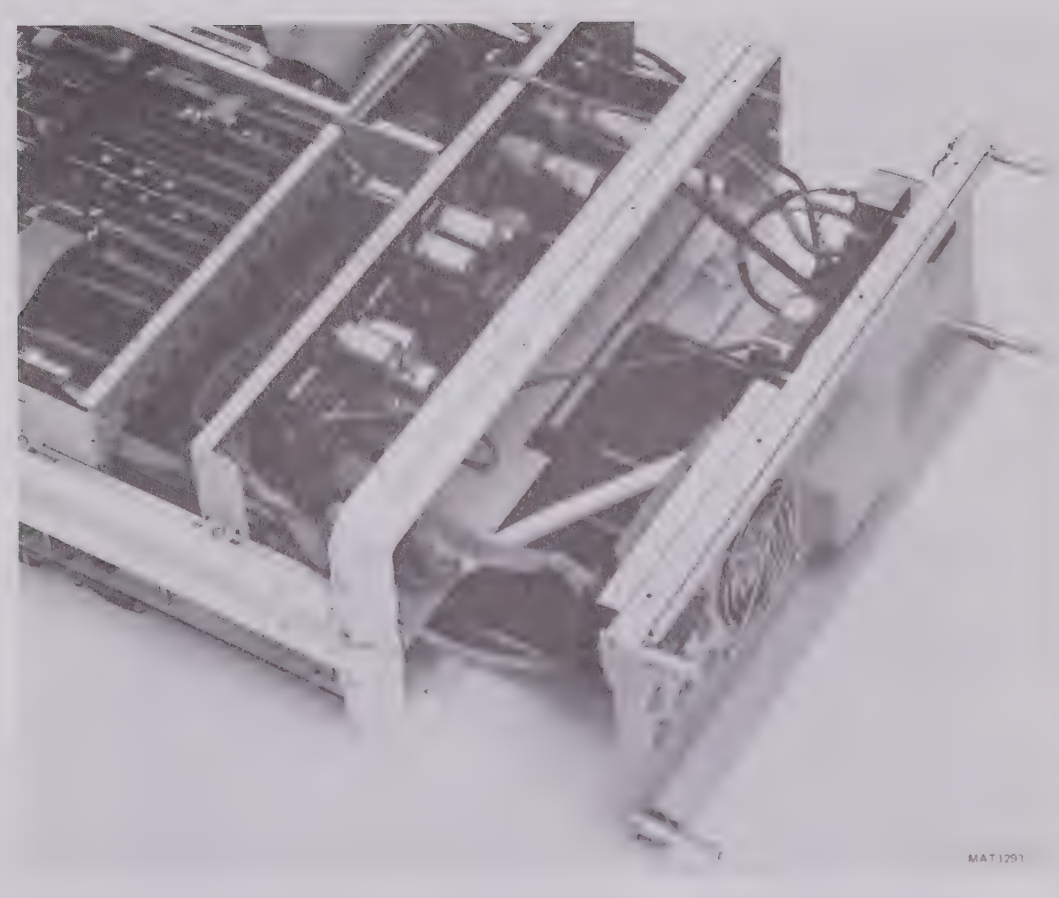

Figure 10.2 Use of the extension board for the rear panel.

To reinstall the rear panel the above mentioned steps have to be done in reverse order.

Special attention is asked for:

- The cable from the mains switch to connector X4401 on unit A19 has to be positioned as much as possible between capacitors C4416 + C4417 and the side of the oscilloscope, to pick up the less interference from transformer T4401.
- The high voltage cable from the E.H.T. transformer should not touch transistor V4612.

10.5 ACCESS TO THE TRIGGER CONTROL UNIT

To get access to the trigger control unit A34 the three stage trigger unit A32 can be turned up as shown in figure 10.3.

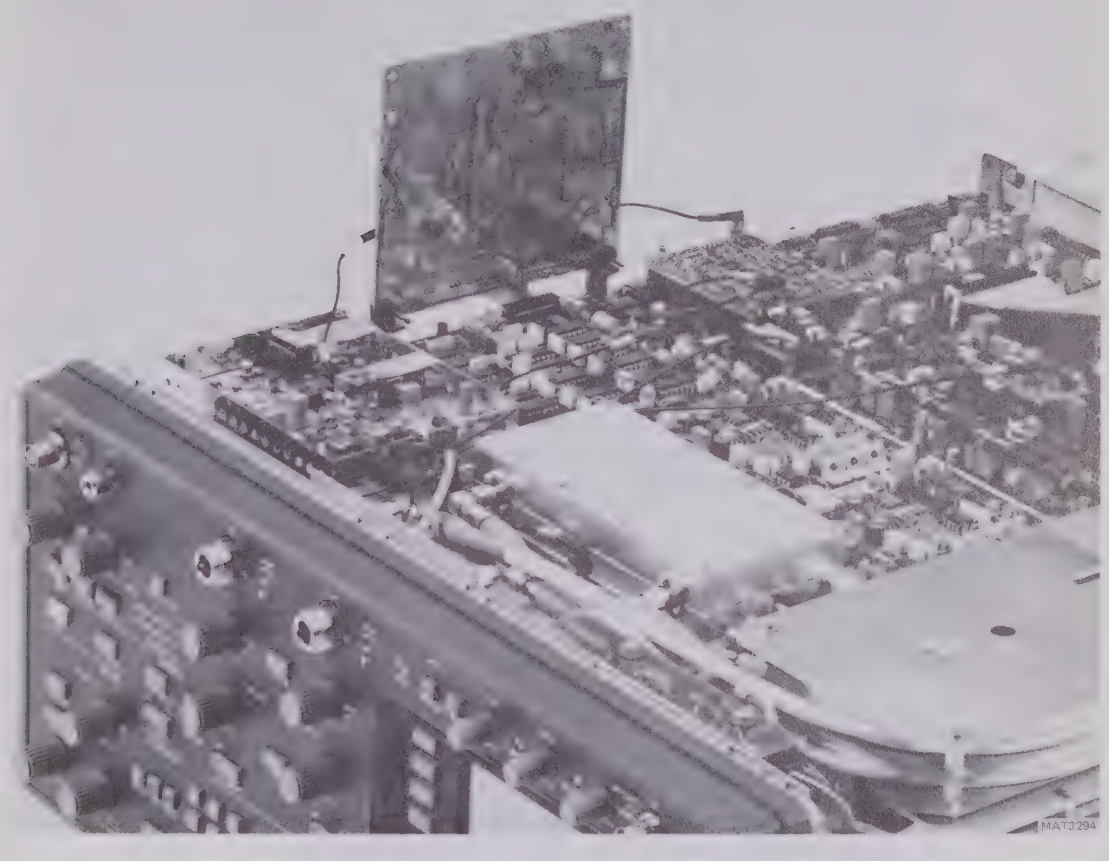

Figure 10.3 Access to trigger control unit.

The three stage triger unit can be turned up as follows:

- Disconnect all coax cables to this unit.
- Unscrew the four fixation screws.
- Turn the unit up and place it on the two supports as shown in figure 10.3.

In this position the oscilloscope can operate, but will not function properly. Nevertheless certain measurements can be done on the trigger control unit A34.

To reinstall the boards the steps have to be done in reverse order. Care should be taken of the reconnection of the coax cables at the right points. The cables should also be repositioned as much as possible to their original positions.

Notes: - If one of the coax cables should be replaced care should be taken that the length difference between this cable and cables with similar signals (e.g. balanced signals) is less than 1 cm, to avoid delay time differences.
- Section 15.3.2 supplies ordering information for longer coax cables.

10.6 REMOVING THE GATE UNIT, THE TRIGGER INPUT UNIT AND THE TRIGGER PICK-OFFS.

10.6.1 Removing the gate unit (unit A54)

The gate unit (inclusive the aluminium housing) can be removed as follows (see figure 10.4):

- Unplug all wiring from the vertical signal unit A55.
- Remove the two shielding plates from unit A55.
- Unplug the two rectangular SMA connectors at the gate housing, marked with A.
- Unscrew the fixation screws of A55 marked with B.
- Remove unit A55 completely from the instrument.
- Turn the unit upside down.
- Unscrew all fixation screws of the gate housing.

To reinstall the gate unit the steps have to be done in reverse order. When the gate unit is placed on the vertical signal unit, care should be taken not to clamp the resistors just beside the connectors of the gate unit (see also section 8.54.2). Care should also be taken of the reconnection of the coax cables at the right points. The cables should also be repositioned as much as possible to their original positions.

WARNING: The gate p.c.b. can be bended easily, which causes broken soldering joints.
Please handle carefully!

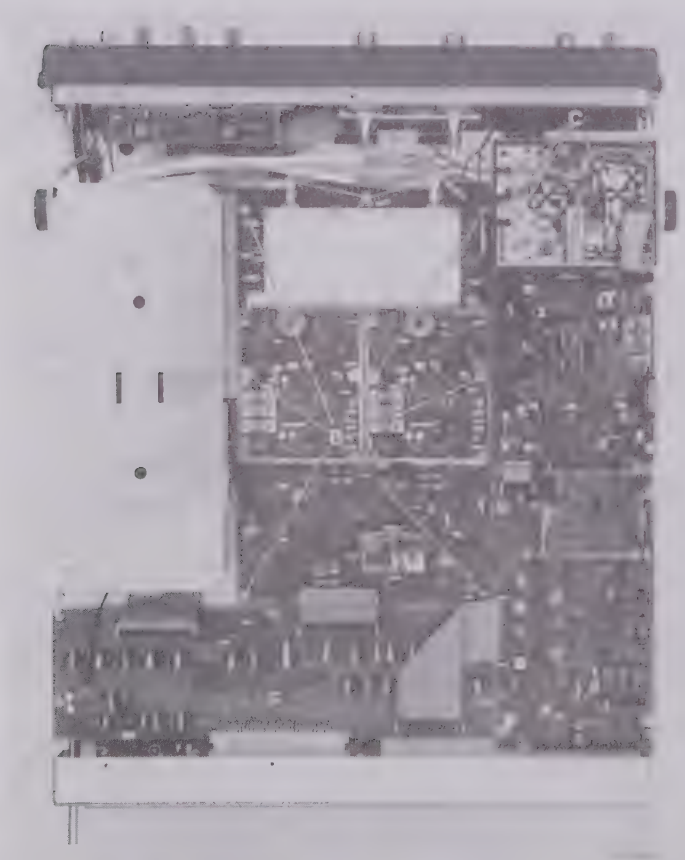

Figure 10.4 Bottom side of the oscilloscope.

10.6.2 Removing the trigger input unit (A31)

The trigger input unit can be removed as follows (see figure 10.4):

- Remove the shielding plate (5 screws)
- Unplug all wiring from the unit.
- Unscrew the distance pieces on the p.c.b.
- Unscrew all fixation screws of which some are marked with C.
- Remove the unit.

WARNING: The p.c.b. can be bended easily, which causes broken soldering joints.
Please handle carefully!

10.6.3 Removing the a trigger pick-off

A trigger pick-off can be removed as follows:

- Remove the complete front unit (see section 10.7.1).
- Unscrew the two fixation screws of the bracket over the trigger pick-offs.
- Disconnect the delay line from the trigger pick-off.
- Disconnect the coax cables of the trigger pick-off signal from the trigger input unit A31.
- Disconnect the trigger pick-off from the N-SMA input socket and remove it.

To reinstall the trigger pick-off the steps have to be done in reverse order.

Note: When the trigger pickoff is placed on the N-SMA input connector, it should be prevented that the central pin inside the input connector is shifted outside, e.g. by fitting the N-BNC adaption connector on the input connector.

10.7 REMOVING THE FRONT UNIT

10.7.1 Removing the complete front unit

- Remove the two screws A (figure 10.5) at the upper side of the front unit.
- Slacken the two screws B.
- Carefully press the front unit via the front side out of the instrument.
- Disconnect the two flatcable connectors from the front unit.
- Remove six screws to remove the cover from the front unit.

10.7.2 Removing the knobs of the rotary controls

- Remove the knob cover.
- Slacken the internal nut.
- Pull off the knob.

10.7.3 Removing the textplate

- Remove the complete front unit as described in section 10.7.1.
- Remove all the knobs of the rotary controls (see in section 10.7.2).
- Remove the four special screws which fix the textplate to the unit. This can be done with a special tool for slotted nuts as described under section 13.3.2.
- Remove the textplate.

NOTE: For a repair of a defective rotary control the textplate has not to be removed. Only the p.c.b. with the leds and the fototransistors has to be removed then.

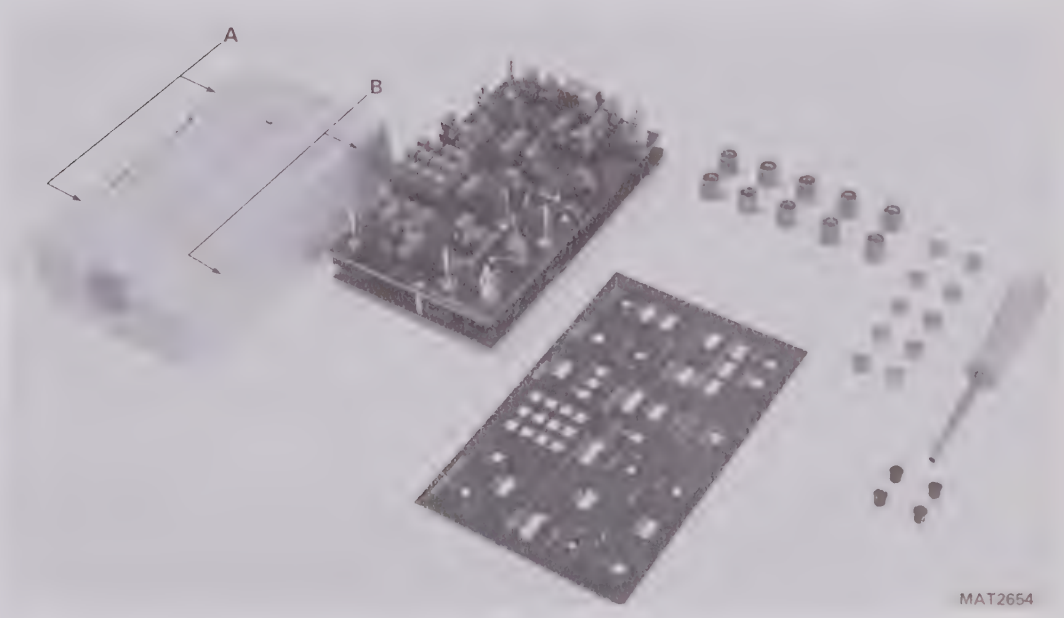

Figure 10.5 Disassembled front unit.

10.8 REMOVING THE C.R.T. CONTROL UNIT (A16 + A18)

- Remove the three C.R.T. control knobs as follows:
  - Remove the knob covers.
  - Slacken the internal screws.
  - Pull the knobs off.
- Remove the electrical wiring.
- Unscrew the two fixation screws on the front profile and pull the unit backwards.

NOTE: When reinstalling the unit take care off the correct position of the marks on the caps of the knobs.

10.9 REMOVING THE SOFTKEY UNIT (A17)

- Remove the front unit as described in section 10.7 until the unit is from the instrument and remove the bezel and the contrast filter.
- Remove the caps from the softkeys (8x).
- Unscrew the two fixation screws of the unit and unscrew the fixation screws of the brackets inside the front panel hole.
- Remove the brackets.
- Disconnect the flatcable from the unit and remove it.
- Remove the unit towards you.

10.10 REMOVING AND INSTALLING THE CATHODE RAY TUBE

- Disconnect flatcable connector X3001 (trace rotation coil) on the C.R.T. control unit A16.
- Remove the rear panel as described in section 10.4.
- Remove the bezel and the blue contrast filter.
- Remove the management unit A25.
- Remove the Z-amplifier unit A15.
- Remove the C.R.T. illumination set (1 screw).
- Slacken the tighten bolt of the C.R.T. pressing plate. This can be done through the hole in the partition on which unit A19 is mounted.
- Remove the pressing plate.

Now the C.R.T. is only fixed by a fork piece at the front end of the C.R.T., which on its turn is pressed by a wedge. The two screws that fix the fork and the wedge can be found in the right top corner above the front side of the C.R.T. The screw that is most right up fixes the wedge; the screw that is left below it fixes the fork piece.

- Slacken the screw of the fork piece.
- Slacken the screw of the wedge.
- Pull the C.R.T. with the shielding cone carefully backwards.

Care should be taken that transistor V3003 on the C.R.T. control unit below the front end of the C.R.T. is not damaged.

- Unplug the E.H.T. plug and discharge the E.H.T. cable by shortening the plug to the chassis.
- Remove the C.R.T. together with the shielding cone.
- Remove the earthing wire and the small spring from the cone.
- Remove the shielding cone and the rubber cap.

To reinstal the C.R.T. all steps have to be done in reverse order.

10.11 REMOVING THE CARRYING HANDLE

- Remove the plastic profile cover, (Item 6 in figure 10.6) which is snapped on the carrying profile (5).
- Remove the four screws (8) which fix the carrying profile to the handle arms.
- Depress the locking pins (1) and turn the carrying handle as far as possible to the upper side of the oscilloscope.
- Keep the locking pin of the right handle arm depressed and pull the handle arm from its bearing.
- Remove the carrying profile from the left handle arm.
- Depress the locking pin of the left handle arm and turn the latter as far as possible to the lower side of the oscilloscope.
- Keep the locking pin depressed and pull the handle arm from its bearing.

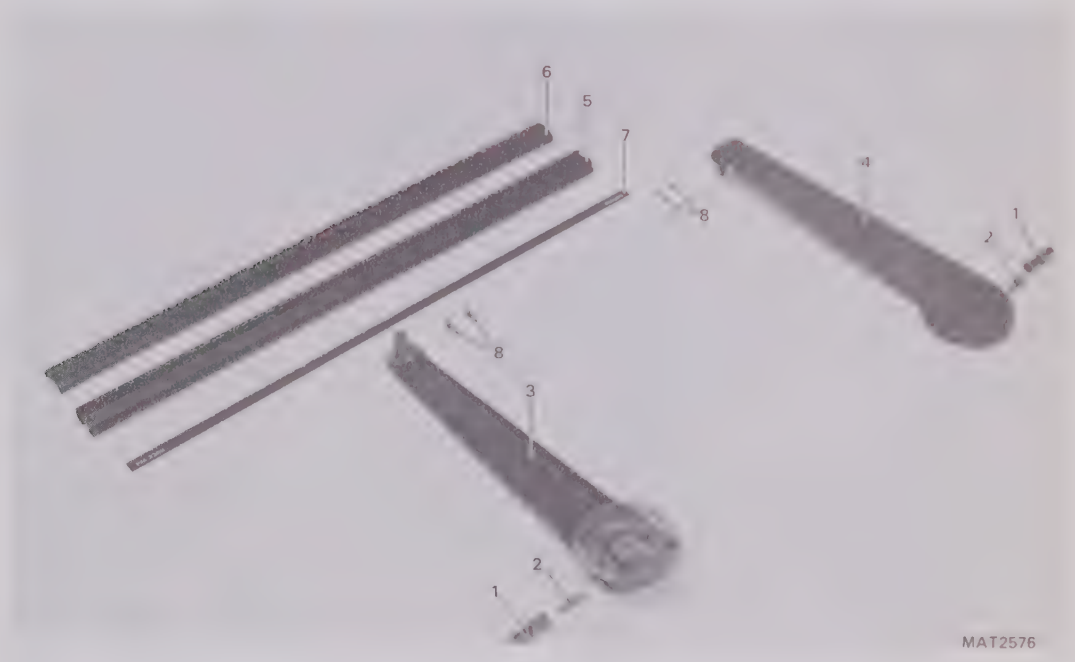

Figure 10.6 Carrying handle.

TROUBLE SHOOTING AND SERVICE DIAGNOSTICS 11

TROUBLE SHOOTING

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11.3 Trouble shooting hints..... 11-2
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11.0 TROUBLE SHOOTING

11.1 INTRODUCTION

The following information is provided to facilitate trouble shooting. Information contained in other sections of the manual should also be used to locate the defect. An understanding of the circuit is helpfull in locating troubles, particularly where integrated circuits are used. Refer to circuit descriptions for this information.

11.2 TROUBLE SHOOTING TECHNIQUES

If a fault appears, the following test sequence can be used to find the defective part:

- Check if the settings of the controls of the oscilloscope are correct. Consult the Operating Instructions.

- Check the equipment to which the oscilloscope is connected and the interconnection cables.

- Check if the oscilloscope is well-calibrated. If not, refer to chapter 9 "ADJUSTING PROCEDURE".

- Visually check the part of the oscilloscope in which the fault is expected. In this way, it is possible to find faults such as bad soldering connections, bad interconnection plugs and wires, damaged components or transistors and IC´s that are not correctly plugged into their sockets.

- Check the circuit part in which the fault is expected: the symptom often indicates this part of the circuit. If the power supply is defective the symptom will appear in several circuit parts.

After having carried out the previous steps, individual components in the suspected circuit parts must be examined:

- Transistors and diodes. Check the voltage between base and emitter (0,7 V approx. in conductive state) and the voltage between collector and emitter (0,2 V approx. in saturation) with a voltmeter or an oscilloscope. When removed from the p.c.b. it is possible to test the transistor with an ohmmeter since the base/emmiter and base/collector junctions can be regarded as diodes. Like a normal diode, the resistance is very high in one direction and low in the other direction. When measuring take care that the current from the ohmmeter does not damage the component under test.
  Replace the suspected component by a new one if you are sure that the circuit is not in such condition that the new component will be damaged.

- Integrated circuits. In circuit testing can be done with an oscilloscope or voltmeter. A good knowledge of the circuit part under test is essential. Therefore first read the circuit description in chapter 8 "CIRCUIT DESCRIPTIONS".

- Capacitors. Leakage can be traced with an ohmmeter adjusted to its highest resistance range. When testing take care of polarity and maximum allowed voltage. An open capacitor can be checked if the response for AC signals is observed. Also a capacitance meter can be used: compare the measured value with the value and tolerance indicated in the parts list.

- Resistors. Can be checked with an ohmmeter after having unsoldered one side of the resistor from the p.c.b. Compare the measured value with the value and tolerance indicated in the parts list.

- Coils and transformers. An ohmmeter can be used for tracing an open circuit. Shorted or partially shorted windings can be found by checking the waveform response when HF signals are passed through the circuit. Also an inductance meter can be used.

- Data latches. To measure on inputs and outputs of data latches a measuring oscilloscope can be triggered by the clock signal which is connected to the clock input of the data latch.
  Check the input data lines one by one during the active edge of the clock signal.
  This measurement can only be done in this way when there is an acceptable repetition time of the clock signal. A too low clock pulse repetition time results in a too low intensity of the trace on the measuring oscilloscope screen.
  The outputs can easily be checked by a voltmeter or oscilloscope.

11.3 TROUBLE SHOOTING HINTS

- If the oscilloscope does not operate at all then check the mains fuse and all power supply voltages.

- Try to find the unit where the failure is by accurately checking every malfunction of the oscilloscope. The block diagram (figures 6.1 and 6.2) may be of great use.

- Finding errors in certain parts can be done by using the service diagnostic software (see section 11.4).

- If there is no signal or text visible on the C.R.T. screen then check:
  - Intensity controls
  - Power supply to C.R.T.
  - Z-control

- If there are only traces visible, something will be broken in the hardware that controls the displaying of text:
  - Text intensity control
  - Z-control
  - Units A3 + A4

- If text is visible but no traces, please check the trace intensity control.

- If the DPU operates properly, the signal ILØ2--LT gives regularly negative pulses.

- If the acquisition operates properly, HDOF at X3054 on unit A52 changes regularly. The falling edge of the signal is the start of the capture of one sample.

11.4 DESCRIPTION OF THE DIAGNOSTIC SOFTWARE

11.4.1 Introduction

The diagnostic software consists of three parts:

- the power up routine
- softkey selectable diagnostic software
- hardware selectable diagnostic software

It is recommended to read the concerning hardware description first (chapter 8), before using the diagnostic software.

Each part will be described in the following subsections.

11.4.2 The power up routine

The power up routine is initiated every time the oscilloscope is turned on or when the microprocessor is restarted by the watchdog circuit (unit A6). It performs the following actions:

- First all leds on the front panel are turned on during 3 seconds.
- The leds SYNCHRONIZE and COUNT DOWN are extinghuished.
  Now the part of the microprocessor RAM (unit A5) which does not contain data that should be retained, is tested. If the test fails, the leds stay off and the address where the failure is, is continuously read and written by the microprocessor. This makes tracing of the failure easier.
- The led SYNCHRONIZE is turned on, so only led COUNT DOWN is off. Now the TEXT MEMORY is tested. The TRACE MEMORY can not be tested, because these data should be retained.
  If the test fails, the led COUNT DOWN stays off and the address where the failure is, is continuously read and written by the microprocessor, as with the previous test.
- The led COUNT DOWN is also turned on, so all leds are on.
  Now the part of the microprocessor ram (unit A5) that contains settings, is tested by means of a checksum test.
  If a fault is found in a setting belonging to a stored trace, this setting is cleared.

If a fault is found in a programmed front setting, the concerning front setting and all front setting which are stored at higher addresses are cleared. Because all settings are stored in time order of entrance, an "arbitrary" part of the settings is cleared.
Next the actual front setting is checked. If it has a checksum fault an AUTO SET is initiated, else the oscilloscope is set according to the values found in the ram.
It is this last routine that initiates AUTO SET after power up, if no backup batteries are installed.

- Finally the battery voltage is tested, and if it is too low, a message appears on the CRT screen.
The battery check is only done in this stage of the power up routine; nowhere else during operation.
The oscilloscope is now ready for operation.

Resumed:
- If the power up routine hangs up with both leds SYNCHRONIZE and COUNT DOWN off, the microprocessor ram is defective.
- If it hangs up with only led COUNT DOWN off, the display ram is defective.
- If stored traces or programmed front settings are cleared or an AUTO SET is initiated, while the backup batteries are OK, the contents of the microprocessor ram is destroyed. This may be caused by the oscilloscope being turned off at the moment the microprocessor was writing in the ram, but if it happens every time the oscilloscope is turned on the ram itself is broken.

NOTE: If the power up routine hangs up, the watchdog circuit on unit A6 is triggered regurlarly by the microprocessor, to prevent a new initiation of the power up routine again.

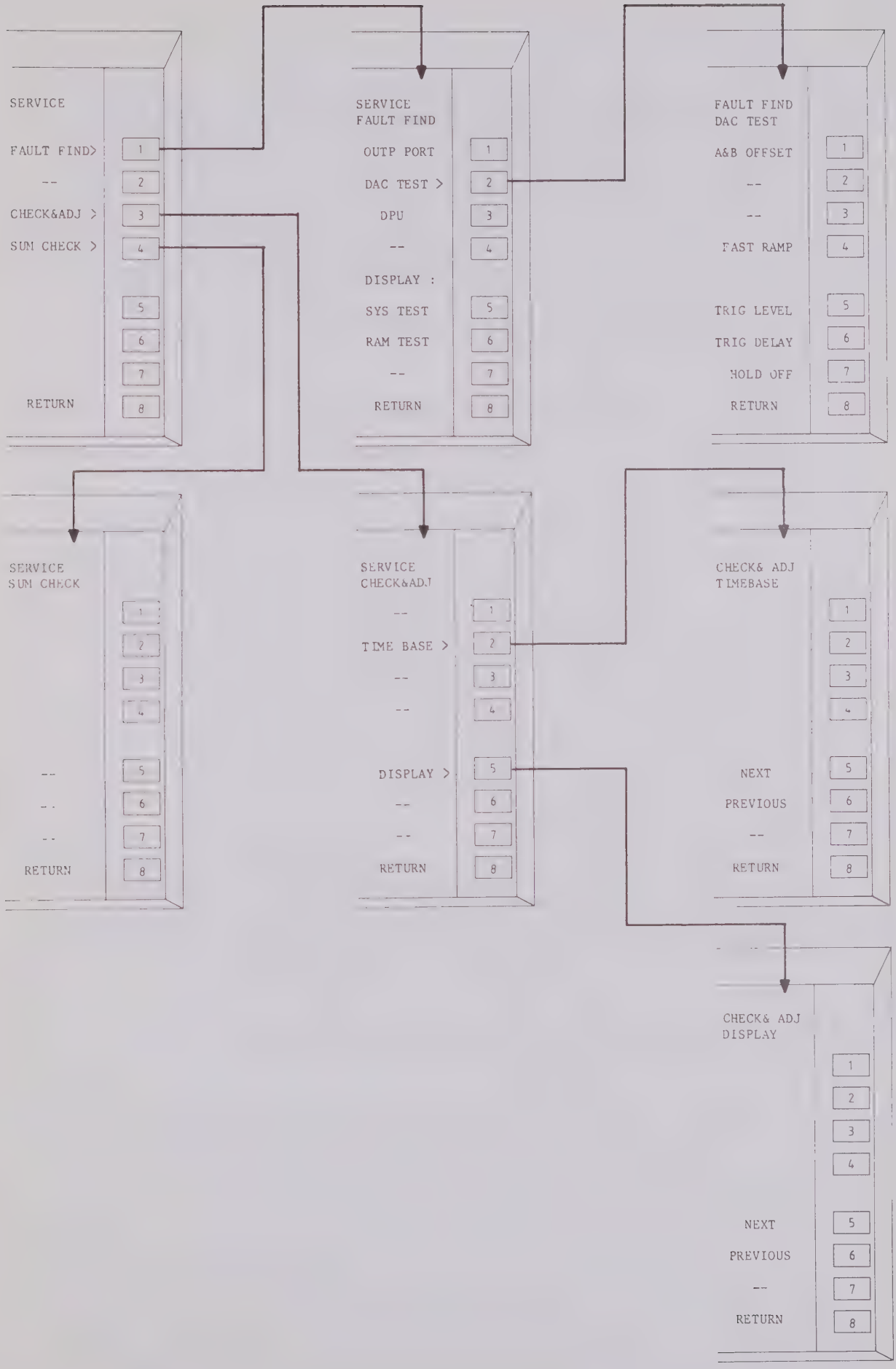


Figure 11.1 Service select menu structure.

11

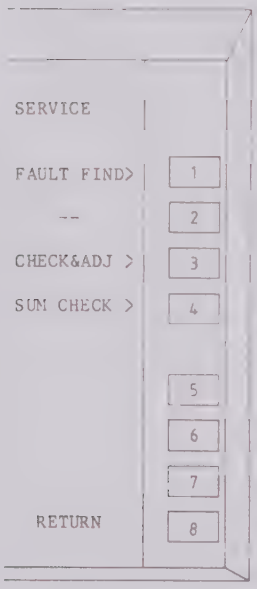
11.4.3 Softkey selectable diagnostic software

If some functions of the oscilloscope do not operate properly, the softkey selectable diagnostic software can be used to detect the defective hardware circuits.
This diagnostic software also contains a number of check and adjust routines (see chapter 9).

The routines destroy the actual front setting. Therefore returning to normal operation via the softkeys generates an AUTO SET.
It is always possible to return to normal operation by pressing the green pushbutton AUTO SET.
When a routine is operative and a setting is done on the front panel, the following message is given:

> Instrument in SERVICE mode.
> Changes are executed, but not always correct.

This is done because settings can not be executed if the concerning hardware is controlled by the selected diagnostic routine.



After pushing the upper and the lower softkey, the SERVICE menu appears on the screen. This menu allows selection of a range of fault find routines and a range of check & adjust routines (see figure 11.1)

Information about the software release is displayed at the left side of the softkeys 5 to 7.

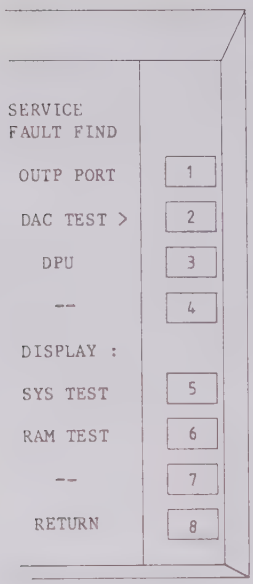
A message

For correct SERVICE handling:
*** switch off any active OPTION ***

may appear.

Options may be installed in the instrument, but they may not be active when the softkey selectable diagnostic software is used.
E.g. an interface should not display TIME and/or DATE.

1 FAULT FIND>



If FAULT FIND is selected the SERVICE FAULT FIND menu is displayed and a number of fault finding routines can be selected.

Each test can be stopped by pressing the same softkey again or by selecting another test.

In this part of the diagnostic software the traces are suppressed.

1 1 OUTP PORT

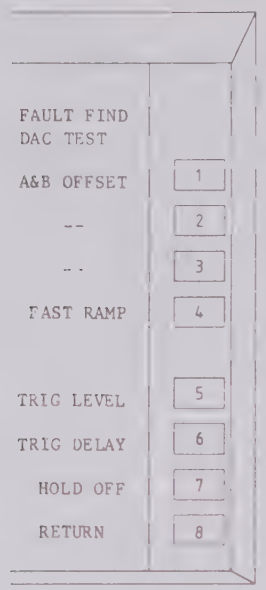
If OUTP PORT is selected an alternating pattern of zeroes and ones with a frequency of 1.6 Hz is generated at the following output ports:

Name	IC nrs	Unit
Variable feedback latches	D3124 + D3144	A25
Trigger latch	D2222	A34
Time-base latch	D3304	A51
Vertical latches	D5001 + D6001	A55
Variable latches	D5002 + D6002	A55

This test can be used to test the proper operation of these latches and their controlling hardware by checking all the outputs with an oscilloscope.

The output signals are at TTL level, except the signals from unit A55. These latches have output signals of 12 Volt.

1 2 DACTEST>



If DACTEST is selected, the FAULT FIND DAC TEST menu is displayed.
With this menu a number of DACs in the acquisition section of the oscilloscope can be tested, by checking their output voltage with another oscilloscope.

Because the softkeys are only checked after a cycle of a test and the cycle can take some time (up to a few seconds), it may be necessary to keep a softkey pressed down a while to get the desired action.

1 2 1 A&B OFFSET

If A&B OFFSET is selected, a sawtooth signal is generated at the outputs of the OFFSET DACs of channels A and B (N3136, N3137, N3138 and N3139 on unit A25). During the slope of the sawtooth the digital values at the inputs of these 14 bit DACs is incremented by 16 every time. So the 4 less significant bits are not tested.
The period is 0.4 s.
The output voltages are measured on the vertical signal unit A55.

Measuring points and voltages:

Name	ICs	Voltage range
OSCRA	N5007 pin 7	0-10 V
OSFIA	N5007 pin 14	0-4 V
OSCRB	N6007 pin 7	0-10 V
OSFIB	N6007 pin 14	0-4 V

1 2 2 --

1 2 3 --

1 2 4 FAST RAMP

If FAST RAMP is selected, a sawtooth signal is generated at the output of the FAST RAMP DAC (N3313 on unit A51).
During the slope of the sawtooth the digital value at the input of this 14 bit DAC is incremented by 16 every time. So the 4 less significant bits are not tested.
The output voltage amplitude is 9 V.
The period is 0.7 s.

Measuring point:

Time-base unit A51, N3314 pin 6.

1 2 5 TRIG LEVEL

If TRIG LEVEL is selected, a sawtooth signal is generated at the output of the TRIGGER LEVEL DAC (N3141 on unit A25).
During the slope of the sawtooth the digital value at the input of this 14 bit DAC is incremented by 16 every time. So the 4 less significant bits are not tested.
The output voltage amplitide is 3.9 V.
The period is 0.7 s.

Measuring point:

Trigger control unit A34, node R2229-Emitter V2206.

1 2 6 TRIG DELAY

If TRIG DELAY is selected, a sawtooth signal is generated at the output of the TRIGGER DELAY DAC (N3306 on unit A51).
During the slope of the sawtooth the digital value at the input of this 14 bit DAC is incremented by 16 every time. So the 4 less significant bits are not tested.
The output voltage amplitude is 8 V.
The period is 0.7 s.

Measuring point:

Time-base unit A51, N3307 pin 6.

1 2 7 HOLD OFF

If HOLD OFF is selected, a sawtooth signal is generated at the output of the HOLD OFF DAC (N3309 on unit A51).
During the slope of the sawtooth the digital value at the input of this 14 bit DAC is incremented by 16 every time. So the 4 less significant bits are not tested.
The output voltage amplitude is 19 V.
The period is 0.7 s.

Measuring point:

Time-base unit A51, N3311 pin 6.

1 2 8 RETURN

Return to SERVICE FAULT FIND menu.

1 3 DPU

If DPU is selected, the control memory of the DPU CONTROL unit A8 is loaded with a program that is run afterwards. This brings the DPU in a steady cycle, which enables testing of the system.
On a number of output signals of the DPU CONTROL a pulse is generated (see table below). These are all the output signals to the DPU (unit A9) and the trigger address comparator on unit A4, except TRRY and RSDU--LT.
The signals can be found on connector X1402.
The pulse width is 125 ns; the repetition time is 4,5 us.
All signals are at TTL level.

Signal name	Pinnr.	Signal name	Pinnr.
DUABØØ	C20	RDDURM	C26
DUABØ1	C21	SFSRØØ	C12
DUABØ2	A21	SFSRØ1	C11
DUABØ3	C22	STRLF	C15
DUABØ4	A22	ENOFD	A18
DUABØ5	C23	CKF	C25
DUABØ6	A23	CO	C13
DUABØ7	C24	SLAM	A28
DUABØ8	C16	RSDUR-LT	C19
DUABØ9	A17	OTDIAD	C29
DUAB1Ø	C18	OEDUØØ	A29
DUAB11	C17	OEDUØ1	A31
CSDURM	A27	LEDP	C31
CKDUR1	C3	SLOFAD	C27
CKDUR2-LT	A25	CNCPCN	A15
CKDUR3	A26	FBRY	C32

The state of the signals at the testpoints of unit A8 is:

Signal name	State
TRRY	Ø
EC	Ø
DAVA	Ø
ILØ2--LT	1
CKPL	Symmetrical square wave, cycle time = 125 ns.

1 4 --

1 5 DISPLAY SYS TEST

If DISPLAY SYS TEST is selected, the display system continuously displays the softkey text area, which can be seen as an intensified display. Traces, other text areas and miscellaneous text are not displayed. So the display system (units A1, A2, A3 and A4) is brought in a steady cycle, which enables testing of the system. See section 8.1 to 8.4 for the concerning hardware.

NOTE: if there is a failure in the display system, which causes the softkey text area not to be displayed, this test can not be selected in a visisble way. Nevertheless pushing the softkeys in the right sequence selects this test.

1 6 DISPLAY RAM TEST

If DISPLAY RAM TEST is selected, the display ram on unit A4 is tested. This ram consists of the text memory (D2014 and D2016) and the trace memory (D2008, D2009, D2011 and D2012). In the text memory the softkey text and the miscellaneous text is not tested.
If the test is completed succesfully, a message:

DISPLAY RAM test completed succesfully.

is displayed.
If the test fails, all leds on the front panel start blinking and the address where the failure is, is continuously read and written by the microprocessor.

NOTES: - this test destroys the contents of the trace memory, so after the test all traces are lost.
- as with the DISPLAY SYS TEST (see above), this test can be selected by pushing the softkeys in the right sequence, in case of a display failure.

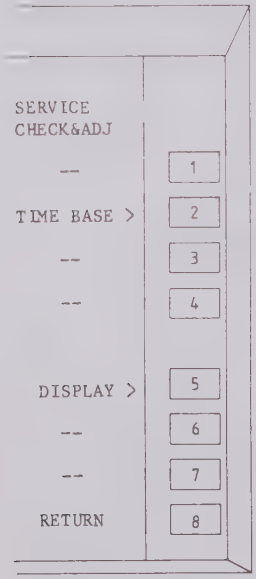
1 7 --

1 8 RETURN

Returns to SERVICE SELECT menu.

2 --

3 CHECK & ADJ>



If CHECK & ADJ is selected, the CHECK & ADJ menu is displayed and a number of adjust routines can be selected.

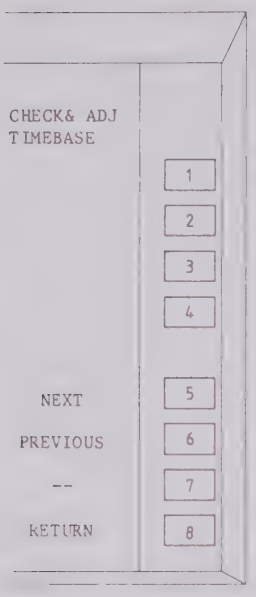
Each routine is only operative if it is displayed.

See chapter 9 for detailed information about the use of the adjust routines.

11

3 1 --

3 2 TIME BASE>



If TIME BASE is selected, the CHECK & ADJ TIMEBASE menu is displayed.
Information about the activated adjust routine for the vertical section of the oscilloscope is given at the left side of the softkeys 1 to 4.
The sequence number of the routine is displayed in the top of the menu behind "TIMEBASE".

3 2 5 NEXT

Activates and displays the time-base adjust routine with the next higher sequence number.

3 2 6 PREVIOUS

Activates and displays the time-base adjust routine with the next lower sequence number.

3 2 7 --

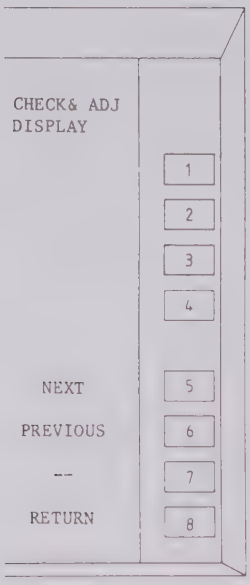
3 2 8 RETURN

Return to SERVICE CHECK & ADJ menu.

3 3 --

3 4 --

3 5 DISPLAY>



If DISPLAY is selected, the CHECK & ADJ DISPLAY menu is displayed.
Information about the activated adjust routine for the display section of the oscilloscope is given at the left side of the softkeys 1 to 4.
The sequence number of the routine is displayed in the top of the menu behind "DISPLAY".

3 5 5 NEXT

Activates and displays the display adjust routine with the next higher sequence number.

3 5 6 PREVIOUS

Activates and displays the display adjust routine with the next lower sequence number.

3 5 7 --

3 5 8 RETURN

Return to SERVICE CHECK & ADJ menu.

3 6 --

3 7 --

3 8 RETURN

Return to SERVICE CHECK & ADJ menu.

4 SUM CHECK>

If SUM CHECK is selected, the SUM CHECK menu is displayed.

At the left side of the softkeys 1 to 4 the sum check data are displayed.

4 5 --

4 6 --

4 7 --

4 8 RETURN

Return to SERVICE menu.

5 --

6 --

7 --

8 RETURN

Return to normal operation.
When a routine is still operative the following message is given:
Changes are executed, but not always correct.
This is done because settings can not be executed if the concerning hardware is controlled by the selected diagnostic.
Therefore this way of returning to normal operation is not recommended.

11.4.4 Hardware selectable diagnostic software

By changing over the service switches on unit A6, a number of service routines can be selected, which are suitable to test the hardware. For some routines not all hardware is needed. So these tests can be used by starting with the minimum required hardware and as long as the routines operate correctly more hardware can be connected until the routines do not operate anymore. The last connected hardware will be broken then.

The table below gives an overview of the tests.

Test	Service switches X1716	X1704	X1706	X1707	Minimum required hardware
Normal operation	fitted	down	down	down	all cards
RAM test	removed	down	up	down	A5 + A6
Front + output ports	removed	up	down	down	A5 + A6 + A8 + frontpanel
Address range	removed	up	up	up	A6

NOTES:
- Figure 11.2 shows the service switches in normal operation position.
- If X1716 is not fitted in normal operation, the oscilloscope may operate normally, but it is possible that it does not start up under certain conditions, because the watchdog circuit is disabled.
- Any options (A7 or A10) should be removed.

The RAM TEST enables testing of the microprocessor ram on unit A5. The test is a cyclic sequence that consists of the following parts:

- All leds on the frontpanel are turned on during 3 seconds.
- All leds are turned off, except the led TRIGGER.
- The microprocessor ram is written with a certain pattern in a certain sequence.
- The led SYNCHRONIZE is turned on.
- The contents of the microprocessor ram is read back and checked. If the contents is OK, all leds are turned on during 3 seconds, etc. If the contents is wrong, the 3 leds TRIGGER, SYNCHRONIZE and COUNT DOWN start blinking with a frequency of about 2 Hz and the address where the failure is, is continuously read and written by the microprocessor.

The FRONTPANEL AND OUTPUT PORTS TEST enables the testing of the frontpanel and the output ports, which can not be tested by the softkey selectable output port test (see section 11.4.3).
When the test is started all leds on the frontpanel start blinking with a frequency of about 2 Hz.
After pushing a pushbutton, the softkeys included, or turning a rotary switch all leds are turned off.
Now the three leds TRIGGER, SYNCHRONIZE and COUNT DOWN form the display of a three byte binary counter. The counter counts the opening or closing of every pushbutton switch on the frontpanel as well as the level changes of the outputs of the rotary switches as they are turned. The counter counts always up, independent of the turning direction of the rotary switches.

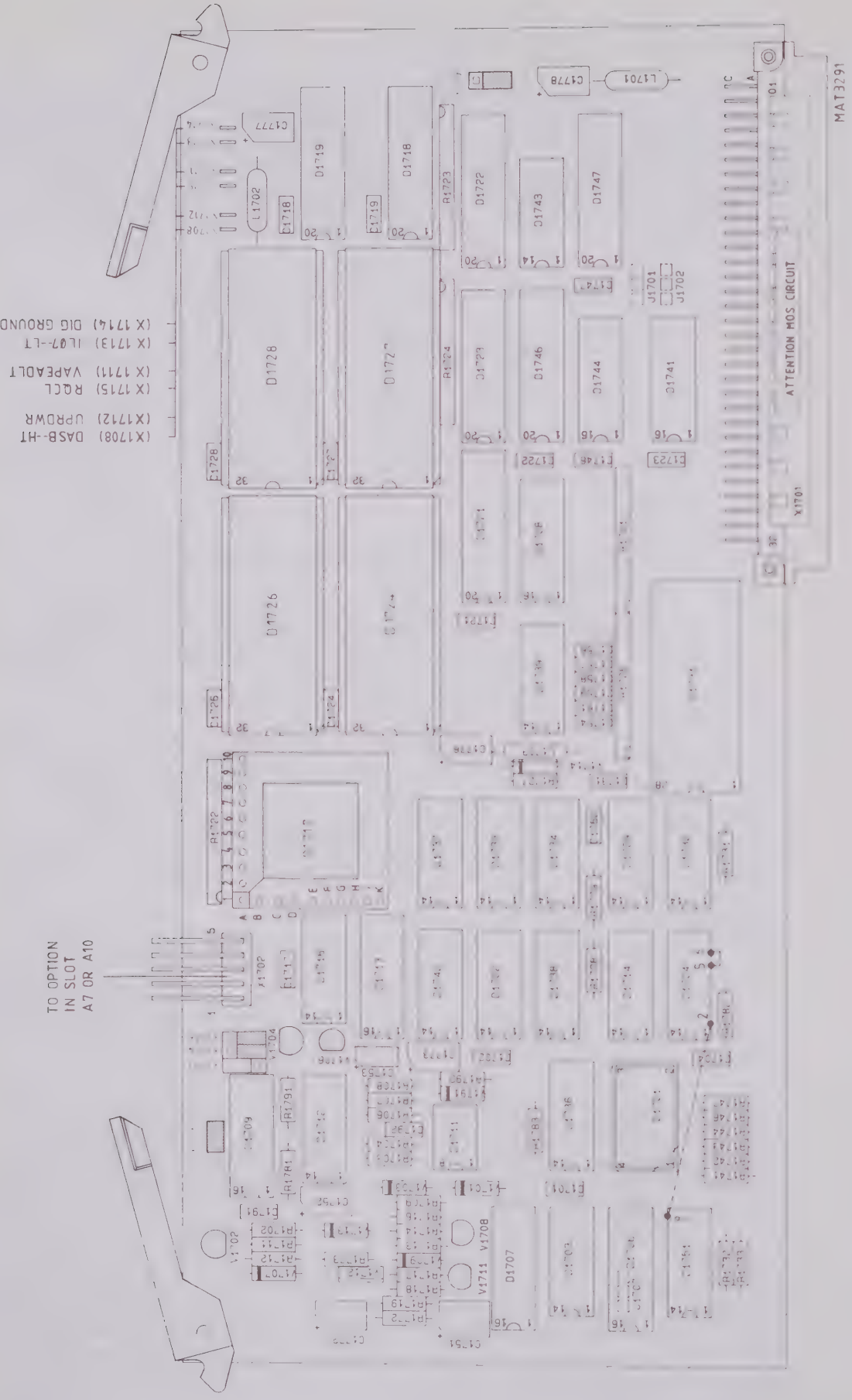


Figure 11.2 Location of service switches.

While the front test is started by pushing a button or turning a rotary switch, the output port test is also started. This test writes an alternating pattern to hardware that is selected by signals with the following names:

Unit	Signal name	IC numbers
A2	WRVEPOLT	D2314 + D2316
A2	WRHOPOLT	D2317 + D2318 + D2332
A3	WRDPSTLT	D2119
A3	WRPSDPLT	D2103 + D2104
A3	WRDPPALT	D2106 + D2107
A3	WRHOVRLT	D2108
A5	LEACL	D1814
A8	SLOT2	D1419
A8	SLOT4	D1421 + D1422

At the outputs of mentioned latches a symmetrical square wave appears with a repetition time of 270 us, except D1814 which gives signals with a repetition time of 1 ms.
Furtheron the alternating pattern is written to the following hardware:

Unit	Signal name	IC numbers
A3	Z + Interrupt timer	D2126
A8	Control memory	D1426 + D1427 + D1428 + D1429

NOTE:
- This test can be done without unit A8 fitted, if a diode link is made between MYSLØ3LT (pin B6) and DATRAKLT (pin C8) on connector X1701. The anode of the diode should be connected to pin C8.

The ADDRESS RANGE TEST writes and reads in sequence the hexadecimal code 5555 to all addresses, followed by the same sequence with hexadecimal code AAAA.
The complete test takes about 74 seconds and is repeated automatically. Each address is read immediately after it is written. The read data are not checked.
During this test all levels of the lines of the microprocessor busses should change regularly.

NOTES:
- Data and address bus lines to other units via the motherboard (unit A12) only change if the address range outside unit A6 is addressed.
- This test can also be run with unit A6 removed from the oscilloscope and supplied by an external 5 Volt power supply.

11.5 RECALIBRATION AFTER REPAIR

After an electrical component has been renewed the calibration of that particular circuit should be checked, as well as the calibration of other closely-related circuits.

Since the power supply affects all circuits, calibration of the entire instrument should be checked if work has been done in the power supply or if the transformer has been renewed.

HANDLING OF COMPONENTS AND SOLDERING TECHNIQUES 12

HANDLING OF COMPONENTS AND SOLDERING TECHNIQUES

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12.0 HANDLING OF COMPONENTS AND SOLDERING TECHNIQUES

12.1 HANDLING OF COMPONENTS

12.1.1 Standard parts

Electrical and mechanical parts replacements can be obtained through your local PHILIPS organisation or representative. However, many of the standard electronic components can be obtained from other local suppliers. Before purchasing or ordering replacement parts, check chapter 15 "PARTS LISTS" for value, tolerance, rating and description.

NOTE: Physical size and shape of a component may affect instruments performance, particularly at high frequencies.
Always use direct replacement components, unless it is known that a substitute will not degrade the instruments performance.

12.1.2 Special parts

In addition to the standard electronic components, some special components are used:

- Components, manufactured or selected by PHILIPS to meet specific performance requirements.
- Components which are important for the safety of the instrument.

ATTENTION: Both type of components may only be replaced by components obtained through your local PHILIPS organisation or representative.

12.1.3 Transistors and integrated circuits

- Return transistors and I.C.'s to their original positions, if removed during routine maintenance.

- Do not renew or switch semi-conductor devices unnecessary, as it may affect the calibration of the instrument.

- Any replacement component should be of the original type or a direct replacement. Bend the leads to fit in the socket or pcb-holes and cut the leads to the same length as on the component being renewed.

- When a device has been renewed, check the operation of the part of the instrument, that may be affected.

- When re-installing power-supply transistors, use silicon grease to increase the heat-transfer capabilities.

WARNING: Handle silicon grease with care. Avoid contact with the eyes. Wash hands thoroughly after use.

12.1.4 Static sensitive components

This instrument contains electrical components that are susceptible to damage from static discharge. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

12.2 HANDLING OF MOS DEVICES

Though all our MOS integrated circuit incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

CAUTION: Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

12.2.1 Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or a special IC carrier that either short-circuits all leads or insulates them from external contact.

12.2.2 Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord to a chain. Connect all testing and handling equipment to the same surface. Signals should not be applied to the input while the device power supply is off. All unused input leads should be connected either to the supply voltage or to ground.

12.2.3 Mounting

Mount MOS integrated circuits on printed circuit boards after all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board, the person mounting the circuit should touch the board before bringing the MOS circuits into contact with it.

12.2.4 Soldering

Soldering iron tips, including those of low voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

12.2.5 Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted, the proper handling precautions should still be observed.
Until the sub-assemblies are inserted into the complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape is put on the circuit board terminals.

12.2.6 Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed circuit boards with MOS devices, from test sockets or systems with power on.

12.2.7 Voltage surges

Beware of voltage surges due to switching electrical equipment ON or OFF, relays and d.c. lines.

12.3 SOLDERING TECHNIQUES

Working method:

- Carefully unsolder one after the other the soldering tags of the semi-conductor.
- Remove all superfluous soldering material. Use a sucking iron or sucking litze wire.
- Check that the tags of the replacement part are clean and pre-tinned on the soldering places.
- Locate the replacement semi-conductor exactly on its place, and solder each tag to the relevant printed conductor on the circuit board.

NOTE: Bear in mind that the maximum permissible soldering time is 10 seconds during which the temperature of the tags must not exceed 250°C. The use of solder with a low melting point is therefore recommended.
Take care not to damage the plastic encapsulation of the semi-conductor (softening point of the plastic is 150°C).

ATTENTION: When you are soldering inside the instrument it is essential to use a low-voltage soldering iron, the tip of which must be earthed to the mass of the oscilloscope.

Suitable soldering irons are:

- ORYX micro-miniature soldering instrument, type 6 A, voltage 6 V, in combination with PLATO pin-point tip type 0-569.
- ERSA miniature soldering iron, type minor 040 B, voltage 6 V.
- Low voltage mini soldering iron, type 800/12 W-6 V, power 12 W, voltage 6 V, order no. 4822 395 10004, in combination with 1 mm pin-point tip, order no. 4822 395 10012.

Ordinary 60/40 solder with core and 35- to 40 W pencil type soldering iron can be used to accomplish the majority of the soldering. If a higher wattage-rating soldering iron is used on the etched circuit boards, excessive heat can cause the etched circuit wiring to separate from the board base material.

12.3.1. Soldering and desoldering of surface mounted devices

Introduction

This description gives you a method for replacing surface mounted devices (S.M.D.'s) and incorporates subjects such as:

- required tools and materials.
- how to arrange the S.M.D.-workshop. (see figure 12.1).
- general hints for S.M.D.-handling.
- interchanging S.M.D.'s with two or three connections.
- interchanging S.M.D.'s with four or more connections.

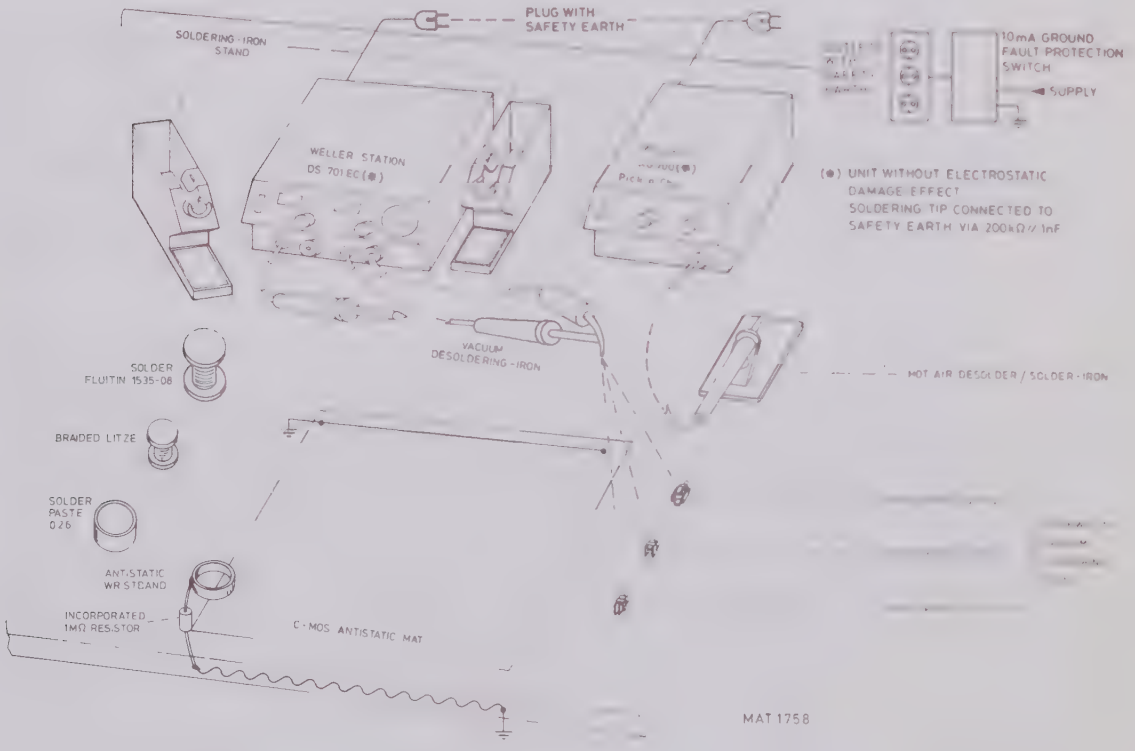

Figure 12.1 Arrangement of working area for S.M.D. exchange.

Required tools and materials

The following tools are necessary:

- A hot-air soldering/desoldering station for components with two or three leads: Weller AG 700 pick-a-chip.
- A vacuum, temperature controlled, soldering/desoldering station for components with four or more connections: Weller DS 701 EC.

- Desoldering accessories that can be attached to the Weller DS 701 EC-equipment: for dual-in-line S.M.D.´s VSO 14 and VSO 16 (with 14 and 16 connections such as used on the HF-attenuator p.c.b.) the types with Weller ordering code 587 13 701 and 587 13 702. For dual-in-line S.M.D.´s VSO 40 (with 40 connections such as used on the LCD-unit) the type with Weller ordering code 587 13 703. For QFP 24 S.M.D.´s (such as used on the time base chip unit) the type with Weller ordering code 587 13 704.
- A working area that has been secured against electro static discharge (E.S.D.).
- A pair of tweezers.

NOTE: The Weller equipment can be ordered via your local Weller-dealer.

The following material is necessary:

- "Fluittin" solder diameter of 0,8 mm, 15/35, Sn Pb 60.
- Solder paste 026.
- Components. Since not all the components are marked, they must be kept in their original packing in order to avoid interchanging them.
- Desoldering braided wire.

General hints for S.M.D.-mounting.

- Protection against E.S.D.: since the working area must be suitable for repair of MOS-devices, some precautions must be taken (see figure 12.1)
  All repairs must be done earthened which means that the repair surface, the soldering iron and the technician must be connected to the earth potential. This is achieved by using a C-MOS antistatic mat that must be connected to earth. The service-technician is connected to earth by wearing an antistatic wristband.
- Components: desoldered components cannot be used again since desoldering is done at a temperature of 350 degrees Celcius while they can only whitstand 240 degrees Celcius for max. 10 sec.
  Keep the new components as long as possible in their original packing in order to avoid damage and mixing up new and old S.M.D.´s.
- For an optimal supply of heat a working area must be used that does not lead away the heat: the antistatic mat in figure 12.1 meets this requirement.

Interchanging S.M.D.´s with two or three connections.

IMPORTANT: Before removing the component, observe very carefully its position in order to aviod that the new component is installed upside-down. This is especially important for capacitors where the metallisation at both ends is longer at the p.c.b. side than at the top side.

Use the equipment Weller AG 700 pick-a-chip and proceed as follows:

- Heat the component up equably with hot air of 350 degrees Celcius.
- Remove the component with a pair of tweezers.
- Clean the p.c.b. tracks, on which the new component has to be soldered, with braided wire or with the use of the vacuum desoldering equipment DS 701 EC.
- Put solder paste on the connections of the new component and position it on the p.c.b..
- Solder the component on to the p.c.b. with the solder described in the materials list. Soldering temperature must be 240 degrees Celsius, soldering time must not exceed 3 sec. per connection. The tip of your soldering iron must not touch the component, but must touch the p.c.b. track close to the component.

Interchanging S.M.D.´s with four or more connections.

Use the equipment Weller DS 701 EC and attach a suitable desoldering piece (VSO 14, VSO 16, VSO 40 or OFP 24). Then proceed as follows:

- Adjust the desoldering temperature to 350 degrees Celcius and place the desoldering piece on the IC that has to be removed. Take care that all connections of the IC are equally heated up).
- Switch the vacuum on and lift the component from the p.c.b.
- Clean the p.c.b. tracks, on which the new component has to be soldered, with braided wire or with the use of the vacuum desoldering equipment DS 701 EC.
- Put solder paste on the connections of the new component and position it on the p.c.b.
- Position the component by soldering first the outside connections in a crosswise manner. Soldering temperature must be 240 degrees Celcius. Keep the soldering time as short as possible.
- Solder now the other connections.
- If necessary you must remove superfluous rests of solder with the use of braided wire.

SERVICE TOOLS 13

SERVICE TOOLS

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13.0 SERVICE TOOLS

13.1 RECOMMENDED TEST AND CALIBRATION EQUIPMENT

A complete list of all material necessary for the adjusting procedure and the performance check is given in section 9.2.

13.2 DUMMY LOAD FOR POWER SUPPLY (unit A20)

Information for an easy access to the power supply and for safe working conditions can be found in chapter 10 "DISASSEMBLING AND ASSEMBLING". This chapter also explains how to measure the power supplies in working condition.
The position of the rear side panel of the oscilloscope under test is also indicated in chapter 10.

In order to be able to determine whether a certain fault condition is initiated by the power supply itself or by the connected oscilloscope circuits, a dummy load is listed in the table below. The table gives also an example of the resistor types that can be used to compose the dummy load: the resistors can be ordered at Concern Service.

The dummy load resistors must be mounted on a p.c.b. and connected via a (flat)cable to X4604 on unit A20 (mounted on rear side panel).
The connector pins are also given in the diagram of chapter 8.20.
Electrolytic capacitors in the dummy load are not necessary because of the capacitive values present on the power supply unit itself.

Supply Voltage	Connector pin(s) X4604 (A20)	Output Current	Power dissi-pation	Dummy load
+5 V (+5 D)	30A-30C-31A-31C-32A-32C	5 A	25W	10 resistors of 10 Ohm, 4 W in parallel: 4822 112 21054
-5 V (-5 D)	13A-13C-14A-14C-15A-15C	2,2 A	11 W	4 resistors of 10 Ohm, 4 W: 4822 112 21054 and 1 resistor of 39 Ohm, 4 W: 4822 112 21069 in parallel
+7 V	16A-16C	550 mA	3,9 W	2 resistors of 27 Ohm, 4 W: 4822 112 21065 in parallel
-7 V	17A-17C	1,2A	8,4 W	2 resistors of 12 Ohm, 7 W: 4822 112 41056 in parallel
+14 V	20A-20C-21A-21C	1,2A	16,8 W	2 resistors of 27 Ohm, 11 W: 4822 112 31065 and 1 resistor of 100 Ohm 4 W: 4822 112 21081 in parallel
-14 V	18A-18C-19A-19C	1A	14 W	2 resistors of 8,2 Ohm, 4 W: 4822 112 21052 in parallel, with 1 resistor of 10 Ohm 11 W: 4822 112 31054 in series
+19 V	23A-23C	150 mA	2,9 W	1 resistor of 100 Ohm, 4 W: 4822 112 21081 in series with 27 Ohm , 4 W: 4822 112 21065
-19 V	22A-22C	250 mA	4,8 W	2 resistors of 150 Ohm, 4 W: 4822 112 21085 in parallel
+40 V	24A-24C	120 mA	4,8 W	1 resistor of 330 Ohm, 7 W: 4822 112 41094
+100 V	12 A	20 mA	2 W	1 resistor of 4,7 kOhm, 4 W: 4822 112 21125
6,3 V a.c filament C.R.T.	X4602 pins 3 and 1	250 mA	1,6 W	lamp 6,3 V 250 mA: 4822 134 40007

13.3 SPECIAL TOOLS

13.3.1 Special tool for removal of N and BNC input connectors

A special tool is available for removal of the nuts that secure the N and BNC input connectors (service ordering code 5322 395 54023). For those who want to make such a tool, a sketch is given with dimensions in mm in figure 13.1. The material is silversteel NO94, tempered 40-45 RC.

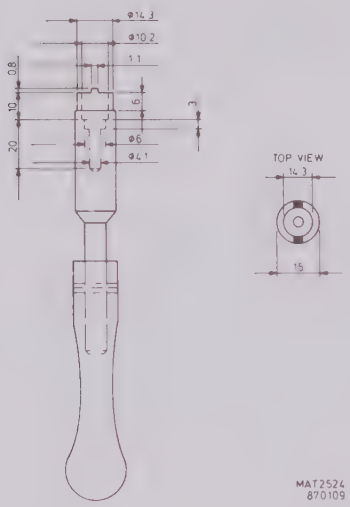

Figure 13.1 Dimensional drawing of tool for BNC input sockets.

13.3.2 Special tool for removing the small rotary knobs of the front panel.

A special tool is available for removing and fixing the small knobs, ordering number 5322 395 54024.
This can also be done with a normal screwdriver as described in chapter 10.
For those who want to make such a tool, a sketch is given below with the dimensions in mm.
The material is silversteel NO94, tempered 40-45RC.

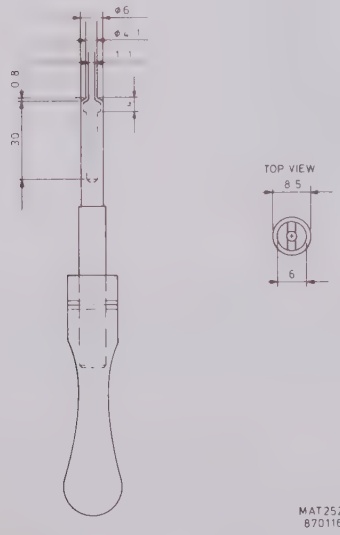

Figure 13.2 Dimensional drawing of tool for slotted nut.

13.3.3 Extension board for the units A1 ... A11 and A20

For test and repair purposes the unit A1 ... A11 or A20 can be plugged in their connectors via an extension board available under codenumber 5322 216 51153
The position of the rear side panel with unit A20 connected to the distribution unit A53 via the above mentioned extension card is indicated in chapter 10.

13.3.4 Special tool for removing integrated circuits (DIL package)

For cutting the connection pins of integrated circuits a special cutnipper is available under ordering number 5322 395 71004

13.4 TRIMMING KIT SBC 317 4822 310 50095

The SBC 317 Trimming Kit matches every current trimming requirement on all products. The set contains 27 pieces (22 different bits, plus 3 bit holders and 2 extension pieces). The insulated holders and extension pieces make it easy to reach into a chassis and make accurate adjustments, without wasting time or risking shocks.
The SBC 317 Trimming Kit is packed in a flat transparent case.
Several of the most commonly required bits are duplicated. In addition, a spare set of 8 bits is separately available as replacement (4822 310 50016).

Figure 13.3 Trimming tool kit.

SAFETY INSPECTION AND TESTS AFTER REPAIR AND MAINTENANCE 14

SAFETY INSPECTION AND TESTS AFTER REPAIR AND MAINTENANCE

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14.0 SAFETY INSPECTION AND TESTS AFTER REPAIR AND MAINTENANCE IN THE PRIMARY CIRCUIT

14.1 SAFETY INSPECTION AND TESTS

14.1.1 General directives

- Take care that the creepage distances and clearances have not been reduced.
- Before soldering, the wires should be bent through the holes of solder tags, or wrapped around the tag in the form of an open U, or, wiring ridigity shall be maintained by cable clamps or cable lacing.
- Replace all insulating guards and -plates.

14.1.2 Safety components

Components in the primary circuit may only be renewed by components selected by PHILIPS, see also clause 12.1.2.

14.1.3 Checking the protective earth connection

The correct connection and condition is checked by visual control and by measuring the resistance between the protective lead connection at the plug and the cabinet/frame. The resistance shall not be more than 0,1 Ohm. During measurement the mains cable should be removed from the mains. Resistance variations indicate a defect.

14.1.4 Checking the insulation resistance

Measure the insulation resistance at U = 500V dc between the mains connections and the protective lead connections. For this purpose set the mains switch to ON. The insulation resistance shall not be less than 2 MOhm.

NOTE: 2 MOhm is a minimum requirement at 40°C and 95% Relative Humidity. Under normal conditions the insulation resistance should be much higher (10 ... 20 MOhm).

14.1.5 Checking the leakage current

The leakage current shall be measured between each pole of the mains supply in turn, and all accessible conductive parts connected together (including the measuring earth terminal).
The leakage current is not excessive if the measured currents from the mentioned parts does not exceed 0,5 mA rms.

14.1.6 Voltage test

The instrument shall withstand, without electrical breakdown, the application of a test voltage between the supply circuit and accessible conductive parts that are likely to become energized. The test potential shall be 1500 V rms at supply-circuit frequency, applied for one second.
The test shall be conducted when the instrument is fully assembled, and with the primary switch in the ON position.
During the test, both sides of the primary circuit of the instrument are connected together and to one terminal of the voltage test equipment; the other voltage test equipment terminal is to be connected to the accessible conductive parts.

14.2 INSTRUMENT REPACKING

If the instrument is to be shipped to a Service Centre for service or repair, attach a tag showing the full addres and the name of the individual at the users firm that can be contacted. The Service Centre needs the complete instrument, its serial number and a fault description. If the original packing is not available, repack the instrument in such a way that no damage occurs during transport.

PARTS LIST

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15.0 PARTS LISTS

SUBJECT TO ALTERATION WITHOUT NOTICE

In this chapter the mechanical and electrical parts are listed.

The item numbers of the parts are indicated in the figures of this chapter.

The opening of parts, or removal of covers, is likely to expose live conductors. The instrument should therefore be disconnected from all voltage sources before any opening of parts or removal of covers is started.
During and after dismantling, bear in mind that capacitors in the instrument may still be charged even if the instrument has been separated from all voltage sources.

15.1 MECHANICAL PARTS

15.1.1 Mechanical + electrical parts front side (figure 15.1)

Item	Qty/. instr.	Description	Ordering number
1	1	Green pushbutton cover for: S4229 AUTO SET	5322 414 20186
2	11	Brown pushbutton cover (12,5 x 6,5) for: S4224 CURSOR S4221 VERTICAL MODE S4219 VERTICAL OFFSET S4217 SAVE/PLOT S4222 HORIZONTAL MAGN/DELAY S4216 MAGNIFY S4218 DISPLAY S4226 FRONT NO S4228 TRIGGER MODE S4223 TRIGGER SOURCE S4227 HORIZONTAL ACQ MODE	5322 414 60037
3	8	Brown pushbutton cover (12,5 x 6,5) for: S4 SOFTKEY 1 S5 SOFTKEY 2 S6 SOFTKEY 3 S7 SOFTKEY 4 S8 SOFTKEY 5 S9 SOFTKEY 6 S10 SOFTKEY 7 S11 SOFTKEY 8	5322 414 20185

Item	Qty/. instr.	Description	Ordering number
4	4	Brown pushbutton cover assembly (6,5 x 6,5) with led window for: S4233 WRITE S4234 LOCK S4231 AUTO SELECT S4237 NEG SLOPE S2 DOTS S3 AVERAGE C=4	5322 414 60038
5	2	Brown pushbutton cover and switch (6,5 x 6,5) for: S4236 CLEAR S4232 URQ	5322 276 11856
6	3	Brown UP/DOWN-control cover (18 x 6,5) and switch for: S4238 A AMP/DIV S4239 B AMP/DIV S4241 TIME/DIV	5322 277 10878
7	11	Brown knob dia 14 mm for rotary controls: CURSOR 1st CURSOR 2nd OFFSET A OFFSET B VARIABLE A VARIABLE B Y-POSITION X-POSITION X-EXPAND HOLD OFF/SYNC LEVEL	5322 414 30062
8	11	Brown cover for 14 mm knob for rotary controls:	5322 414 70015
9	1	Key unit (12 keys with numbered covers)	5322 218 41032
10	3	Brown knob dia 10 mm for: R1 ILLUM R3 INTENS TRACE R5 INTENS TEXT	5322 414 30044
11	3	Brown cover + line for: R1 - R3 and R5	5322 414 70016
12	2	Illumination lamp E1 and E2 (28 V - 80 mA)	5322 134 40534
13	1	Illumination lampholder	5322 255 24015
14	1	Illumination lamp unit including cable	5322 218 41033
15	1	POWER ON knob	5322 414 60142
16	1	Spring for POWER ON knob	5322 492 41354
17	1	POWER ON ledholder	5322 255 40231
18	1	POWER ON led CQW54-VI H1	5322 130 32704

19	7	Led CQY54-A-2 for: UNCAL A H4204 UNCAL B H4206 REMOTE H4207 TRIGGER H4201 SYNCHRONIZE H4202 COUNT DOWN H4203 UNCAL X-EXPAND H4208	4822 130 31128
20	1	X1 CAL BNC output socket	5322 267 10004
21	2	N input socket for: X2 A X3 B	5322 263 21009
22	4	X6 EXT TRIG BNC input socket	5322 267 10191
23	1	Knurled nut for earth connector X5	5322 505 14178
24	1	Thread end for earth connector X5	5322 535 84446
25	1	Front text plate (with adhesive backside)	5322 455 21357
26	1	Textplate under C.R.T. (with adhesive backside)	5322 455 21356
27	1	Textstrip above C.R.T. (with adhesive backside)	5322 455 21355
28	1	Blue contrast filter	5322 381 10963
29	1	Bezel (window for contrast filter)	5322 450 60977
30	2	Spring for bezel	5322 492 63719
31	1	Plastic front frame	5322 447 91377
-	1	Front cover (without inner plate)	5322 447 91378
-	1	Inner plate of front cover	5322 447 91376

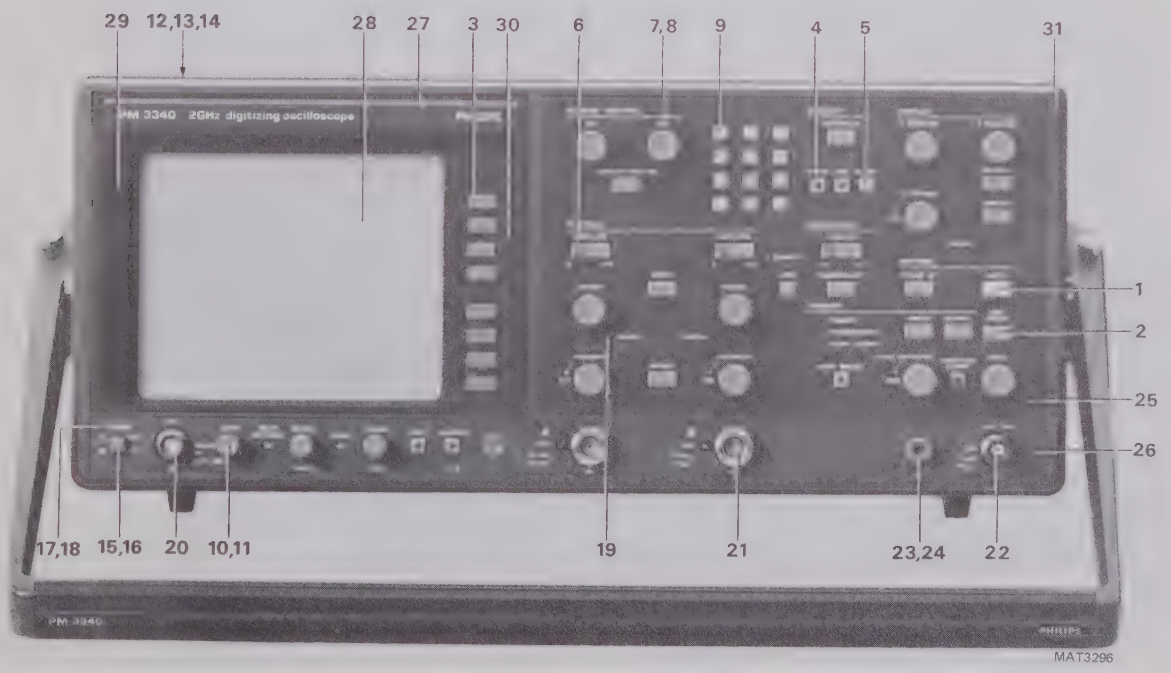

Figure 15.1 Mechanical parts front side.

15.1.2 Mechanical + electrical parts rear side (figure 15.2 and 15.3)

Item	Qty/. instr.	Description	Ordering number
1	4	Distance piece for rear foot	5322 462 50385
2	2	Rear foot (without rubber feet)	5322 462 41135
3	4	Rubber foot for rear foot	5322 462 40765
4	4	Screw for rear foot	5322 502 12882
5	4	Distance peace for rear foot	5322 532 24591
6	4	Washer	5322 532 14593
7	4	Spring washer	4822 530 80163
8	1	Cover for battery holder	5322 462 40766
9	2	Battery holder	5322 256 64014
10	1	Rear textplate	5322 447 91374
11	1	PLOT output socket X17	4822 267 40039
12	1	Power inlet X19 (Fuse holder + mains input socket)	5322 265 20353
13	1	Fuse 2,5 A TZ F1	4822 253 30026
14	1	Fan M1	5322 361 10453
15	1	Fan protection grid	5322 466 30269
16	2	Rear profile (without strip and grounding joint)	5322 466 61552
17	70cm	HF grounding joint for rear profile	5322 466 61551

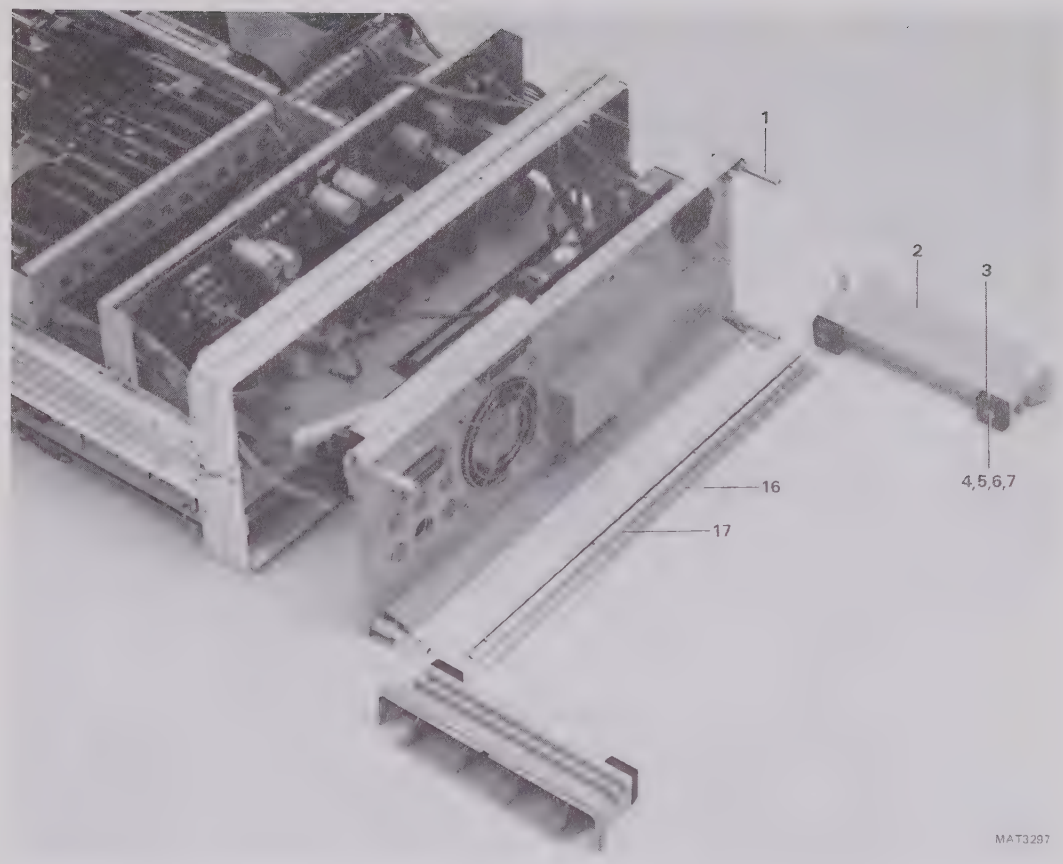

Figure 15.2 Mechanical parts rear side.

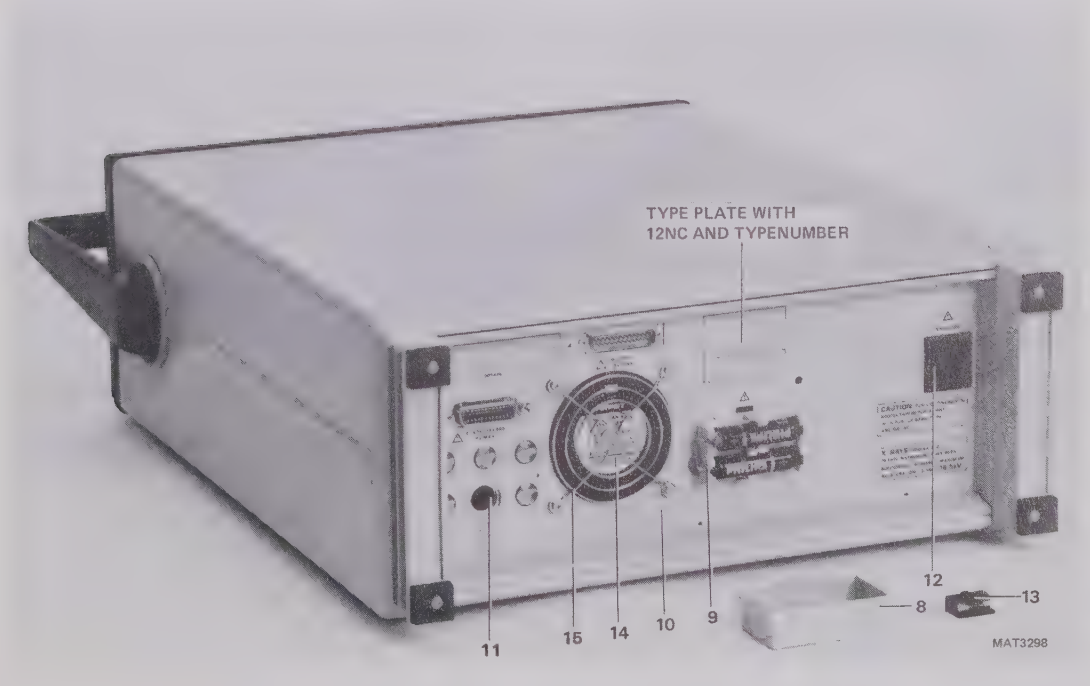

Figure 15.3 Mechanical parts rear side.

15.1.3 Carrying handle and housing (figure 15.4 and 15.5)

Carrying handle

Item	Qty/. instr.	Description	Ordering number
1	2	Locking pin	5322 535 74401
2	2	Spring	5322 492 54155
3	1	Handle arm left	5322 498 50225
4	1	Handle arm right	5322 498 50226
5	1	Metal carrying profile	5322 466 61554
6	1	Plastic carrying profile cover	5322 466 61555
7	1	Textstrip	5322 455 21358
8	4	Screw	4822 502 10064
A	2	Ratchet Block	18592
B	4	Screws for Ratchet block	39168

Housing

Item	Qty/. instr.	Description	Ordering number
9	2	Beige side profile (left or right)	5322 466 61553
10	2	Beige handle ring	5322 498 50242
11	1	Top cover	5322 462 71475
12	4	Fixing part for pouch (top side)	5322 462 71476
13	1	Bottom cover	5322 447 91556
14	4	Foot (bottom side)	5322 462 44297

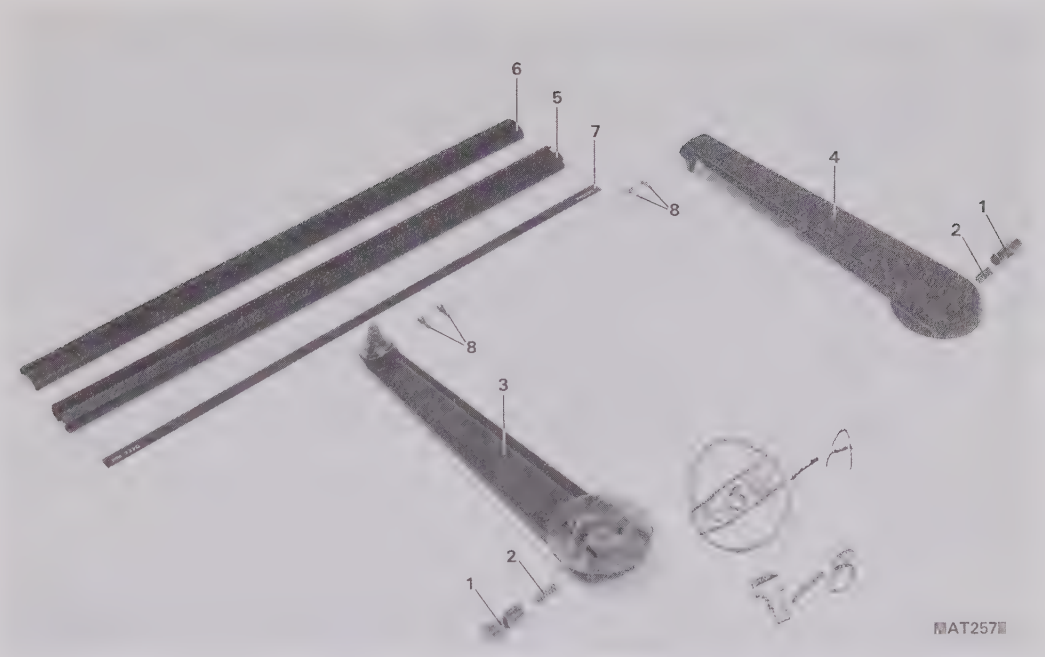

Figure 15.4 Carrying handle.

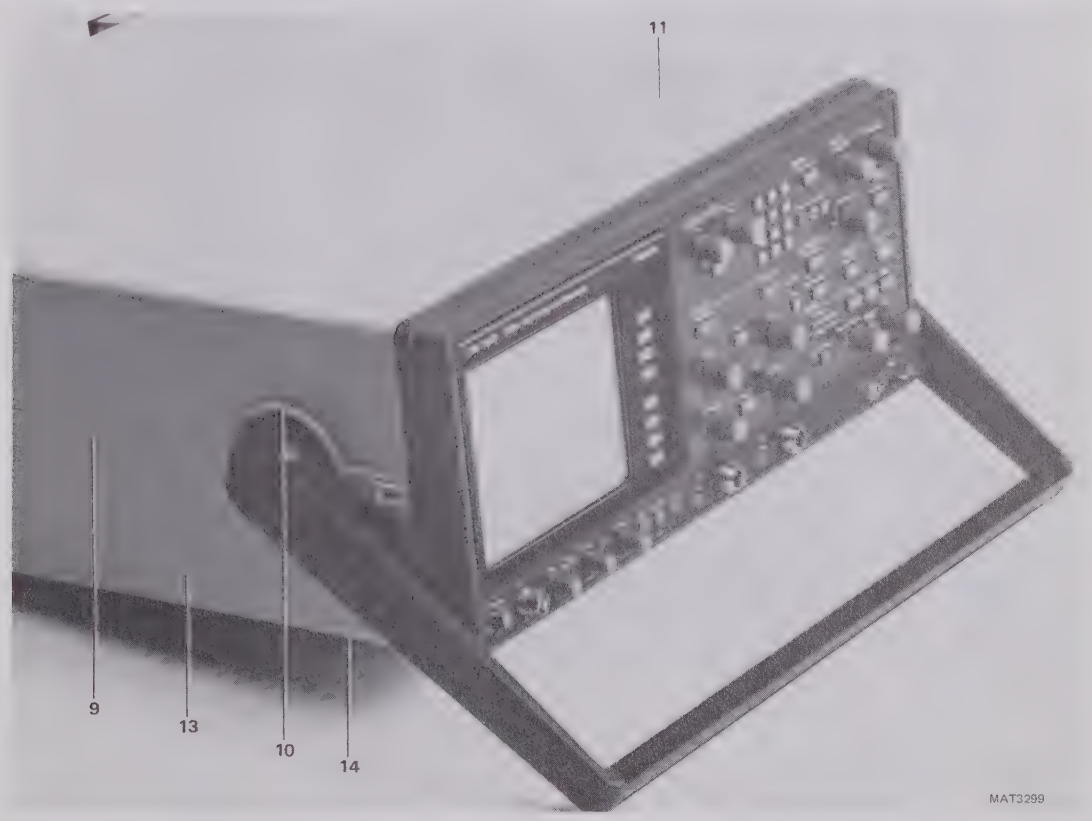

Figure 15.5 Housing.

15.1.4 Internal mechanical parts for front unit (figure 15.6)

Item	Qty/. instr.	Description	Ordering number
1	11	Prism for rotary shaft encoder	5322 256 91198
2	11	Lock for rotary shaft encoder	5322 532 51869
3	11	Rotary shaft encoder	5322 535 91823
4	11	Fixture for leds and fototransistors	5322 256 91199
5	4	Nut for textplate	5322 505 14186
6	4	Spacer for textplate	5322 532 21284
7	6	Distance piece M3 x 5 (between units)	5322 535 92336
8	6	Distance piece M3 x 20	5322 535 91905

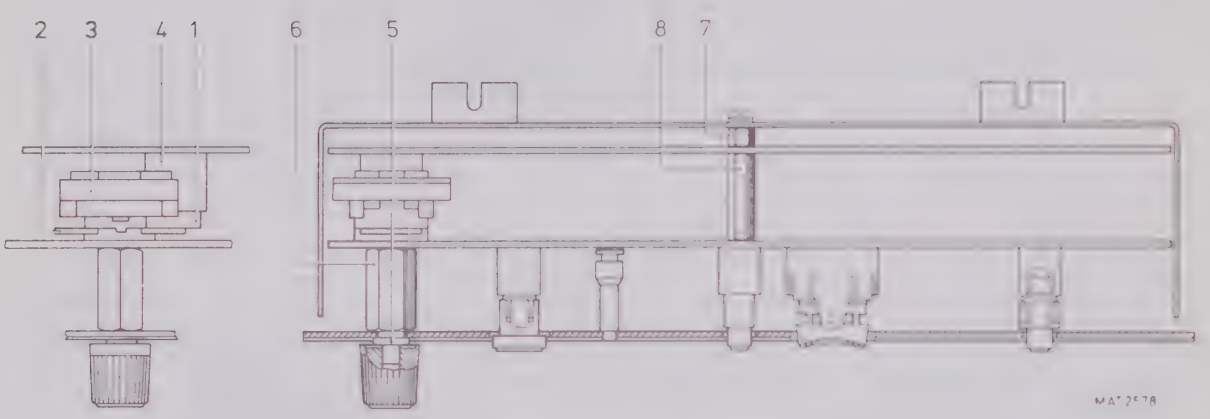

Figure 15.6 Mechanical parts front unit.

15.1.5 C.R.T. fixing materials (figure 15.7)

Item	Qty/. instr.	Description	Ordering number
1	1	C.R.T. socket X1504	5322 255 40502
2	1	Earthing spring for C.R.T. shielding	5322 492 63718
3	6	Gummi parts in C.R.T. shielding	5322 466 61556
4	1	Plastic/rubber pressure support for C.R.T.	5322 462 41136
5	3	Gummi parts around C.R.T. front	5322 532 11588
6	1	Plastic clamping fork for front side of C.R.T.	5322 401 11112
7	1	Metal wedge for front side of C.R.T.	5322 535 20072
8	1	Metal clamping piece for front side of C.R.T.	5322 535 20071

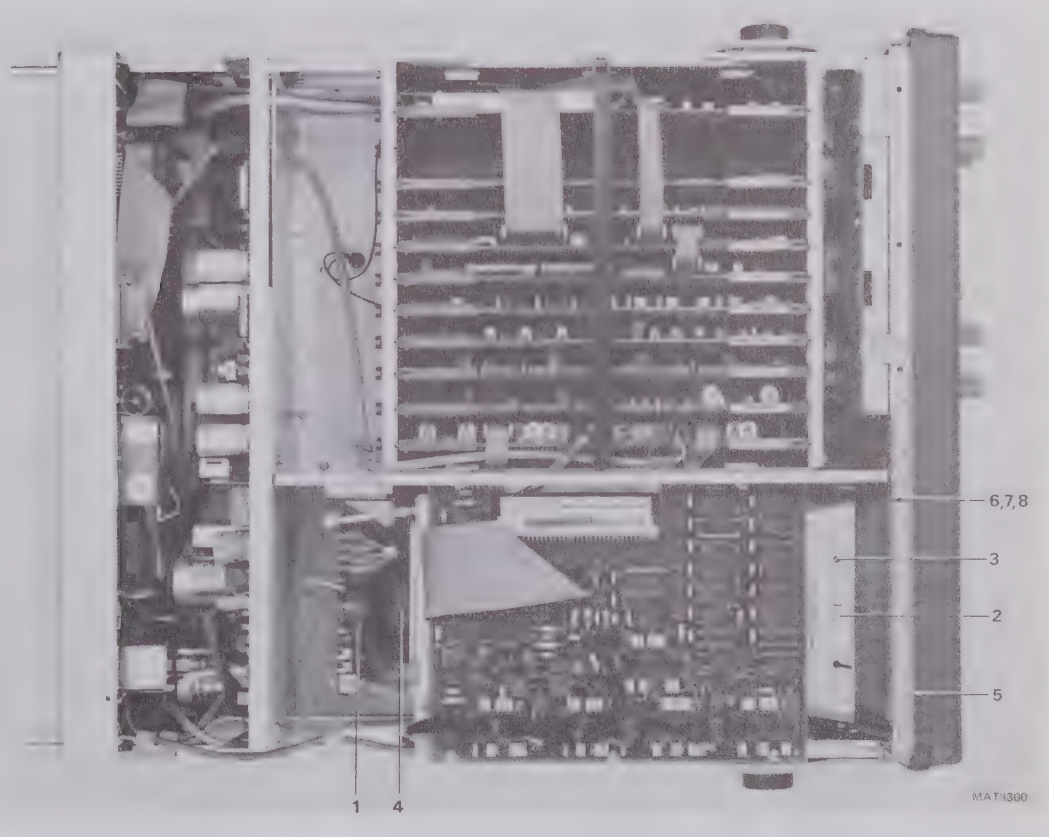

Figure 15.7 C.R.T. fixing materials.

15.2 ELECTRICAL UNITS (Figures 15,8 and 15,9)

Item	Description	Ordering number
A1	Final amplifier unit	5322 216 51154
A2	Display dac unit	5322 216 51155
A3	Display control unit	5322 216 51156
A4	Display memory unit	5322 216 51157
A5	GRAM unit	5322 216 51217
A6	UPROC unit	5322 214 90187
A8	DPU control unit	5322 216 51161
A9	DPU unit	5322 216 51162
A11	ADC + T&H unit	5322 216 51163
A13	FRONT 1 unit	5322 216 51176
A14	FRONT 2 unit	5322 216 51178
A15	Z-amplifier unit	5322 216 51164
A16	C.R.T. control unit	5322 216 51179
A17	Softkey unit	5322 218 41031
A18	SMOOTH + DOTS unit	5322 216 51181
A19	POWER 1 unit	5322 216 51182
A20	POWER 2 unit	5322 216 51183
A25	Management unit	5322 216 51218
A31	Trigger input unit	5322 216 51219
A32	Three stage trigger unit	5322 216 51221
A34	Trigger control unit	5322 216 51222
A51	Time-base unit	5322 216 51223
A52	Fast ramp unit	5322 216 51224
A53	Distribution unit	5322 216 51225
A54	Gate unit (incl. aluminium housing)	5322 219 81163
A55	Vertical signal unit	5322 216 51226
A56	Trigger pick-off	5322 321 22892
A69	Delay line unit	5322 320 40182
-	Extension board	5322 216 51153
-	EHT unit	5322 216 51177
-	Set of software (inclusive FFT)	5322 310 10309

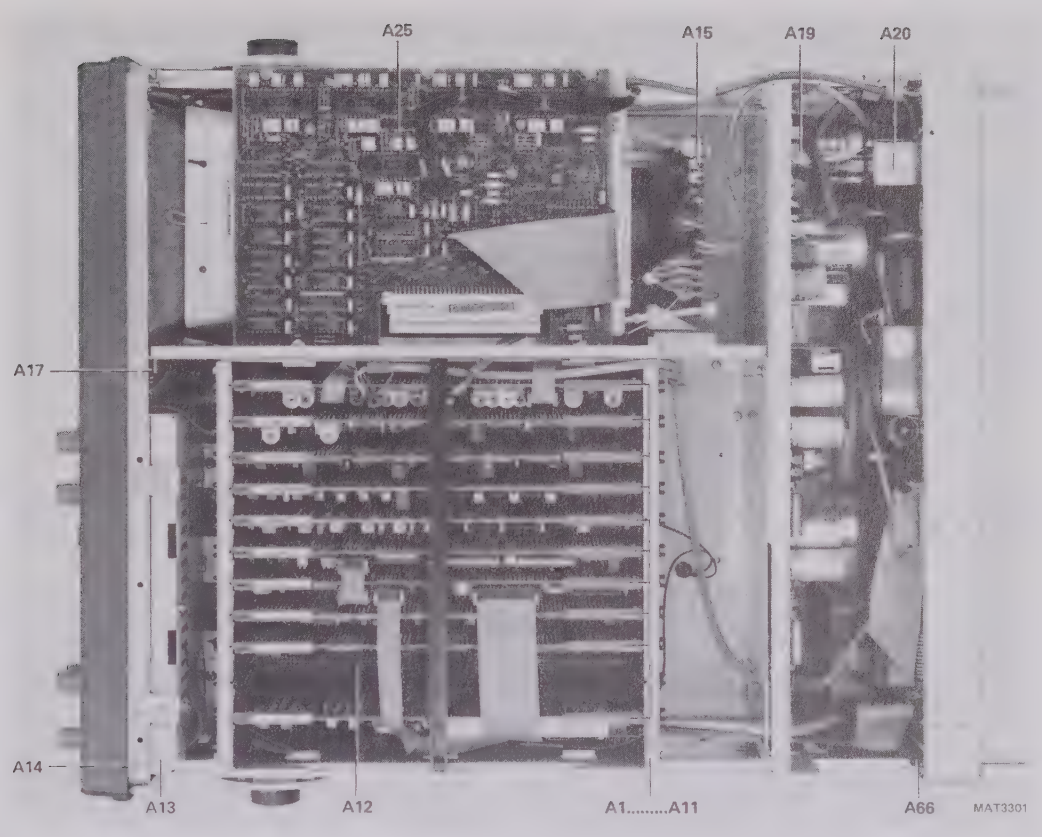

Figure 15.8 Position of electrical units.

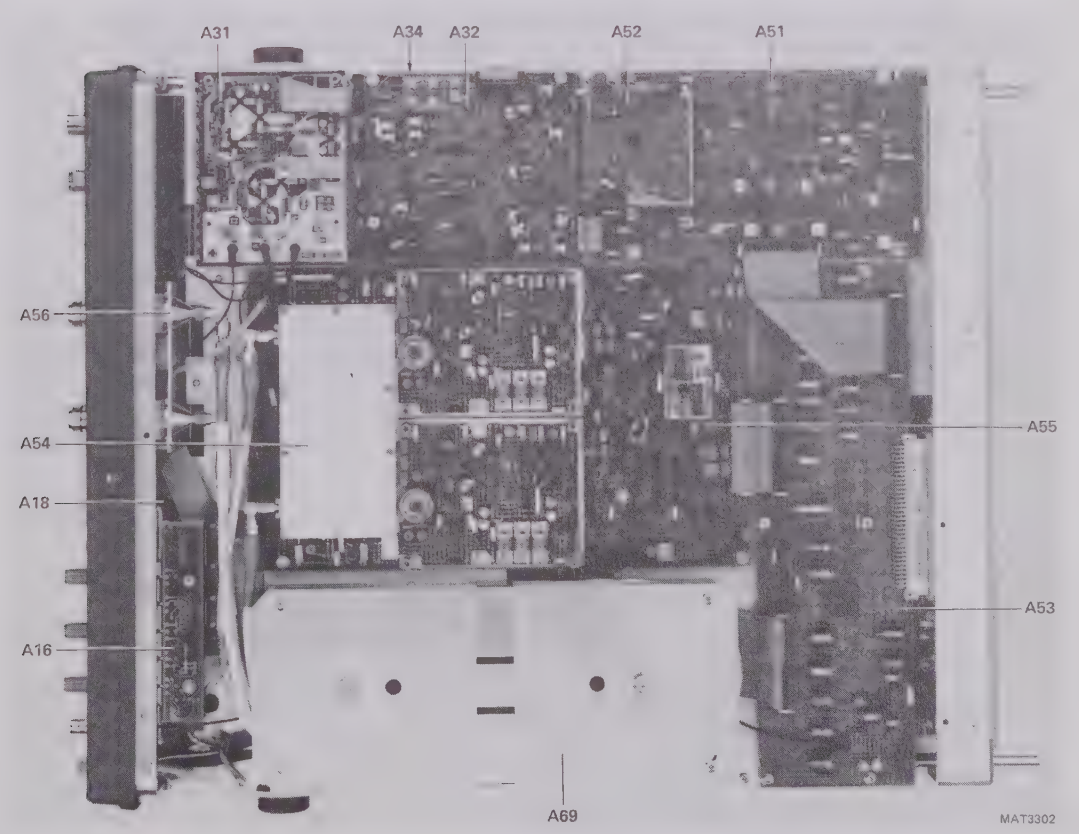

Figure 15.9 Position of electrical units.

15.3 CABLES AND CONNECTORS

15.3.1 Flatcables and connectors

For the flatcables used in this oscilloscope, the required version must be made by yourself with the following parts:

- Universal flatcable, 40 wires, length 60 cm 5322 323 50112

To get the required number of wires the flat cable must be split by means of a pair of scissors or a knife.
The cable must be cut on the required length.

- Flatcable connectors

The connectors can be mounted on the flatcable by means of a pair of pliers or in a bench-vice.

Attention: check the position of the flatcable in the connector before pressing the connector together.

The following connectors are available:	Ordering number:
10 pole cable connector	5322 265 51117
20 pole cable connector	5322 265 54059
24 pole cable connector	5322 265 51114
26 pole cable connector	5322 267 60164
34 pole cable connector	5322 267 70163
40 pole cable connector	5322 267 70162

15.3.2 50 Ohm cables

The 50 Ohm coax-cables are standardized, so some cables are a little bit too long.
The tules around the cable ends can have a different colour, but if necessary it can be replaced by the original one.

Connectors	Remarks	Ordering number
	Cable length: 20 cm	5322 321 21291
	Cable length: 26 cm	5322 321 21293
	Cable length: 31 cm	5322 321 21292
	Cable length: 40 cm	5322 321 21297
	Cable length: 51 cm	5322 321 21294

15.3.3 50 Ohm coax-connector socket (35 connectors per instrument)

	Ordering number
Outer part (bush)	5322 268 24116
Inner part (pin)	5322 268 14141

15.3.4 50 Ohm rectangular SMA connector (4 connectors per instrument)

Ordering number
5322 263 21008

15.4 MISCELLANEOUS PARTS (except electrical parts, Figure 15.10)

Item	Qty/. instr.	Description	Ordering number
1	1	C.R.T. D18-190GH/129 V1	5322 131 20205
2	22	Plastic conductor for units A1..A11	5322 401 11109
3	22	Red p.c.b. handle	5322 401 11108
4	22	Pin for red p.c.b. handle	5322 402 10036
5	1	Bracket over plug-in units	5322 401 11113
6	3	Ball cord for unit A15	5322 401 11114
7	5	Spring for heatsink on unit A19 for transistors: V4447 - V4448 - V4429 - V4424 - V4426	5322 492 63721
8	1	Bracket for high voltage unit D4601	5322 401 11111
9	1	Power on switch S1	5322 276 11859
-	110	Coding pin for DIN connectors	5322 268 10254

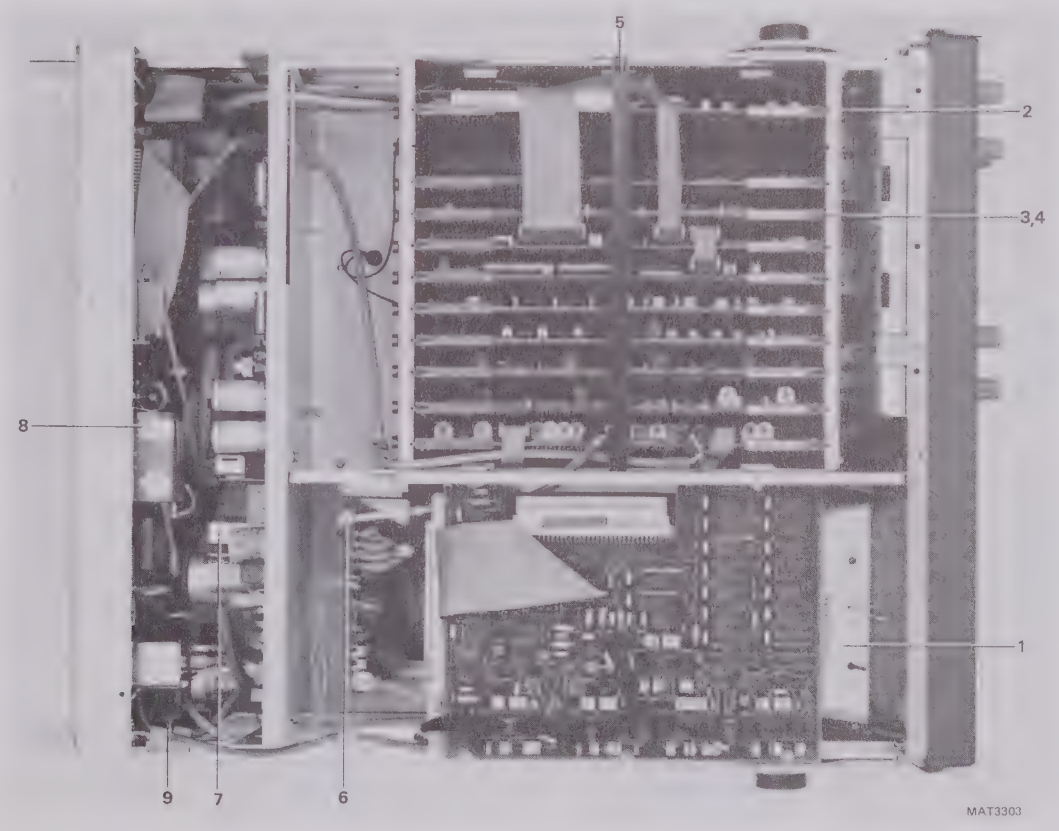

Figure 15.10 Miscellaneous parts.

15.5 MAINS CORDS:

	Last digit 12nc of oscilloscope (on packing)	
European version	1	5322 321 21616
U.S.A. version	3	5322 321 10446
U.K. version	4	5322 321 21617
Swiss version	5	5322 321 21618
Australian version	8	5322 321 21781

15.6 TOOLS:

Cutnipper	5322 395 71004
Extension board	5322 216 51153

15.7 ELECTRICAL PARTS

The opening of parts, or removal of covers, is likely to expose live conductors. The instrument should therefore be disconnected from all voltage sources before any opening of parts or removal of covers is started.
During and after dismantling, bear in mind that capacitors in the instrument may still be charged even if the instrument has been separated from all voltage sources.

CAPACITORS

POSNR	DESCRIPTION		ORDERING CODE
C 0601	-10+50%	47UF	4822 124 20699
C 0602	-20+50%	10NF	4822 122 31414
C 0603	-20+50%	10NF	4822 122 31414
C 0604	2%	10PF	4822 122 32185
C 0606	-20+50%	10NF	4822 122 31414
C 0609	-10+50%	47UF	4822 124 20699
C 0611	-20+50%	10NF	4822 122 31414
C 0612	-10+50%	47UF	4822 124 20699
C 0613	-20+50%	10NF	4822 122 31414
C 0614	-20+50%	10NF	4822 122 31414
C 0616	-20+50%	10NF	4822 122 31414
C 0617	-20+50%	10NF	4822 122 31414
C 0618	-10+50%	47UF	4822 124 20699
C 0619	-20+50%	10NF	4822 122 31414
C 0621	-20+50%	10NF	4822 122 31414
C 0622	-10+50%	47UF	4822 124 20699
C 0623	-20+50%	10NF	4822 122 31414
C 0624	-10+50%	100UF	4822 124 20701
C 0626	-20+50%	10NF	4822 122 31414
C 0627	-10+50%	100UF	4822 124 20701
C 0628	-20+50%	10NF	4822 122 31414
C 0629	-10+50%	100UF	4822 124 20701
C 0631	-20+50%	10NF	4822 122 31414
C 0632	-10+50%	6.8UF	4822 124 20741
C 0633	-20+50%	10NF	4822 122 31414
C 0634	-10+50%	6.8UF	4822 124 20741
C 0636	-20+50%	10NF	4822 122 31414
C 0637	-10+50%	100UF	4822 124 20701
C 0638	-20+50%	10NF	4822 122 31414
C 0639	-20+50%	10NF	4822 122 31414
C 0641	-20+50%	10NF	4822 122 31414
C 0642	-20+50%	10NF	4822 122 31414
C 0643	-20+50%	10NF	4822 122 31414
C 0644	-20+50%	10NF	4822 122 31414
C 0646	-20+50%	10NF	4822 122 31414
C 0647	-20+50%	10NF	4822 122 31414
C 0648	-20+50%	10NF	4822 122 31414
C 0649	-20+50%	10NF	4822 122 31414
C 0651	-10+50%	47UF	4822 124 20699
C 0652	-20+50%	10NF	4822 122 31414
C 0654	-20+50%	10NF	4822 122 31414
C 0658	-10+50%	47UF	4822 124 20699
C 0659	-10+50%	47UF	4822 124 20699
C 0661	-10+50%	6.8UF	4822 124 20741
C 0662	-10+50%	6.8UF	4822 124 20741
C 0663	-10+50%	6.8UF	4822 124 20741
C 0664	-10+50%	330UF	4822 124 20705
C 0667	-20+50%	10NF	4822 122 31414
C 0701	-20+50%	10NF	4822 122 31414
C 0702	-10+50%	100UF	4822 124 20701
C 0901	50V 5%	1.2PF	5322 122 33537
C 0902	50V 5%	1.2PF	5322 122 33537
C 0904	50V 5%	47PF	5322 122 32452
C 0906	50V 5%	150PF	5322 122 33538
C 0907	50V 10%	22NF	5322 122 32654
C 0908	50V 10%	22NF	5322 122 32654
C 0909	50V 5%	150PF	5322 122 33538
C 0911	50V 5%	150PF	5322 122 33538
C 0912	50V 5%	1PF	5322 122 32447
C 0913	50V 5%	1PF	5322 122 32447
C 0914	50V 5%	3.3PF	5322 122 32449
C 0916	50V 5%	5.6PF	5322 122 32967
C 0917	50V 5%	5.6PF	5322 122 32967
C 0918	50V 5%	150PF	5322 122 33538
C 0919	50V 5%	150PF	5322 122 33538
C 0921	50V 5%	3.3PF	5322 122 32449
C 0922	50V 5%	1NF	5322 122 32531
C 0923	50V 5%	1NF	5322 122 32531
C 0924	50V 10%	22NF	5322 122 32654
C 0926	50V 10%	22NF	5322 122 32654
C 0927	50V 5%	5.6PF	5322 122 32967
C 0928	50V 5%	5.6PF	5322 122 32967
C 0929	50V 5%	1.2PF	5322 122 33537
C 0931	50V 5%	1.2PF	5322 122 33537
C 0933	50V 10%	22NF	5322 122 32654
C 0934	50V 10%	22NF	5322 122 32654
C 1201	-20+50%	10NF	4822 122 31414
C 1203	-20+50%	10NF	4822 122 31414
C 1204	-20+50%	10NF	4822 122 31414
C 1206	-20+50%	10NF	4822 122 31414
C 1207	-20+50%	10NF	4822 122 31414
C 1208	-20+50%	10NF	4822 122 31414
C 1216	-20+50%	10NF	4822 122 31414
C 1217	-20+50%	10NF	4822 122 31414
C 1219	-20+50%	10NF	4822 122 31414
C 1223	-20+50%	10NF	4822 122 31414
C 1224	-20+50%	10NF	4822 122 31414
C 1229	-20+50%	10NF	4822 122 31414

POSNR	DESCRIPTION		ORDERING CODE
C 1234	-20+50%	10NF	4822 122 31414
C 1236	-20+50%	10NF	4822 122 31414
C 1237	-20+50%	10NF	4822 122 31414
C 1238	-20+50%	10NF	4822 122 31414
C 1239	-20+50%	10NF	4822 122 31414
C 1241	-20+50%	10NF	4822 122 31414
C 1242	-20+50%	10NF	4822 122 31414
C 1243	-20+50%	10NF	4822 122 31414
C 1244	-20+50%	10NF	4822 122 31414
C 1248	-20+50%	10NF	4822 122 31414
C 1249	10V 20%	10UF	5322 124 21956
C 1251	10V 20%	33UF	5322 124 21957
C 1252	-20+50%	10NF	4822 122 31414
C 1253	-20+50%	10NF	4822 122 31414
C 1254	2%	56PF	4822 122 32027
C 1256	2%	68PF	4822 122 31349
C 1257	2%	56PF	4822 122 32027
C 1258	2%	56PF	4822 122 32027
C 1259	2%	56PF	4822 122 32027
C 1301	50V 10%	22NF	5322 122 32654
C 1302	50V 10%	22NF	5322 122 32654
C 1303	16V 20%	10UF	5322 124 41622
C 1304	50V 10%	22NF	5322 122 32654
C 1306	50V 5%	10PF	5322 122 32448
C 1307	50V 10%	22NF	5322 122 32654
C 1308	50V 10%	22NF	5322 122 32654
C 1309	16V 20%	10UF	5322 124 41622
C 1311	50V 10%	22NF	5322 122 32654
C 1312	50V 10%	22NF	5322 122 32654
C 1313	16V 20%	10UF	5322 124 41622
C 1314	50V 10%	22NF	5322 122 32654
C 1316	50V 5%	10PF	5322 122 32448
C 1317	50V 10%	22NF	5322 122 32654
C 1318	50V 10%	22NF	5322 122 32654
C 1319	16V 20%	10UF	5322 124 41622
C 1321	50V 10%	22NF	5322 122 32654
C 1322	50V 5%	10PF	5322 122 32448
C 1323	50V 10%	22NF	5322 122 32654
C 1324	50V 10%	22NF	5322 122 32654
C 1326	16V 20%	10UF	5322 124 41622
C 1327	50V 10%	22NF	5322 122 32654
C 1328	50V 5%	10PF	5322 122 32448
C 1329	50V 10%	22NF	5322 122 32654
C 1331	50V 10%	22NF	5322 122 32654
C 1332	50V 10%	22NF	5322 122 32654
C 1333	50V 5%	1NF	5322 122 32531
C 1334	50V 10%	22NF	5322 122 32654
C 1336	50V 5%	1NF	5322 122 32531
C 1337	50V 10%	22NF	5322 122 32654
C 1338	50V 10%	22NF	5322 122 32654
C 1339	50V 10%	22NF	5322 122 32654
C 1341	50V 10%	22NF	5322 122 32654
C 1342	50V 5%	56PF	5322 122 32661
C 1343	50V 5%	56PF	5322 122 32661
C 1344	50V 10%	22NF	5322 122 32654
C 1346	50V 5%	56PF	5322 122 32661
C 1347	50V 5%	56PF	5322 122 32661
C 1348	50V 5%	100PF	5322 122 32532
C 1349	50V 10%	22NF	5322 122 32654
C 1351	50V 5%	3.3PF	5322 122 32449
C 1352	50V 5%	3.3PF	5322 122 32449
C 1353	50V 10%	10NF	5322 122 34098
C 1354	50V 10%	22NF	5322 122 32654
C 1356	10V 20%	33UF	5322 124 21957
C 1357	10V 20%	33UF	5322 124 21957
C 1358	50V 10%	22NF	5322 122 32654
C 1359	50V 10%	22NF	5322 122 32654
C 1361	50V 10%	22NF	5322 122 32654
C 1362	50V 10%	22NF	5322 122 32654
C 1363	16V 20%	10UF	5322 124 41622
C 1364	50V 10%	22NF	5322 122 32654
C 1366	50V 10%	22NF	5322 122 32654
C 1367	16V 20%	10UF	5322 124 41622
C 1368	50V 5%	1NF	5322 122 32531
C 1369	50V 10%	22NF	5322 122 32654
C 1371	16V 20%	10UF	5322 124 41622
C 1372	50V 10%	22NF	5322 122 32654
C 1373	50V 5%	10PF	5322 122 32448
C 1374	50V 5%	10PF	5322 122 32448
C 1376	50V 5%	10PF	5322 122 32448
C 1377	50V 10%	22NF	5322 122 32654
C 1378	50V 10%	22NF	5322 122 32654
C 1379	16V 20%	10UF	5322 124 41622
C 1381	50V 5%	10PF	5322 122 32448
C 1402	10V 20%	33UF	5322 124 21957
C 1403	-20+50%	10NF	4822 122 31414
C 1404	-20+50%	10NF	4822 122 31414
C 1406	-20+50%	10NF	4822 122 31414
C 1407	-20+50%	10NF	4822 122 31414
C 1408	-20+50%	10NF	4822 122 31414

POSNR	DESCRIPTION		ORDERING CODE
C 1409	-20+50%	10NF	4822 122 31414
C 1411	-20+50%	10NF	4822 122 31414
C 1412	-20+50%	10NF	4822 122 31414
C 1413	-20+50%	10NF	4822 122 31414
C 1414	2%	12PF	4822 122 31056
C 1416	2%	100PF	4822 122 31316
C 1701	-20+50%	10NF	4822 122 31414
C 1702	-20+50%	10NF	4822 122 31414
C 1704	-20+50%	10NF	4822 122 31414
C 1717	-20+50%	10NF	4822 122 31414
C 1718	-20+50%	10NF	4822 122 31414
C 1719	-20+50%	10NF	4822 122 31414
C 1721	-20+50%	10NF	4822 122 31414
C 1722	-20+50%	10NF	4822 122 31414
C 1723	-20+50%	10NF	4822 122 31414
C 1724	-20+50%	10NF	4822 122 31414
C 1726	-20+50%	10NF	4822 122 31414
C 1727	-20+50%	10NF	4822 122 31414
C 1728	-20+50%	10NF	4822 122 31414
C 1731	-20+50%	10NF	4822 122 31414
C 1746	-20+50%	10NF	4822 122 31414
C 1747	-20+50%	10NF	4822 122 31414
C 1751	10V 20%	33UF	5322 124 21957
C 1752	10V 20%	33UF	5322 124 21957
C 1753	10V 20%	33UF	5322 124 21957
C 1754	0.25PF	0.56PF	5322 122 32107
C 1756	2%	150PF	4822 122 31413
C 1757	2%	33PF	5322 122 32072
C 1758	2%	100PF	4822 122 31316
C 1759	2%	150PF	4822 122 31413
C 1761	2%	100PF	4822 122 31316
C 1762	0.25PF	6.8PF	4822 122 31049
C 1772	10V 20%	33UF	5322 124 21957
C 1773	10V 20%	33UF	5322 124 21957
C 1776	10V 20%	33UF	5322 124 21957
C 1777	10V 20%	33UF	5322 124 21957
C 1778	10V 20%	33UF	5322 124 21957
C 1791	2%	100PF	4822 122 31316
C 1792	2%	330PF	4822 122 31353
C 1801	10V 20%	10UF	5322 124 21956
C 1802	63V 10%	100NF	5322 121 42492
C 1803	10V 20%	33UF	5322 124 21957
C 1804	63V 10%	100NF	5322 121 42492
C 1805	63V 10%	100NF	5322 121 42492
C 1806	63V 10%	100NF	5322 121 42492
C 1807	63V 10%	100NF	5322 121 42492
C 1808	63V 10%	100NF	5322 121 42492
C 1809	63V 10%	100NF	5322 121 42492
C 1810	63V 10%	100NF	5322 121 42492
C 1811	63V 10%	100NF	5322 121 42492
C 1812	63V 10%	100NF	5322 121 42492
C 1813	63V 10%	100NF	5322 121 42492
C 1814	63V 10%	100NF	5322 121 42492
C 1815	63V 10%	100NF	5322 121 42492
C 1816	63V 10%	100NF	5322 121 42492
C 1817	63V 10%	100NF	5322 121 42492
C 1818	10V 20%	10UF	5322 124 21956
C 1819	63V 10%	100NF	5322 121 42492
C 1820	63V 10%	100NF	5322 121 42492
C 1821	63V 10%	100NF	5322 121 42492
C 1822	63V 10%	100NF	5322 121 42492
C 1833	63V 10%	100NF	5322 121 42492
C 1834	63V 10%	100NF	5322 121 42492
C 1836	63V 10%	100NF	5322 121 42492
C 1837	63V 10%	100NF	5322 121 42492
C 1838	63V 10%	100NF	5322 121 42492
C 1852	630V 1%	215PF	5322 121 54075
C 1853	630V 1%	215PF	5322 121 54075
C 1854	2%	27PF	4822 122 30045
C 1856	2%	27PF	4822 122 30045
C 1857	10%	1NF	4822 122 30027
C 1858	630V 1%	215PF	5322 121 54075
C 1861	630V 1%	100PF	4822 121 50562
C 1862	630V 1%	215PF	5322 121 54075
C 1863	2%	27PF	4822 122 30045
C 1864	2%	27PF	4822 122 30045
C 1866	630V 1%	215PF	5322 121 54075
C 1867	10%	470PF	4822 122 30034
C 1868	2%	56PF	4822 122 32027
C 1869	10V 20%	10UF	5322 124 21956
C 1871	10V 20%	10UF	5322 124 21956
C 1881	63V 10%	100NF	5322 121 42492
C 1882	63V 10%	100NF	5322 121 42492
C 1883	63V 10%	100NF	5322 121 42492
C 1884	63V 10%	100NF	5322 121 42492
C 1886	63V 10%	100NF	5322 121 42492
C 1887	63V 10%	100NF	5322 121 42492
C 1888	63V 10%	100NF	5322 121 42492
C 1889	63V 10%	100NF	5322 121 42492
C 1891	63V 10%	100NF	5322 121 42492

POSNR	DESCRIPTION		ORDERING CODE
C 1892	2%	56PF	4822 122 32027
C 1893	2%	330PF	4822 122 31353
C 2002	-20+50%	10NF	4822 122 31414
C 2006	-20+50%	10NF	4822 122 31414
C 2008	-20+50%	10NF	4822 122 31414
C 2009	-20+50%	10NF	4822 122 31414
C 2011	-20+50%	10NF	4822 122 31414
C 2012	-20+50%	10NF	4822 122 31414
C 2013	-20+50%	10NF	4822 122 31414
C 2014	-20+50%	10NF	4822 122 31414
C 2016	-20+50%	10NF	4822 122 31414
C 2017	-20+50%	10NF	4822 122 31414
C 2018	-20+50%	10NF	4822 122 31414
C 2022	-20+50%	10NF	4822 122 31414
C 2023	-20+50%	10NF	4822 122 31414
C 2024	-20+50%	10NF	4822 122 31414
C 2027	-20+50%	10NF	4822 122 31414
C 2028	-20+50%	10NF	4822 122 31414
C 2029	-20+50%	10NF	4822 122 31414
C 2031	-20+50%	10NF	4822 122 31414
C 2034	-20+50%	10NF	4822 122 31414
C 2036	-20+50%	10NF	4822 122 31414
C 2039	-20+50%	10NF	4822 122 31414
C 2041	16V 20%	6.8UF	5322 124 21763
C 2043	16V 20%	6.8UF	5322 124 21763
C 2044	16V 20%	6.8UF	5322 124 21763
C 2046	16V 20%	6.8UF	5322 124 21763
C 2047	2%	68PF	4822 122 31349
C 2048	0.25PF	5.6PF	5322 122 32163
C 2101	-20+50%	10NF	4822 122 31414
C 2102	-20+50%	10NF	4822 122 31414
C 2103	-20+50%	10NF	4822 122 31414
C 2106	-20+50%	10NF	4822 122 31414
C 2107	-20+50%	10NF	4822 122 31414
C 2108	-20+50%	10NF	4822 122 31414
C 2112	-20+50%	10NF	4822 122 31414
C 2115	-20+50%	10NF	4822 122 31414
C 2121	-20+50%	10NF	4822 122 31414
C 2122	-20+50%	10NF	4822 122 31414
C 2123	-20+50%	10NF	4822 122 31414
C 2124	-20+50%	10NF	4822 122 31414
C 2126	-20+50%	10NF	4822 122 31414
C 2128	-20+50%	10NF	4822 122 31414
C 2129	-20+50%	10NF	4822 122 31414
C 2130	-20+50%	10NF	4822 122 31414
C 2136	-20+50%	10NF	4822 122 31414
C 2137	-20+50%	10NF	4822 122 31414
C 2139	-20+50%	10NF	4822 122 31414
C 2141	-20+50%	10NF	4822 122 31414
C 2142	-20+50%	10NF	4822 122 31414
C 2144	-20+50%	10NF	4822 122 31414
C 2145	-20+50%	10NF	4822 122 31414
C 2147	-20+50%	10NF	4822 122 31414
C 2151	-20+50%	10NF	4822 122 31414
C 2156	-20+50%	10NF	4822 122 31414
C 2158	-20+50%	10NF	4822 122 31414
C 2159	16V 20%	6.8UF	5322 124 21763
C 2160	16V 20%	6.8UF	5322 124 21763
C 2161	10%	2.2NF	4822 122 30114
C 2162	-20+50%	4.7NF	4822 122 30128
C 2164	-20+50%	10NF	4822 122 31414
C 2165	-20+50%	6.8NF	4822 122 31429
C 2167	10%	680PF	4822 122 30053
C 2168	16V 20%	6.8UF	5322 124 21763
C 2169	-10+50%	33UF	4822 124 20712
C 2171	16V 20%	6.8UF	5322 124 21763
C 2172	2%	10PF	4822 122 32185
C 2173	2%	68PF	4822 122 31349
C 2201	-10+50%	150UF	4822 124 20672
C 2202	63V 10%	100NF	5322 121 42492
C 2203	63V 10%	100NF	5322 121 42492
C 2204	63V 10%	100NF	5322 121 42492
C 2206	63V 10%	100NF	5322 121 42492
C 2207	63V 10%	100NF	5322 121 42492
C 2208	63V 10%	100NF	5322 121 42492
C 2209	63V 10%	100NF	5322 121 42492
C 2211	63V 10%	100NF	5322 121 42492
C 2212	63V 10%	100NF	5322 121 42492
C 2213	63V 10%	100NF	5322 121 42492
C 2214	63V 10%	100NF	5322 121 42492
C 2216	63V 10%	100NF	5322 121 42492
C 2217	63V 10%	100NF	5322 121 42492
C 2218	63V 10%	100NF	5322 121 42492
C 2219	63V 10%	100NF	5322 121 42492
C 2221	63V 10%	100NF	5322 121 42492
C 2222	-10+50%	150UF	4822 124 20691
C 2223	-10+50%	150UF	4822 124 20672
C 2224	-10+50%	150UF	4822 124 20691

POSNR	DESCRIPTION	ORDERING CODE
C 2226	-10+50% 150UF	4822 124 20691
C 2227	-10+50% 150UF	4822 124 20691
C 2228	-10+50% 150UF	4822 124 20691
C 2229	-10+50% 150UF	4822 124 20672
C 2231	63V 10% 100NF	5322 121 42492
C 2232	63V 10% 100NF	5322 121 42492
C 2233	10% 1NF	4822 122 30027
C 2234	63V 10% 100NF	5322 121 42492
C 2236	63V 10% 100NF	5322 121 42492
C 2237	10% 1NF	4822 122 30027
C 2238	100V 10% 10NF	5322 121 42495
C 2239	160V 1% 22NF	5322 121 51352
C 2241	63V 10% 100NF	5322 121 42492
C 2242	250V 1% 1.5NF	4822 121 42729
C 2243	160V 1% 22NF	5322 121 51352
C 2244	63V 10% 100NF	5322 121 42492
C 2246	250V 1% 1.5NF	4822 121 42729
C 2247	63V 10% 100NF	5322 121 42492
C 2248	-10+50% 150UF	4822 124 20691
C 2249	-10+50% 150UF	4822 124 20691
C 2251	63V 10% 100NF	5322 121 42492
C 2252	63V 10% 100NF	5322 121 42492
C 2253	10V 20% 10UF	5322 124 21956
C 2254	16V 20% 6.8UF	5322 124 21763
C 2256	10V 20% 10UF	5322 124 21956
C 2257	-20+50% 10NF	4822 122 31414
C 2258	-20+50% 10NF	4822 122 31414
C 2259	-20+50% 10NF	4822 122 31414
C 2261	-20+50% 10NF	4822 122 31414
C 2301	16V 20% 6.8UF	5322 124 21763
C 2302	-20+50% 10NF	4822 122 31414
C 2306	-20+50% 10NF	4822 122 31414
C 2319	-20+50% 10NF	4822 122 31414
C 2321	-20+50% 10NF	4822 122 31414
C 2322	-20+50% 10NF	4822 122 31414
C 2323	-20+50% 10NF	4822 122 31414
C 2327	-20+50% 10NF	4822 122 31414
C 2334	16V 20% 6.8UF	5322 124 21763
C 2336	-20+50% 10NF	4822 122 31414
C 2339	63V 10% 100NF	5322 121 42492
C 2341	16V 20% 6.8UF	5322 124 21763
C 2343	16V 20% 6.8UF	5322 124 21763
C 2348	2% 100PF	4822 122 31316
C 2349	2% 100PF	4822 122 31316
C 2351	2% 220PF	4822 122 30094
C 2352	2% 220PF	4822 122 30094
C 2353	63V 10% 100NF	5322 121 42492
C 2354	-20+50% 10NF	4822 122 31414
C 2356	16V 20% 6.8UF	5322 124 21763
C 2357	63V 10% 100NF	5322 121 42492
C 2358	-20+50% 10NF	4822 122 31414
C 2359	16V 20% 6.8UF	5322 124 21763
C 2361	-20+50% 10NF	4822 122 31414
C 2363	63V 10% 100NF	5322 121 42492
C 2364	-20+50% 10NF	4822 122 31414
C 2366	630V 1% 316PF	4822 121 50531
C 2367	630V 1% 316PF	4822 121 50531
C 2369	2% 330PF	4822 122 31353
C 2373	2% 39PF	4822 122 31069
C 2374	63V 10% 100NF	5322 121 42492
C 2376	-20+50% 10NF	4822 122 31414
C 2377	-20+50% 10NF	4822 122 31414
C 2378	-20+50% 10NF	4822 122 31414
C 2379	630V 1% 316PF	4822 121 50531
C 2381	630V 1% 316PF	4822 121 50531
C 2382	-20+50% 10NF	4822 122 31414
C 2383	2% 330PF	4822 122 31353
C 2384	2% 39PF	4822 122 31069
C 2389	-20+50% 10NF	4822 122 31414
C 2391	-20+50% 10NF	4822 122 31414
C 2392	-20+50% 10NF	4822 122 31414
C 2393	25V 20% 6.8UF	5322 124 21961
C 2394	63V 10% 100NF	5322 121 42492
C 2397	-20+50% 10NF	4822 122 31414
C 2398	16V 20% 6.8UF	5322 124 21763
C 2399	-20+50% 10NF	4822 122 31414
C 2401	16V 20% 6.8UF	5322 124 21763
C 2402	63V 10% 100NF	5322 121 42492
C 2403	-20+50% 10NF	4822 122 31414
C 2404	-20+50% 10NF	4822 122 31414
C 2406	-20+50% 10NF	4822 122 31414
C 2407	-20+50% 10NF	4822 122 31414
C 2408	-20+50% 10NF	4822 122 31414
C 2409	-20+50% 10NF	4822 122 31414
C 2411	2% 56PF	4822 122 32027
C 2412	2% 56PF	4822 122 32027
C 2501	-10+50% 22UF	4822 124 20731
C 2502	-20+50% 10NF	4822 122 31414
C 2503	-20+50% 10NF	4822 122 31414
C 2504	-10+50% 22UF	4822 124 20731

POSNR	DESCRIPTION	ORDERING CODE
C 2513	400V 10% 100NF	5322 121 44198
C 2514	2% 100PF	5322 122 32655
C 2522	-10+50% 47UF	4822 124 20699
C 2523	-20+50% 10NF	4822 122 31414
C 2524	-20+50% 10NF	4822 122 31414
C 2526	-20+50% 10NF	4822 122 31414
C 2527	-20+50% 10NF	4822 122 31414
C 2528	-20+50% 10NF	4822 122 31414
C 2534	-10+50% 47UF	4822 124 20699
C 2536	-20+50% 10NF	4822 122 31414
C 2537	-20+50% 10NF	4822 122 31414
C 2547	-10+50% 100UF	4822 124 20679
C 2551	-20+50% 10NF	4822 122 31414
C 2552	-20+50% 10NF	4822 122 31414
C 2553	-20+50% 10NF	4822 122 31414
C 2559	-10+50% 100UF	4822 124 20679
C 2561	-20+50% 10NF	4822 122 31414
C 2562	-20+50% 10NF	4822 122 31414
C 2563	-20+50% 10NF	4822 122 31414
C 2564	-20+50% 10NF	4822 122 31414
C 2566	-20+50% 10NF	4822 122 31414
C 2572	-10+50% 100UF	4822 124 20679
C 2573	-20+50% 10NF	4822 122 31414
C 2574	-20+50% 10NF	4822 122 31414
C 2583	-20+50% 10NF	4822 122 31414
C 2584	-20+50% 10NF	4822 122 31414
C 2587	-20+50% 10NF	4822 122 31414
C 2591	2% 100PF	4822 122 31316
C 2592	2% 100PF	4822 122 31316
C 2594	63V 10% 100NF	5322 121 42492
C 2595	63V 10% 100NF	5322 121 42492
C 2596	-20+50% 10NF	4822 122 31414
C 2597	-20+50% 10NF	4822 122 31414
C 2613	0.25PF 0.56PF	5322 122 32107
C 2616	2% 39PF	4822 122 31069
C 2617	2% 39PF	4822 122 31069
C 2621	10% 470PF	4822 122 30034
C 2626	100V 10% 47NF	5322 121 42491
C 2627	2% 220PF	4822 122 30094
C 2632	-20+50% 10NF	4822 122 31414
C 2633	-20+50% 10NF	4822 122 31414
C 2642	-20+50% 10NF	4822 122 31414
C 2643	-20+50% 10NF	4822 122 31414
C 2646	-20+50% 10NF	4822 122 31414
C 2651	-20+50% 10NF	4822 122 31414
C 2652	16V 20% 6.8UF	5322 124 21763
C 2653	2% 100PF	4822 122 31316
C 2661	-20+50% 10NF	4822 122 31414
C 2662	-20+50% 10NF	4822 122 31414
C 2663	-20+50% 10NF	4822 122 31414
C 2664	-20+50% 10NF	4822 122 31414
C 2666	2% 47PF	4822 122 31072
C 2801	400V 10% 100NF	5322 121 44198
C 2802	-20+50% 10NF	4822 122 31414
C 2803	20% 470PF	5322 122 50086
C 2804	2% 100PF	4822 122 31316
C 2805	-20+50% 10NF	5322 122 50091
C 2806	20% 1NF	5322 122 50077
C 2807	400V 10% 100NF	5322 121 44198
C 2808	-20+50% 10NF	5322 122 50091
C 2810	-20+50% 10NF	5322 122 50091
C 2811	-20+50% 10NF	4822 122 31414
C 2812	-20+50% 10NF	4822 122 31414
C 2813	-20+50% 10NF	4822 122 31414
C 2814	-20+50% 10NF	4822 122 31414
C 3101	2% 22PF	5322 122 32143
C 3102	-10+50% 100UF	4822 124 20679
C 3103	63V 10% 100NF	5322 121 42492
C 3104	63V 10% 100NF	5322 121 42492
C 3106	-10+50% 47UF	4822 124 20699
C 3107	63V 10% 100NF	5322 121 42492
C 3108	-10+50% 47UF	4822 124 20699
C 3109	63V 10% 100NF	5322 121 42492
C 3111	-10+50% 47UF	4822 124 20699
C 3112	63V 10% 100NF	5322 121 42492
C 3113	-10+50% 47UF	4822 124 20699
C 3114	63V 10% 100NF	5322 121 42492
C 3116	-10+50% 100UF	4822 124 20679
C 3117	63V 10% 100NF	5322 121 42492
C 3118	-10+50% 68UF	4822 124 20689
C 3121	2% 18PF	4822 122 31061
C 3122	2% 18PF	4822 122 31061
C 3123	2% 18PF	4822 122 31061
C 3124	2% 18PF	4822 122 31061
C 3126	63V 10% 100NF	5322 121 42492
C 3127	100V 10% 10NF	5322 121 42495
C 3128	63V 10% 100NF	5322 121 42492
C 3129	63V 10% 100NF	5322 121 42492
C 3131	10% 1NF	4822 122 30027
C 3132	10% 1.5NF	4822 122 31169

POSNR	DESCRIPTION			ORDERING CODE
C 3133	63V	10%	100NF	5322 121 42492
C 3134	63V	10%	100NF	5322 121 42492
C 3136	63V	10%	100NF	5322 121 42492
C 3137	63V	10%	100NF	5322 121 42492
C 3138	63V	10%	100NF	5322 121 42492
C 3139	100V	10%	10NF	5322 121 42495
C 3141	100V	10%	10NF	5322 121 42495
C 3142	100V	10%	10NF	5322 121 42495
C 3143	100V	10%	10NF	5322 121 42495
C 3144	100V	10%	10NF	5322 121 42495
C 3146	63V	10%	100NF	5322 121 42492
C 3147	100V	10%	10NF	5322 121 42495
C 3148	63V	10%	100NF	5322 121 42492
C 3149	63V	10%	100NF	5322 121 42492
C 3151		10%	1NF	4822 122 30027
C 3152		10%	1.5NF	4822 122 31169
C 3153	63V	10%	100NF	5322 121 42492
C 3154	63V	10%	100NF	5322 121 42492
C 3156	63V	10%	100NF	5322 121 42492
C 3157	63V	10%	100NF	5322 121 42492
C 3158	63V	10%	100NF	5322 121 42492
C 3159	100V	10%	10NF	5322 121 42495
C 3161	100V	10%	10NF	5322 121 42495
C 3162	100V	10%	10NF	5322 121 42495
C 3163	100V	10%	10NF	5322 121 42495
C 3164	100V	10%	10NF	5322 121 42495
C 3166	63V	10%	100NF	5322 121 42492
C 3167	100V	10%	10NF	5322 121 42495
C 3168	63V	10%	100NF	5322 121 42492
C 3169	63V	10%	100NF	5322 121 42492
C 3171		10%	1NF	4822 122 30027
C 3172		10%	1.5NF	4822 122 31169
C 3173	63V	10%	100NF	5322 121 42492
C 3174	63V	10%	100NF	5322 121 42492
C 3176	63V	10%	100NF	5322 121 42492
C 3177	63V	10%	100NF	5322 121 42492
C 3178	63V	10%	100NF	5322 121 42492
C 3179	100V	10%	10NF	5322 121 42495
C 3181	100V	10%	10NF	5322 121 42495
C 3182	100V	10%	10NF	5322 121 42495
C 3183	100V	10%	10NF	5322 121 42495
C 3184	100V	10%	10NF	5322 121 42495
C 3186	63V	10%	100NF	5322 121 42492
C 3187	100V	10%	10NF	5322 121 42495
C 3188	63V	10%	100NF	5322 121 42492
C 3189	63V	10%	100NF	5322 121 42492
C 3191		10%	1NF	4822 122 30027
C 3192		10%	1.5NF	4822 122 31169
C 3193	63V	10%	100NF	5322 121 42492
C 3194	63V	10%	100NF	5322 121 42492
C 3196	63V	10%	100NF	5322 121 42492
C 3197	63V	10%	100NF	5322 121 42492
C 3198	63V	10%	100NF	5322 121 42492
C 3199	100V	10%	10NF	5322 121 42495
C 3201	100V	10%	10NF	5322 121 42495
C 3202	100V	10%	10NF	5322 121 42495
C 3203	100V	10%	10NF	5322 121 42495
C 3204	100V	10%	10NF	5322 121 42495
C 3206	63V	10%	100NF	5322 121 42492
C 3207	100V	10%	10NF	5322 121 42495
C 3208	63V	10%	100NF	5322 121 42492
C 3209	63V	10%	100NF	5322 121 42492
C 3211		10%	1NF	4822 122 30027
C 3212		10%	1.5NF	4822 122 31169
C 3213	63V	10%	100NF	5322 121 42492
C 3214	63V	10%	100NF	5322 121 42492
C 3216	63V	10%	100NF	5322 121 42492
C 3217	63V	10%	100NF	5322 121 42492
C 3218	63V	10%	100NF	5322 121 42492
C 3219	100V	10%	10NF	5322 121 42495
C 3221	100V	10%	10NF	5322 121 42495
C 3222	100V	10%	10NF	5322 121 42495
C 3223	100V	10%	10NF	5322 121 42495
C 3224	100V	10%	10NF	5322 121 42495
C 3226	-10+50%		100UF	4822 124 20679
C 3227	63V	10%	100NF	5322 121 42492
C 3228	-10+50%		100UF	4822 124 20679
C 3229	63V	10%	100NF	5322 121 42492
C 3231		2%	18PF	4822 122 31061
C 3232		2%	18PF	4822 122 31061
C 3233	63V	10%	100NF	5322 121 42492
C 3234	63V	10%	100NF	5322 121 42492
C 3237	63V	10%	100NF	5322 121 42492
C 3238	63V	10%	100NF	5322 121 42492
C 3239	63V	10%	100NF	5322 121 42492
C 3241	63V	10%	100NF	5322 121 42492
C 3242	63V	10%	100NF	5322 121 42492
C 3243	63V	10%	100NF	5322 121 42492
C 3244	63V	10%	100NF	5322 121 42492
C 3246	63V	10%	100NF	5322 121 42492

POSNR	DESCRIPTION			ORDERING CODE
C 3247	63V	10%	100NF	5322 121 42492
C 3248	63V	10%	100NF	5322 121 42492
C 3249	63V	10%	100NF	5322 121 42492
C 3251	63V	10%	100NF	5322 121 42492
C 3252	63V	10%	100NF	5322 121 42492
C 3253	63V	10%	100NF	5322 121 42492
C 3254	63V	10%	100NF	5322 121 42492
C 3256	63V	10%	100NF	5322 121 42492
C 3257	63V	10%	100NF	5322 121 42492
C 3258	63V	10%	100NF	5322 121 42492
C 3259	63V	10%	100NF	5322 121 42492
C 3261		2%	18PF	4822 122 31316
C 3262		2%	18PF	4822 122 31316
C 3301	-20+50%		10NF	4822 122 31414
C 3302	-20+50%		10NF	4822 122 31414
C 3304	63V	10%	100NF	5322 121 42492
C 3305	-20+50%		10NF	4822 122 31414
C 3306	16V	20%	6.8UF	5322 124 21763
C 3307		2%	22PF	4822 122 31353
C 3308	-20+50%		10NF	4822 122 31414
C 3309	16V	20%	6.8UF	5322 124 21763
C 3310		10%	1NF	4822 122 30027
C 3313	-20+50%		10NF	4822 122 31414
C 3314	-20+50%		10NF	4822 122 31414
C 3316	63V	10%	100NF	5322 121 42492
C 3317	63V	10%	100NF	5322 121 42492
C 3318	63V	10%	100NF	5322 121 42492
C 3319	63V	10%	100NF	5322 121 42492
C 3321	63V	10%	100NF	5322 121 42492
C 3322	100V	10%	10NF	5322 121 42495
C 3324	100V	10%	10NF	5322 121 42495
C 3325	63V	10%	100NF	5322 121 42492
C 3326	-20+50%		10NF	4822 122 31414
C 3327	63V	10%	100NF	5322 121 42492
C 3328	63V	10%	100NF	5322 121 42492
C 3329	-20+50%		10NF	4822 122 31414
C 3330	16V	20%	6.8UF	5322 124 21763
C 3331	63V	10%	100NF	5322 121 42492
C 3332	-20+50%		10NF	4822 122 31414
C 3333	63V	10%	100NF	5322 121 42492
C 3334	63V	10%	100NF	5322 121 42492
C 3336	63V	10%	100NF	5322 121 42492
C 3337	63V	10%	100NF	5322 121 42492
C 3338	63V	10%	100NF	5322 121 42492
C 3339	63V	10%	100NF	5322 121 42492
C 3341	100V	10%	10NF	5322 121 42495
C 3342	100V	10%	10NF	5322 121 42495
C 3343	100V	10%	10NF	5322 121 42495
C 3344	100V	10%	10NF	5322 121 42495
C 3346		10%	1.5NF	4822 122 31169
C 3347	100V	10%	10NF	5322 121 42495
C 3348	100V	10%	10NF	5322 121 42495
C 3349	100V	10%	10NF	5322 121 42495
C 3351		10%	1.5NF	4822 122 31169
C 3352		10%	1NF	4822 122 30027
C 3353	-20+50%		10NF	4822 122 31414
C 3354	-20+50%		10NF	4822 122 31414
C 3355	-20+50%		10NF	4822 122 31414
C 3356	16V	20%	6.8UF	5322 124 21763
C 3359	-20+50%		10NF	4822 122 31414
C 3360	16V	20%	6.8UF	5322 124 21763
C 3361	63V	10%	100NF	5322 121 42492
C 3362	-20+50%		10NF	4822 122 31414
C 3363	63V	10%	100NF	5322 121 42492
C 3364	63V	10%	100NF	5322 121 42492
C 3368	63V	10%	100NF	5322 121 42492
C 3369		10%	1NF	4822 122 30027
C 3371	63V	10%	100NF	5322 121 42492
C 3372	100V	10%	10NF	5322 121 42495
C 3373	63V	10%	100NF	5322 121 42492
C 3374	63V	10%	100NF	5322 121 42492
C 3376	63V	10%	100NF	5322 121 42492
C 3377	63V	10%	100NF	5322 121 42492
C 3378	63V	10%	100NF	5322 121 42492
C 3379	100V	10%	10NF	5322 121 42495
C 3381	100V	10%	10NF	5322 121 42495
C 3382	100V	10%	10NF	5322 121 42495
C 3383	100V	10%	10NF	5322 121 42495
C 3384	100V	10%	10NF	5322 121 42495
C 3386		10%	1.5NF	4822 122 31169
C 3387		2%	220PF	4822 122 30094
C 3388	-20+50%		10NF	4822 122 31414
C 3390		2%	33PF	4822 122 31353
C 3391	-20+50%		10NF	4822 122 31414
C 3393	63V	10%	100NF	5322 121 42492
C 3394	10V	20%	10UF	5322 124 21956
C 3396	10V	20%	33UF	5322 124 21957
C 3397	-20+50%		10NF	4822 122 31414
C 3398	16V	20%	6.8UF	5322 124 21763
C 3399	10V	20%	33UF	5322 124 21957

POSNR	DESCRIPTION	ORDERING CODE
C 3401	16V 20% 6.8UF	5322 124 21763
C 3402	16V 20% 6.8UF	5322 124 21763
C 3407	-10+50% 150UF	4822 124 20691
C 3408	-10+50% 150UF	4822 124 20691
C 3409	-10+50% 150UF	4822 124 20691
C 3411	-10+50% 150UF	4822 124 20691
C 3413	-10+50% 100UF	4822 124 20701
C 3501	50V 10% 22NF	5322 122 32654
C 3502	50V 10% 22NF	5322 122 32654
C 3504	50V 5% 33PF	5322 122 32659
C 3506	7-10.0 PF MUR	5322 125 11013
C 3508	50V 5% 560PF	5322 116 80853
C 3509	50V 5% 4.7NF	5322 122 33536
C 3510	50V 5% 4.7NF	5322 122 33536
C 3511	50V 10% 22NF	5322 122 32654
C 3512	50V 10% 22NF	5322 122 32654
C 3513	50V 10% 22NF	5322 122 32654
C 3514	50V 10% 22NF	5322 122 32654
C 3515	50V 10% 22NF	5322 122 32654
C 3516	50V 10% 22NF	5322 122 32654
C 3517	50V 10% 22NF	5322 122 32654
C 3518	50V 10% 22NF	5322 122 32654
C 3519	50V 10% 22NF	5322 122 32654
C 3521	50V 10% 22NF	5322 122 32654
C 3522	50V 10% 22NF	5322 122 32654
C 3523	50V 10% 22NF	5322 122 32654
C 3524	50V 10% 22NF	5322 122 32654
C 3525	50V 10% 22NF	5322 122 32654
C 3526	50V 10% 22NF	5322 122 32654
C 3527	50V 10% 22NF	5322 122 32654
C 3528	50V 10% 22NF	5322 122 32654
C 3529	50V 10% 22NF	5322 122 32654
C 3531	50V 10% 22NF	5322 122 32654
C 3532	50V 10% 22NF	5322 122 32654
C 3533	50V 10% 22NF	5322 122 32654
C 3534	50V 10% 22NF	5322 122 32654
C 3535	2% 33PF	5322 122 32072
C 3536	50V 10% 22NF	5322 122 32654
C 3537	50V 10% 22NF	5322 122 32654
C 3538	50V 10% 22NF	5322 122 32654
C 3539	50V 5% 6.8PF	5322 122 32269
C 3540	0.25PF 1PF	4822 122 30104
C 3701	-10+50% 100UF	4822 124 20701
C 3702	-10+50% 150UF	4822 124 20691
C 3703	-10+50% 220UF	4822 124 20681
C 3704	-10+50% 150UF	4822 124 20691
C 3706	-10+50% 100UF	4822 124 20701
C 3707	-10+50% 10UF	4822 124 21129
C 3708	-10+50% 100UF	4822 124 20701
C 3709	-10+50% 100UF	4822 124 20701
C 3711	-10+50% 150UF	4822 124 20691
C 3712	-10+50% 150UF	4822 124 20691
C 3713	-10+50% 100UF	4822 124 20701
C 3714	-10+50% 100UF	4822 124 20701
C 3717	-10+50% 100UF	4822 124 20701
C 3718	-10+50% 150UF	4822 124 20691
C 3721	-10+50% 150UF	4822 124 20691
C 3722	-10+50% 100UF	4822 124 20701
C 3723	-10+50% 150UF	4822 124 20672
C 3724	-10+50% 150UF	4822 124 20672
C 3726	63V 10% 100NF	5322 121 42492
C 3727	63V 10% 100NF	5322 121 42492
C 3728	-10+50% 150UF	4822 124 20691
C 3729	-10+50% 150UF	4822 124 20672
C 3731	-10+50% 150UF	4822 124 20672
C 3732	63V 10% 100NF	5322 121 42492
C 3733	63V 10% 100NF	5322 121 42492
C 3734	-10+50% 100UF	4822 124 20701
C 3736	-10+50% 100UF	4822 124 20701
C 3737	0.25PF 2.7PF	4822 122 31038
C 4001	2% 100PF	4822 122 31316
C 4002	2% 100PF	4822 122 31316
C 4003	2% 100PF	4822 122 31316
C 4004	2% 100PF	4822 122 31316
C 4006	2% 100PF	4822 122 31316
C 4007	2% 100PF	4822 122 31316
C 4008	2% 100PF	4822 122 31316
C 4009	2% 100PF	4822 122 31316
C 4011	2% 100PF	4822 122 31316
C 4012	2% 100PF	4822 122 31316
C 4013	2% 100PF	4822 122 31316
C 4014	2% 100PF	4822 122 31316
C 4016	2% 100PF	4822 122 31316
C 4017	2% 100PF	4822 122 31316
C 4018	2% 100PF	4822 122 31316
C 4019	2% 100PF	4822 122 31316
C 4021	2% 100PF	4822 122 31316
C 4022	2% 100PF	4822 122 31316
C 4023	2% 100PF	4822 122 31316
C 4024	2% 100PF	4822 122 31316

POSNR	DESCRIPTION	ORDERING CODE
C 4026	2% 100PF	4822 122 31316
C 4027	2% 100PF	4822 122 31316
C 4028	-20+50% 10NF	4822 122 31414
C 4029	-20+50% 10NF	4822 122 31414
C 4031	-20+50% 10NF	4822 122 31414
C 4032	-10+50% 150UF	4822 124 20672
C 4033	-10+50% 150UF	4822 124 20672
C 4034	-10+50% 150UF	4822 124 20672
C 4036	-20+50% 10NF	4822 122 31414
C 4037	-20+50% 10NF	4822 122 31414
C 4038	-20+50% 10NF	4822 122 31414
C 4039	-20+50% 10NF	4822 122 31414
C 4041	-20+50% 10NF	4822 122 31414
C 4042	-20+50% 10NF	4822 122 31414
C 4043	-20+50% 10NF	4822 122 31414
C 4044	-20+50% 10NF	4822 122 31414
C 4046	-20+50% 10NF	4822 122 31414
C 4047	-20+50% 10NF	4822 122 31414
C 4048	-20+50% 10NF	4822 122 31414
C 4206	-10+50% 150UF	4822 124 20672
C 4207	-10+50% 150UF	4822 124 20672
C 4208	-20+50% 10NF	4822 122 31414
C 4209	-20+50% 10NF	4822 122 31414
C 4211	-20+50% 10NF	4822 122 31414
C 4212	-20+50% 10NF	4822 122 31414
C 4213	-20+50% 10NF	4822 122 31414
C 4214	-20+50% 10NF	4822 122 31414
C 4216	-20+50% 10NF	4822 122 31414
C 4217	-20+50% 10NF	4822 122 31414
C 4401	250V 10% 220NF	5322 121 44142
C 4402	ME275 20% 2.2NF	5322 121 42978
C 4403	-20+50% 10NF	4822 122 31414
C 4404	-20+50% 10NF	4822 122 31414
C 4405	100V 10% 47NF	5322 121 42491
C 4406	-20+50% 10NF	4822 122 31414
C 4407	ME275 20% 2.2NF	5322 121 42978
C 4408	63V 10% 470NF	5322 121 42979
C 4409	-20+50% 10NF	4822 122 31414
C 4411	63V 10% 100NF	5322 121 42492
C 4412	-20+50% 10NF	4822 122 31414
C 4413	-20+50% 10NF	4822 122 31414
C 4414	63V 10% 100NF	5322 121 42492
C 4416	-20+20% 330UF	5322 124 21472
C 4417	-20+20% 330UF	5322 124 21472
C 4418	-20+20% 150UF	4822 124 21695
C 4419	160V 1% 33NF	5322 121 50997
C 4422	2000V 5% 2.2NF	4822 121 41339
C 4423	63V 10% 100NF	5322 121 42492
C 4424	-10+50% 33UF	4822 124 20712
C 4427	2% 220PF	4822 122 30094
C 4428	-20+50% 10NF	4822 122 31414
C 4429	20% 6800UF	4822 124 40692
C 4430	100V 10% 22NF	5322 121 42496
C 4431	20% 6800UF	4822 124 40692
C 4432	20% 6800UF	4822 124 40692
C 4433	20% 6800UF	4822 124 40692
C 4434	-10+50% 680UF	4822 124 20685
C 4436	20% 6800UF	4822 124 40692
C 4437	-10+50% 680UF	4822 124 20685
C 4438	20% 6800UF	4822 124 40692
C 4439	-10+50% 680UF	4822 124 20685
C 4442	63V 10% 470NF	5322 121 42979
C 4443	-20+20% 10000UF	5322 124 21343
C 4446	-10+50% 470UF	4822 124 20695
C 4447	-20+20% 10000UF	5322 124 21343
C 4449	-10+50% 470UF	4822 124 20695
C 4451	-10+50% 330UF	4822 124 20705
C 4452	-10+50% 330UF	4822 124 20705
C 4453	-10+50% 330UF	4822 124 20705
C 4454	-10+50% 330UF	4822 124 20705
C 4456	-10+50% 22UF	5322 124 21768
C 4457	-10+50% 100UF	4822 124 20735
C 4458	-10+50% 22UF	4822 124 20731
C 4459	-10+50% 10UF	4822 124 21129
C 4461	-10+50% 100UF	4822 124 20679
C 4462	63V 10% 100NF	5322 121 42492
C 4471	10% 1NF	4822 122 30027
C 4472	63V 10% 680NF	5322 121 42494
C 4473	10% 1NF	4822 122 30027
C 4474	100V 10% 22NF	5322 121 42496
C 4476	2% 100PF	5322 122 32655
C 4477	2% 100PF	5322 122 32655
C 4478	2% 100PF	5322 122 32655
C 4479	-20+50% 1.5NF	5322 122 50092
C 4601	63V 10% 100NF	5322 121 42492
C 4602	-10+50% 68UF	4822 124 20689
C 4603	10% 4.7NF	4822 122 31125
C 4604	-10+10% 33PF	5322 122 33081
C 4606	100V 10% 47NF	5322 121 42491
C 4607	2% 47PF	4822 122 31072

POSNR	DESCRIPTION	ORDERING CODE
C 4608	63V 10% 100NF	5322 121 42492
C 4609	10% 4.7NF	4822 122 31125
C 4611	10% 1NF	4822 122 30027
C 4613	-10+50% 68UF	4822 124 20734
C 4614	-20+50% 10NF	5322 122 50091
C 4616	-20+50% 2.2NF	5322 122 50093
C 4616	-20+50% 2.2NF	5322 122 50093
C 4617	63V 10% 220NF	5322 121 42493
C 4618	-10+50% 10UF	4822 124 20742
C 4619	100V 10% 47NF	5322 121 42491
C 4621	-10+50% 33UF	4822 124 20712
C 4622	63V 10% 680NF	5322 121 42494
C 4623	10% 1NF	4822 122 30027
C 4624	-10+50% 150UF	4822 124 20716
C 4626	-10+50% 33UF	4822 124 20712
C 4627	-10+50% 33UF	4822 124 20712
C 4628	-10+50% 33UF	4822 124 20712
C 4629	-20+20% 2200UF	4822 124 21324
C 5001	63V 10% 100NF	5322 121 42492
C 5002	63V 10% 100NF	5322 121 42492
C 5003	63V 10% 100NF	5322 121 42492
C 5004	10% 4.7NF	4822 122 31125
C 5006	10% 4.7NF	4822 122 31125
C 5007	2% 150PF	4822 122 31413
C 5008	2% 33PF	5322 122 32072
C 5009	16V 20% 6.8UF	5322 124 21763
C 5011	0.25PF 1.2PF	5322 122 32312
C 5012	16V 20% 6.8UF	5322 124 21763
C 5013	2% 39PF	4822 122 31069
C 5015	16V 20% 6.8UF	5322 124 21763
C 5025	63V 10% 100NF	5322 121 42492
C 5027	63V 10% 100NF	5322 121 42492
C 5028	63V 10% 100NF	5322 121 42492
C 5029	63V 10% 100NF	5322 121 42492
C 5031	0.25PF 2.7PF	4822 122 31038
C 5032	2% 10PF	4822 122 32185
C 5033	0.25PF 4.7PF	4822 122 31822
C 5036	-20+50% 10NF	4822 122 31414
C 5037	-20+50% 10NF	4822 122 31414
C 5038	-20+50% 10NF	4822 122 31414
C 5041	-20+50% 10NF	4822 122 31414
C 5042	-20+50% 10NF	4822 122 31414
C 5043	63V 10% 100NF	5322 121 42492
C 5044	-20+50% 10NF	4822 122 31414
C 5046	2% 100PF	4822 122 31316
C 5047	100V 10% 22NF	5322 121 42496
C 5048	63V 10% 100NF	5322 121 42492
C 5049	16V 20% 6.8UF	5322 124 21763
C 5050	16V 20% 6.8UF	5322 124 21763
C 5052	2% 39PF	4822 122 31069
C 5053	63V 10% 100NF	5322 121 42492
C 5054	63V 10% 100NF	5322 121 42492
C 5055	16V 20% 6.8UF	5322 124 21763
C 5057	-20+50% 10NF	4822 122 31414
C 5058	-20+50% 10NF	4822 122 31414
C 5059	63V 10% 100NF	5322 121 42492
C 5061	-20+50% 10NF	4822 122 31414
C 5062	63V 10% 100NF	5322 121 42492
C 5063	16V 20% 6.8UF	5322 124 21763
C 5064	16V 20% 6.8UF	5322 124 21763
C 5066	63V 10% 100NF	5322 121 42492
C 5068	63V 10% 100NF	5322 121 42492
C 5069	10% 1NF	4822 122 30027
C 5071	10% 1NF	4822 122 30027
C 5072	10% 1NF	4822 122 30027
C 5073	10% 1NF	4822 122 30027
C 5074	10% 1NF	4822 122 30027
C 5081	63V 10% 100NF	5322 121 42492
C 5082	16V 20% 6.8UF	5322 124 21763
C 5083	16V 20% 6.8UF	5322 124 21763
C 5085	16V 20% 6.8UF	5322 124 21763
C 5086	16V 20% 6.8UF	5322 124 21763
C 5088	16V 20% 6.8UF	5322 124 21763
C 5089	16V 20% 6.8UF	5322 124 21763
C 5091	16V 20% 6.8UF	5322 124 21763
C 5095	16V 20% 6.8UF	5322 124 21763
C 5096	2% 22PF	5322 122 32143
C 5201	50V 5% 1NF	5322 122 32531
C 5202	50V 10% 22NF	5322 122 32654
C 5204	50V 10% 22NF	5322 122 32654
C 5206	50V 10% 22NF	5322 122 32654
C 5207	50V 10% 22NF	5322 122 32654
C 5208	50V 10% 22NF	5322 122 32654
C 5209	50V 10% 22NF	5322 122 32654
C 5211	50V 10% 22NF	5322 122 32654
C 5212	50V 5% 33PF	5322 122 32659
C 5213	50V 10% 22NF	5322 122 32654
C 5214	50V 5% 33PF	5322 122 32659
C 5216	50V 10% 22NF	5322 122 32654
C 5217	50V 10% 22NF	5322 122 32654

POSNR	DESCRIPTION	ORDERING CODE
C 5218	16V 20% 10UF	5322 124 41622
C 5219	50V 10% 22NF	5322 122 32654
C 5222	50V 10% 22NF	5322 122 32654
C 5223	50V 10% 100NF	4822 122 33156
C 5224	50V 10% 22NF	5322 122 32654
C 5226	50V 10% 22NF	5322 122 32654
C 5227	50V 10% 1.5NF	5322 122 31865
C 5228	50V 10% 22NF	5322 122 32654
C 5231	50V 10% 22NF	5322 122 32654
C 5232	50V 10% 22NF	5322 122 32654
C 5233	50V 10% 22NF	5322 122 32654
C 5234	50V 10% 22NF	5322 122 32654
C 5236	50V 5% 33PF	5322 122 32659
C 5237	50V 10% 22NF	5322 122 32654
C 5238	50V 10% 22NF	5322 122 32654
C 5239	50V 10% 22NF	5322 122 32654
C 5241	50V 10% 22NF	5322 122 32654
C 5242	50V 10% 22NF	5322 122 32654
C 5243	50V 10% 22NF	5322 122 32654
C 5244	50V 10% 22NF	5322 122 32654
C 5246	50V 10% 22NF	5322 122 32654
C 5247	50V 5% 33PF	5322 122 32659
C 5248	50V 5% 33PF	5322 122 32659
C [illegible]	50V 5% 33PF	5322 122 32659
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	50V 5% 27PF	5322 122 31946
C [illegible]	50V 5% 68PF	5322 122 32269
C [illegible]	50V 5% 68PF	5322 122 32269
C [illegible]	50V 5% 27PF	5322 122 31946
C [illegible]	50V 10% 100NF	4822 122 33156
C [illegible]	50V 5% 10PF	5322 122 32448
C [illegible]	50V 10% 100NF	4822 122 33156
C [illegible]	50V 5% 27PF	5322 122 31946
C [illegible]	50V 5% 68PF	5322 122 32269
C [illegible]	50V 5% 68PF	5322 122 32269
C [illegible]	50V 5% 27PF	5322 122 31946
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	16V 20% 10UF	5322 124 41622
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	50V 10% 22NF	5322 122 32654
C [illegible]	63V 10% 100NF	5322 121 42492
C [illegible]	63V 10% 100NF	5322 121 42492
C [illegible]	63V 10% 100NF	5322 121 42492
C 6004	10% 4.7NF	4822 122 31125
C 6006	10% 4.7NF	4822 122 31125
C 6007	2% 150PF	4822 122 31413
C 6008	2% 33PF	5322 122 32072
C 6009	16V 20% 6.8UF	5322 124 21763
C 6011	0.25PF 1.2PF	5322 122 32312
C 6012	16V 20% 6.8UF	5322 124 21763
C 6013	2% 39PF	4822 122 31069
C 6015	16V 20% 6.8UF	5322 124 21763
C 6025	63V 10% 100NF	5322 121 42492
C 6027	63V 10% 100NF	5322 121 42492
C 6028	63V 10% 100NF	5322 121 42492
C 6029	63V 10% 100NF	5322 121 42492
C 6031	0.25PF 2.7PF	4822 122 31038
C 6032	2% 10PF	4822 122 32185
C 6033	0.25PF 4.7PF	4822 122 31822
C 6036	-20+50% 10NF	4822 122 31414
C 6037	-20+50% 10NF	4822 122 31414
C 6038	-20+50% 10NF	4822 122 31414
C 6041	-20+50% 10NF	4822 122 31414
C 6042	-20+50% 10NF	4822 122 31414

POSNR	DESCRIPTION	ORDERING CODE
C 6043	63V 10% 100NF	5322 121 42492
C 6044	-20+50% 10NF	4822 122 31414
C 6046	2% 100PF	4822 122 31316
C 6047	100V 10% 22NF	5322 121 42496
C 6048	63V 10% 100NF	5322 121 42492
C 6049	16V 20% 6.8UF	5322 124 21763
C 6050	16V 20% 6.8UF	5322 124 21763
C 6052	2% 39PF	4822 122 31069
C 6053	63V 10% 100NF	5322 121 42492
C 6054	63V 10% 100NF	5322 121 42492
C 6055	16V 20% 6.8UF	5322 124 21763
C 6057	-20+50% 10NF	4822 122 31414
C 6058	-20+50% 10NF	4822 122 31414
C 6059	63V 10% 100NF	5322 121 42492
C 6061	-20+50% 10NF	4822 122 31414
C 6062	63V 10% 100NF	5322 121 42492
C 6066	63V 10% 100NF	5322 121 42492
C 6068	63V 10% 100NF	5322 121 42492
C 6069	10% 1NF	4822 122 30027
C 6071	10% 1NF	4822 122 30027
C 6072	10% 1NF	4822 122 30027
C 6073	10% 1NF	4822 122 30027
C 6074	10% 1NF	4822 122 30027
C 6081	63V 10% 100NF	5322 121 42492
C 6082	16V 20% 6.8UF	5322 124 21763
C 6083	16V 20% 6.8UF	5322 124 21763
C 6086	16V 20% 6.8UF	5322 124 21763
C 6088	16V 20% 6.8UF	5322 124 21763
C 6089	16V 20% 6.8UF	5322 124 21763
C 6091	16V 20% 6.8UF	5322 124 21763
C 6095	16V 20% 6.8UF	5322 124 21763
C 6096	2% 22PF	5322 122 32143
C 7001	16V 20% 6.8UF	5322 124 21763
C 7002	-20+50% 10NF	4822 122 31414
C 7003	2% 10PF	4822 122 32185
C 7004	63V 10% 100NF	5322 121 42492
C 7005	16V 20% 6.8UF	5322 124 21763
C 7007	2% 10PF	4822 122 32185
C 7008	63V 10% 100NF	5322 121 42492
C 7009	63V 10% 100NF	5322 121 42492
C 7010	63V 10% 100NF	5322 121 42492
C 7011	-10+50% 6.8UF	4822 124 20741
C 7012	400V 10% 22NF	5322 121 40308
C 7013	400V 10% 22NF	5322 121 40308
C 7014	-10+50% 47UF	4822 124 20699
C 7015	63V 10% 100NF	5322 121 42492
C 7016	63V 10% 100NF	5322 121 42492
C 7017	63V 10% 100NF	5322 121 42492
C 7018	-10+50% 6.8UF	4822 124 20741
C 7020	63V 10% 100NF	5322 121 42492
C 7021	2% 100PF	4822 122 31316
C 7022	2% 100PF	4822 122 31316
C 7023	10% 470PF	4822 122 30034
C 7024	10% 470PF	4822 122 30034
C 7026	-20+50% 10NF	4822 122 31414
C 7027	-20+50% 10NF	4822 122 31414
C 7028	-20+50% 10NF	4822 122 31414
C 7029	-20+50% 10NF	4822 122 31414

RESISTORS

R 0001	CPP12 20% 47K	5322 101 20945
R 0002	CPP12 20% 47K	5322 101 20946
R 0003	CPP12 20% 47K	5322 101 20945
R 0004	CPP12 20% 47K	5322 101 20946
R 0005	CPP12 20% 47K	5322 101 20945
R 0501	-104 330E/470E	5322 111 90836
R 0502	-104 330E/470E	5322 111 90836
R 0503	-104 330E/470E	5322 111 90836
R 0504	-104 330E/470E	5322 111 90836
R 0506	-104 330E/470E	5322 111 90836
R 0507	-104 330E/470E	5322 111 90836
R 0508	-104 330E/470E	5322 111 90836
R 0602	MRS25 1% 10K	4822 116 53022
R 0603	MRS25 1% 51E1	5322 116 53213
R 0604	MRS25 1% 51E1	5322 116 53213
R 0606	MRS25 1% 51E1	5322 116 53213
R 0607	MRS25 1% 10K	4822 116 53022
R 0608	MRS25 1% 51E1	5322 116 53213
R 0609	MRS25 1% 51E1	5322 116 53213
R 0611	MRS25 1% 100E	5322 116 53126
R 0612	MRS25 1% 100E	5322 116 53126
R 0613	MRS25 1% 51E1	5322 116 53213
R 0614	MRS25 1% 51E1	5322 116 53213
R 0616	MRS25 1% 100E	5322 116 53126
R 0617	MRS25 1% 100E	5322 116 53126
R 0618	MRS25 1% 10E	4822 116 52891

POSNR	DESCRIPTION	ORDERING CODE
R 0619	MRS25 1% 51E1	5322 116 53213
R 0621	MRS25 1% 5K11	5322 116 53494
R 0622	MRS25 1% 10K	4822 116 53022
R 0623	MRS25 1% 10K	4822 116 53022
R 0624	MRS25 1% 1K	4822 116 53108
R 0626	MRS25 1% 2K37	5322 116 53536
R 0627	MRS25 1% 51E1	5322 116 53213
R 0628	MRS25 1% 619E	5322 116 53337
R 0629	MRS25 1% 215E	5322 116 53325
R 0631	MRS25 1% 1K1	5322 116 53473
R 0632	MRS25 1% 51E1	5322 116 53213
R 0633	MRS25 1% 162E	5322 116 53523
R 0634	MRS25 1% 825E	5322 116 53541
R 0635	MRS25 1% 51E1	5322 116 53213
R 0636	MRS25 1% 5K11	5322 116 53494
R 0637	MRS25 1% 7K5	4822 116 53028
R 0638	MRS25 1% 5E11	4822 116 52999
R 0639	MRS25 1% 8K25	5322 116 53267
R 0640	MRS25 1% 51E1	5322 116 53213
R 0641	MRS25 1% 51E1	5322 116 53213
R 0642	MRS25 1% 1K47	5322 116 53185
R 0643	MRS25 1% 51E1	5322 116 53213
R 0644	MRS25 1% 511E	5322 116 53135
R 0646	MRS25 1% 196E	5322 116 53492
R 0647	MRS25 1% 51E1	5322 116 53213
R 0648	MRS25 1% 51E1	5322 116 53213
R 0649	MRS25 1% 619E	5322 116 53337
R 0651	MRS25 1% 619E	5322 116 53337
R 0652	MRS25 1% 100E	5322 116 53126
R 0653	MRS25 1% 100E	5322 116 53126
R 0654	MRS25 1% 100E	5322 116 53126
R 0657	MRS25 1% 10E	4822 116 52891
R 0658	MRS25 1% 121E	4822 116 52955
R 0659	MRS25 1% 100E	5322 116 53126
R 0661	NFR25 5% 1E	4822 111 30483
R 0662	NFR25 5% 1E	4822 111 30483
R 0663	NFR25 5% 1E	4822 111 30483
R 0664	NFR25 5% 1E	4822 111 30483
R 0666	NFR25 5% 1E	4822 111 30483
R 0667	NFR25 5% 1E	4822 111 30483
R 0668	MRS25 1% 10K	4822 116 53022
R 0669	MRS25 1% 10K	4822 116 53022
R 0671	MRS25 1% 10K	4822 116 53022
R 0672	MRS25 1% 10K	4822 116 53022
R 0673	MRS25 1% 10K	4822 116 53022
R 0674	MRS25 1% 1K	4822 116 53108
R 0676	MRS25 1% 1K	4822 116 53108
R 0677	MRS25 1% 5K11	5322 116 53494
R 0681	MRS25 1% 1K62	5322 116 53257
R 0682	MRS25 1% 6K81	5322 116 53252
R 0683	MRS25 1% 750E	5322 116 53265
R 0684	MRS25 1% 7K5	4822 116 53028
R 0686	MRS25 1% 237E	5322 116 53259
R 0687	MRS25 1% 1K47	5322 116 53185
R 0688	MRS25 1% 1K47	5322 116 53185
R 0689	MRS25 1% 261E	5322 116 53549
R 0691	MRS25 1% 14K7	4822 116 53531
R 0692	MRS25 1% 3K48	4822 116 53315
R 0693	MRS25 1% 3K48	4822 116 53315
R 0694	MRS25 1% 14K7	4822 116 53531
R 0696	MRS25 1% 7K5	4822 116 53028
R 0697	MRS25 1% 2K37	5322 116 53536
R 0698	MRS25 1% 1K21	4822 116 52956
R 0699	MRS25 1% 1K21	4822 116 52956
R 0701	MRS25 1% 237E	5322 116 53259
R 0702	MRS25 1% 348E	5322 116 53591
R 0703	MRS25 1% 237E	5322 116 53259
R 0704	MRS25 1% 5E11	4822 116 52999
R 0706	MRS25 1% 4K64	5322 116 53212
R 0707	MRS25 1% 23E7	5322 116 53606
R 0708	MRS25 1% 3K48	4822 116 53315
R 0709	MRS25 1% 750E	5322 116 53265
R 0711	MRS25 1% 237E	5322 116 53259
R 0712	MRS25 1% 2K87	5322 116 53513
R 0713	MRS25 1% 2K87	5322 116 53513
R 0714	MRS25 1% 1K21	4822 116 52956
R 0716	MRS25 1% 1K21	4822 116 52956
R 0717	MRS25 1% 23E7	5322 116 53606
R 0718	MRS25 1% 1K21	4822 116 52956
R 0719	MRS25 1% 1K21	4822 116 52956
R 0721	MTP10 20% 4K7	5322 101 14067
R 0722	MRS25 1% 5E11	4822 116 52999
R 0723	MRS25 1% 5K11	5322 116 53494
R 0724	MRS25 1% 10K	4822 116 53022
R 0726	MRS25 1% 2K15	5322 116 53239
R 0727	MRS25 1% 10K	4822 116 53022
R 0728	MRS25 1% 10K	4822 116 53022
R 0729	MRS25 1% 4K22	5322 116 53246
R 0751	MRS25 1% 46E4	5322 116 53248
R 0901	MCR18 1% 110E	4822 111 90335

POSNR	DESCRIPTION	ORDERING CODE
R 0902	MCR18 1% 39E	4822 111 90361
R 0904	MCR18 1% 110E	4822 111 90335
R 0906	MCR18 1% 100E	5322 111 91134
R 0907	MCR18 1% 51E	5322 111 91352
R 0908	MCR18 1% 5K6	4822 111 90572
R 0909	MCR18 1% 5K6	4822 111 90572
R 0911	MCR18 1% 5K6	4822 111 90572
R 0912	MCR18 1% 68E	4822 111 90203
R 0913	MRS25 1% 100E	5322 116 53126
R 0914	MCR18 1% 68E	4822 111 90203
R 0916	MRS25 1% 100E	5322 116 53126
R 0917	MCR18 1% 220E	4822 111 90178
R 0918	MCR18 1% 220E	4822 111 90178
R 0919	MCR18 1% 5K6	4822 111 90572
R 0921	MCR18 1% 5K6	4822 111 90572
R 0922	MCR18 1% 68E	4822 111 90203
R 0923	MRS25 1% 100E	5322 116 53126
R 0924	MCR18 1% 68E	4822 111 90203
R 0926	MRS25 1% 100E	5322 116 53126
R 0927	MCR18 1% 220E	4822 111 90178
R 0928	MCR18 1% 220E	4822 111 90178
R 0929	MCR18 1% 110E	4822 111 90335
R 0931	MCR18 1% 100E	5322 111 91134
R 0932	MCR18 1% 110E	4822 111 90335
R 0933	MCR18 1% 39E	4822 111 90361
R 0936	MCR18 1% 22K	5322 111 91349
R 0937	MCR18 1% 100E	5322 111 91134
R 0938	MCR18 1% 22K	5322 111 91349
R 0939	MCR18 1% 100E	5322 111 91134
R 1201	MRS25 1% 464E	5322 116 53232
R 1202	MRS25 1% 464E	5322 116 53232
R 1203	MRS25 1% 5K11	5322 116 53494
R 1204	MRS25 1% 5K11	5322 116 53494
R 1206	MRS25 1% 5K11	5322 116 53494
R 1207	MRS25 1% 464E	5322 116 53232
R 1208	MRS25 1% 464E	5322 116 53232
R 1209	MRS25 1% 5K11	5322 116 53494
R 1211	MRS25 1% 464E	5322 116 53232
R 1212	MRS25 1% 464E	5322 116 53232
R 1213	MRS25 1% 464E	5322 116 53232
R 1214	MRS25 1% 51E1	5322 116 53213
R 1216	MRS25 1% 51E1	5322 116 53213
R 1217	MRS25 1% 51E1	5322 116 53213
R 1218	MRS25 1% 51E1	5322 116 53213
R 1219	MRS25 1% 51E1	5322 116 53213
R 1301	MCR18 1% 100E	5322 111 91134
R 1302	MCR18 1% 100E	5322 111 91134
R 1303	MCR18 1% 100E	5322 111 91134
R 1304	MCR18 1% 100E	5322 111 91134
R 1306	MCR18 1% 510E	4822 111 90245
R 1307	MCR18 1% 510E	4822 111 90245
R 1308	MCR18 1% 510E	4822 111 90245
R 1309	MCR18 1% 510E	4822 111 90245
R 1311	MCR18 1% 680E	4822 111 90162
R 1312	MCR18 1% 680E	4822 111 90162
R 1313	MCR18 1% 680E	4822 111 90162
R 1314	MCR18 1% 200E	5322 116 80599
R 1316	MCR18 1% 200E	5322 116 80599
R 1317	MCR18 1% 200E	5322 116 80599
R 1318	MCR18 1% 200E	5322 116 80599
R 1319	MCR18 1% 20E	4822 111 90352
R 1321	MCR18 1% 20E	4822 111 90352
R 1322	MCR18 1% 510E	4822 111 90245
R 1323	MCR18 1% 510E	4822 111 90245
R 1324	MCR18 1% 510E	4822 111 90245
R 1326	MCR18 1% 510E	4822 111 90245
R 1327	MCR18 1% 680E	4822 111 90162
R 1328	MCR18 1% 680E	4822 111 90162
R 1329	MCR18 1% 680E	4822 111 90162
R 1331	MCR18 1% 20E	4822 111 90352
R 1332	MCR18 1% 20E	4822 111 90352
R 1333	MCR18 1% 510E	4822 111 90245
R 1334	MCR18 1% 510E	4822 111 90245
R 1336	MCR18 1% 510E	4822 111 90245
R 1337	MCR18 1% 510E	4822 111 90245
R 1338	MCR18 1% 680E	4822 111 90162
R 1339	MCR18 1% 680E	4822 111 90162
R 1341	MCR18 1% 680E	4822 111 90162
R 1342	MCR18 1% 100E	5322 111 91134
R 1343	MCR18 1% 100E	5322 111 91134
R 1344	MCR18 1% 20E	4822 111 90352
R 1346	MCR18 1% 20E	4822 111 90352
R 1348	MCR18 1% 1K	5322 111 90092
R 1349	MCR18 1% 150E	5322 111 90098
R 1351	MCR18 1% 10K	4822 111 90249
R 1352	MCR18 1% 22E	4822 111 90186
R 1353	MCR18 1% 2K2	4822 111 90248
R 1354	MCR18 1% 51E	5322 111 91352
R 1356	MCR18 1% 100K	4822 111 90214
R 1357	MCR18 1% 3K3	4822 111 90157

POSNR	DESCRIPTION	ORDERING CODE
R 1358	MCR18 1% 100E	5322 111 91134
R 1359	MCR18 1% 10K	4822 111 90249
R 1361	0.3W 25% 1K	5322 105 20032
R 1362	MCR18 1% 1K	5322 111 90092
R 1363	MCR18 1% 100K	4822 111 90214
R 1364	MCR18 1% 10K	4822 111 90249
R 1366	MCR18 1% 1K	5322 111 90092
R 1367	MCR18 1% 1K	5322 111 90092
R 1368	MCR18 1% 5K1	5322 111 91471
R 1369	MCR18 1% 5K1	5322 111 91471
R 1401	MRS25 1% 10K	4822 116 53022
R 1402	MRS25 1% 5K11	5322 116 53494
R 1403	MRS25 1% 5K11	5322 116 53494
R 1404	MRS25 1% 5K11	5322 116 53494
R 1406	MRS25 1% 464E	5322 116 53232
R 1407	MRS25 1% 464E	5322 116 53232
R 1408	MRS25 1% 464E	5322 116 53232
R 1409	MRS25 1% 464E	5322 116 53232
R 1411	MRS25 1% 1K	4822 116 53108
R 1412	MRS25 1% 10K	4822 116 53022
R 1413	MRS25 1% 1K	4822 116 53108
R 1414	MRS25 1% 1K	4822 116 53108
R 1416	MRS25 1% 75E	5322 116 53339
R 1701	-105-472 4K7	5322 111 90474
R 1702	MRS25 1% 100K	4822 116 52973
R 1703	MRS25 1% 10K	4822 116 53022
R 1704	MRS25 1% 100K	4822 116 52973
R 1706	MRS25 1% 10K	4822 116 53022
R 1707	MRS25 1% 5K11	5322 116 53494
R 1708	MRS25 1% 5K11	5322 116 53494
R 1709	MRS25 1% 511E	5322 116 53135
R 1711	MRS25 1% 10K	4822 116 53022
R 1712	MRS25 1% 2K15	5322 116 53239
R 1713	MRS25 1% 562E	5322 116 53214
R 1714	MRS25 1% 100E	5322 116 53126
R 1716	MRS25 1% 10K	4822 116 53022
R 1717	MRS25 1% 100E	5322 116 53126
R 1718	MRS25 1% 562E	5322 116 53214
R 1719	MRS25 1% 147E	5322 116 53569
R 1723	-105-472 4K7	5322 111 90474
R 1724	-105-472 4K7	5322 111 90474
R 1726	-105-222 2K2	5322 111 90826
R 1727	MRS25 1% 10K	4822 116 53022
R 1728	MRS25 1% 511E	5322 116 53135
R 1731	MRS25 1% 511E	5322 116 53135
R 1732	MRS25 1% 511E	5322 116 53135
R 1733	MRS25 1% 511E	5322 116 53135
R 1741	MRS25 1% 562E	5322 116 53214
R 1742	MRS25 1% 909E	4822 116 53533
R 1743	MRS25 1% 562E	5322 116 53214
R 1744	MRS25 1% 909E	4822 116 53533
R 1746	MRS25 1% 562E	5322 116 53214
R 1747	MRS25 1% 909E	4822 116 53533
R 1772	NFR25 5% 1E	4822 111 30483
R 1773	NFR25 5% 1E	4822 111 30483
R 1779	MRS25 1% 10K	4822 116 53022
R 1781	MRS25 1% 1K	4822 116 53108
R 1782	MRS25 1% 1K	4822 116 53108
R 1783	MRS25 1% 1K	4822 116 53108
R 1791	MRS25 1% 10K	4822 116 53022
R 1792	MRS25 1% 1K	4822 116 53108
R 1801	MRS25 1% 511E	5322 116 53135
R 1802	MRS25 1% 1K	4822 116 53108
R 1803	MRS25 1% 1K	4822 116 53108
R 1804	MRS25 1% 464E	5322 116 53232
R 1808	MRS25 1% 1E	4822 116 52976
R 1809	MRS25 1% 1E	4822 116 52976
R 1811	MRS25 1% 5K11	5322 116 53494
R 1813	MRS25 1% 51E1	5322 116 53213
R 1816	MRS25 1% 1E	4822 116 52976
R 1817	MRS25 1% 5K11	5322 116 53494
R 1819	MRS25 1% 1K	4822 116 53108
R 1821	MRS25 1% 10K	4822 116 53022
R 1822	MRS25 1% 5K11	5322 116 53494
R 1823	MRS25 1% 5K11	5322 116 53494
R 1826	MRS25 1% 6K19	5322 116 53263
R 1827	MRS25 1% 100K	4822 116 52973
R 1831	MRS25 1% 10K	4822 116 53022
R 1832	MRS25 1% 10K	4822 116 53022
R 1833	MRS25 1% 1K	4822 116 53108
R 1834	MRS25 1% 1E	4822 116 52976
R 1836	MRS25 1% 1E	4822 116 52976
R 1839	MRS25 1% 1K	4822 116 53108
R 1841	MRS25 1% 5K11	5322 116 53494
R 1842	MRS25 1% 1K	4822 116 53108
R 1843	MRS25 1% 511E	5322 116 53135
R 1844	MRS25 1% 13K3	5322 116 53489
R 1851	MRS25 1% 5K11	5322 116 53494
R 1899	MRS25 1% 511E	5322 116 53135
R 2001	MRS25 1% 10K	4822 116 53022

POSNR	DESCRIPTION	ORDERING CODE
R 2002	MRS25 1% 10K	4822 116 53022
R 2003	MRS25 1% 511E	5322 116 53135
R 2004	MRS25 1% 511E	5322 116 53135
R 2006	MRS25 1% 511E	5322 116 53135
R 2007	MRS25 1% 10K	4822 116 53022
R 2008	MRS25 1% 10K	4822 116 53022
R 2009	MRS25 1% 10K	4822 116 53022
R 2011	MRS25 1% 10K	4822 116 53022
R 2012	MRS25 1% 1E	4822 116 52976
R 2013	MRS25 1% 1E	4822 116 52976
R 2014	MRS25 1% 10K	4822 116 53022
R 2016	MRS25 1% 511E	5322 116 53135
R 2017	MRS25 1% 10K	4822 116 53022
R 2018	MRS25 1% 511E	5322 116 53135
R 2019	NFR25 5% 1E	4822 111 30483
R 2021	NFR25 5% 1E	4822 111 30483
R 2022	NFR25 5% 1E	4822 111 30483
R 2023	NFR25 5% 1E	4822 111 30483
R 2024	NFR25 5% 1E	4822 111 30483
R 2026	MRS25 1% 511E	5322 116 53135
R 2027	MRS25 1% 1K	4822 116 53108
R 2028	MRS25 1% 1K	4822 116 53108
R 2029	MRS25 1% 1K	4822 116 53108
R 2031	MRS25 1% 1K	4822 116 53108
R 2032	MRS25 1% 10K	4822 116 53022
R 2033	MRS25 1% 10K	4822 116 53022
R 2034	MRS25 1% 1K	4822 116 53108
R 2036	MRS25 1% 10K	4822 116 53022
R 2037	MRS25 1% 10K	4822 116 53022
R 2038	MRS25 1% 1K	4822 116 53108
R 2101	MRS25 1% 10K	4822 116 53022
R 2102	MRS25 1% 10K	4822 116 53022
R 2103	MRS25 1% 511E	5322 116 53135
R 2104	MRS25 1% 511E	5322 116 53135
R 2106	MRS25 1% 511E	5322 116 53135
R 2107	MRS25 1% 10K	4822 116 53022
R 2108	MRS25 1% 10K	4822 116 53022
R 2109	MRS25 1% 511E	5322 116 53135
R 2111	MRS25 1% 511E	5322 116 53135
R 2112	MRS25 1% 511E	5322 116 53135
R 2113	MRS25 1% 511E	5322 116 53135
R 2114	MRS25 1% 5K11	5322 116 53494
R 2116	MRS25 1% 5K11	5322 116 53494
R 2117	MRS25 1% 21K5	5322 116 53241
R 2118	MRS25 1% 10K	4822 116 53022
R 2119	MRS25 1% 10K	4822 116 53022
R 2120	MRS25 1% 10K	4822 116 53022
R 2121	MRS25 1% 511E	5322 116 53135
R 2123	MRS25 1% 10K	4822 116 53022
R 2124	MRS25 1% 5K11	5322 116 53494
R 2126	MRS25 1% 10K	4822 116 53022
R 2127	MRS25 1% 10K	4822 116 53022
R 2128	MRS25 1% 511E	5322 116 53135
R 2129	MRS25 1% 10K	4822 116 53022
R 2131	MRS25 1% 10K	4822 116 53022
R 2132	MRS25 1% 10K	4822 116 53022
R 2133	MRS25 1% 1K	4822 116 53108
R 2134	NFR25 5% 1E	4822 111 30483
R 2136	NFR25 5% 1E	4822 111 30483
R 2137	NFR25 5% 1E	4822 111 30483
R 2138	NFR25 5% 1E	4822 111 30483
R 2139	NFR25 5% 1E	4822 111 30483
R 2141	NFR25 5% 1E	4822 111 30483
R 2142	MRS25 1% 1K	4822 116 53108
R 2201	MRS25 1% 10K	4822 116 53022
R 2202	MRS25 1% 10K	4822 116 53022
R 2203	MRS25 1% 316K	4822 116 53058
R 2204	MRS25 1% 1K	4822 116 53108
R 2206	MRS25 1% 316K	4822 116 53058
R 2207	MRS25 1% 1K	4822 116 53108
R 2208	MRS25 1% 10K	4822 116 53022
R 2209	MRS25 1% 100K	4822 116 52973
R 2211	MRS25 1% 100K	4822 116 52973
R 2212	MRS25 1% 3K48	4822 116 53315
R 2213	MRS25 1% 100K	4822 116 52973
R 2214	MRS25 1% 100K	4822 116 52973
R 2216	MRS25 1% 21K5	5322 116 53241
R 2217	MRS25 1% 1M	4822 116 52843
R 2218	MRS25 1% 10K	4822 116 53022
R 2219	MRS25 1% 237E	5322 116 53259
R 2220	0.3W 25% 1K	5322 105 20032
R 2221	MRS25 1% 1K33	5322 116 53512
R 2222	MRS25 1% 237E	5322 116 53259
R 2223	MRS25 1% 1K62	5322 116 53257
R 2224	MRS25 1% 1E	4822 116 52976
R 2225	0.3W 25% 4K7	5322 105 20034
R 2226	MRS25 1% 1E	4822 116 52976
R 2227	MRS25 1% 1E	4822 116 52976
R 2228	MRS25 1% 1E	4822 116 52976
R 2229	MRS25 1% 2K15	5322 116 53239

POSNR	DESCRIPTION	ORDERING CODE
R 2231	MRS25 1% 1K21	4822 116 52956
R 2232	0.3W 25% 470E	5322 105 20028
R 2233	MRS25 1% 196K	5322 116 53661
R 2234	MRS25 1% 196K	5322 116 53661
R 2236	MRS25 1% 1K	4822 116 53108
R 2237	MRS25 1% 5K11	5322 116 53494
R 2301	MRS25 1% 10K	4822 116 53022
R 2302	MRS25 1% 10K	4822 116 53022
R 2303	MRS25 1% 511E	5322 116 53135
R 2304	MRS25 1% 511E	5322 116 53135
R 2305	MRS25 1% 100E	5322 116 53126
R 2306	MRS25 1% 511E	5322 116 53135
R 2307	MRS25 1% 511E	5322 116 53135
R 2308	MRS25 1% 511E	5322 116 53135
R 2309	MRS25 1% 511E	5322 116 53135
R 2310	MRS25 1% 100E	5322 116 53126
R 2311	MRS25 1% 10K	4822 116 53022
R 2312	MRS25 1% 10K	4822 116 53022
R 2313	MRS25 1% 511E	5322 116 53135
R 2314	MRS25 1% 511E	5322 116 53135
R 2316	MRS25 1% 5K11	5322 116 53494
R 2317	MRS25 1% 2K61	5322 116 53327
R 2318	MRS25 1% 2K37	5322 116 53536
R 2319	MRS25 1% 5K11	5322 116 53494
R 2321	MRS25 1% 2K61	5322 116 53327
R 2322	MRS25 1% 2K37	5322 116 53536
R 2323	MRS25 1% 5K11	5322 116 53494
R 2324	MRS25 1% 2K37	5322 116 53536
R 2326	MRS25 1% 2K61	5322 116 53327
R 2327	NFR25 5% 1E	4822 111 30483
R 2328	MRS25 1% 750E	5322 116 53265
R 2329	MRS25 1% 750E	5322 116 53265
R 2331	NFR25 5% 1E	4822 111 30483
R 2332	NFR25 5% 1E	4822 111 30483
R 2333	MRS25 1% 7K5	4822 116 53028
R 2334	MTP10 20% 22K	5322 100 10118
R 2336	MRS25 1% 7K5	4822 116 53028
R 2337	MRS25 1% 100K	4822 116 52973
R 2338	MRS25 1% 562E	5322 116 53214
R 2339	MRS25 1% 1K	4822 116 53108
R 2341	MRS25 1% 1K	4822 116 53108
R 2342	MRS25 1% 562E	5322 116 53214
R 2343	MRS25 1% 562E	5322 116 53214
R 2344	MRS25 1% 562E	5322 116 53214
R 2346	MRS25 1% 215E	5322 116 53325
R 2349	MRS25 1% 215E	5322 116 53325
R 2351	MRS25 1% 2K61	5322 116 53327
R 2352	MRS25 1% 750E	5322 116 53265
R 2353	MRS25 1% 2K61	5322 116 53327
R 2354	MRS25 1% 750E	5322 116 53265
R 2356	MRS25 1% 261E	5322 116 53549
R 2357	MRS25 1% 511E	5322 116 53135
R 2366	MRS25 1% 261E	5322 116 53549
R 2367	MRS25 1% 511E	5322 116 53135
R 2368	MRS25 1% 1K78	5322 116 53208
R 2369	MRS25 1% 6K19	5322 116 53263
R 2374	MRS25 1% 3K48	4822 116 53315
R 2376	MRS25 1% 7K5	4822 116 53028
R 2377	MTP10 20% 22K	5322 100 10118
R 2378	MRS25 1% 7K5	4822 116 53028
R 2379	NFR25 5% 1E	4822 111 30483
R 2381	MRS25 1% 619E	5322 116 53337
R 2382	MRS25 1% 2K61	5322 116 53327
R 2383	MRS25 1% 2K61	5322 116 53327
R 2384	MRS25 1% 619E	5322 116 53337
R 2386	MRS25 1% 619E	5322 116 53337
R 2387	MRS25 1% 619E	5322 116 53337
R 2388	MRS25 1% 249E	5322 116 53573
R 2392	MRS25 1% 249E	5322 116 53573
R 2399	MRS25 1% 2K61	5322 116 53327
R 2401	MRS25 1% 750E	5322 116 53265
R 2402	MRS25 1% 2K61	5322 116 53327
R 2403	MRS25 1% 750E	5322 116 53265
R 2404	MRS25 1% 261E	5322 116 53549
R 2406	MRS25 1% 511E	5322 116 53135
R 2407	MRS25 1% 2K15	5322 116 53239
R 2408	MRS25 1% 464E	5322 116 53232
R 2409	MRS25 1% 121E	4822 116 52955
R 2411	MRS25 1% 2K15	5322 116 53239
R 2412	MRS25 1% 464E	5322 116 53232
R 2413	MRS25 1% 121E	4822 116 52955
R 2414	MRS25 1% 100K	4822 116 52973
R 2416	MRS25 1% 261E	5322 116 53549
R 2417	MRS25 1% 511E	5322 116 53135
R 2421	NFR25 5% 1E	4822 111 30483
R 2422	NFR25 5% 1E	4822 111 30483
R 2424	NFR25 5% 1E	4822 111 30483
R 2426	MRS25 1% 562E	5322 116 53214
R 2451	NFR25 5% 1E	4822 111 30483
R 2452	NFR25 5% 1E	4822 111 30483

POSNR	DESCRIPTION			ORDERING CODE
R 2453	NFR25	5%	1E	4822 111 30483
R 2454	NFR25	5%	1E	4822 111 30483
R 2456	NFR25	5%	1E	4822 111 30483
R 2500	MRS25	1%	10K	4822 116 53022
R 2502	MRS25	1%	1K	4822 116 53108
R 2503	MRS25	1%	100E	5322 116 53126
R 2504	MRS25	1%	3K83	4822 116 53079
R 2506	MRS25	1%	3K83	4822 116 53079
R 2507	MRS25	1%	3K83	4822 116 53079
R 2508	MRS25	1%	100E	5322 116 53126
R 2512	MRS25	1%	38K3	4822 116 53526
R 2513	MTP10	20%	47K	5322 101 14293
R 2514	MRS25	1%	38K3	4822 116 53526
R 2516	MTP10	20%	47K	5322 101 14293
R 2517	MRS25	1%	6K19	5322 116 53263
R 2518	MRS25	1%	100E	5322 116 53126
R 2519	MRS25	1%	100E	5322 116 53126
R 2521	MRS25	1%	287K	4822 116 53119
R 2522	MRS25	1%	287K	4822 116 53119
R 2523	MRS25	1%	42K2	5322 116 53431
R 2524	MRS25	1%	10K	4822 116 53022
R 2526	MRS25	1%	511E	5322 116 53135
R 2527	MRS25	1%	511E	5322 116 53135
R 2528	MRS25	1%	511E	5322 116 53135
R 2529	MRS25	1%	750E	5322 116 53265
R 2531	MTP10	20%	1K	5322 101 10294
R 2532	MRS25	1%	31K6	5322 116 53262
R 2533	MTP10	20%	1K	5322 101 10294
R 2534	MRS25	1%	1K62	5322 116 53257
R 2535	MRS25	1%	1K62	5322 116 53257
R 2536	MRS25	1%	1K78	5322 116 53208
R 2537	MRS25	1%	5K62	5322 116 53495
R 2538	MRS25	1%	3K48	4822 116 53315
R 2539	MRS25	1%	196E	5322 116 53492
R 2541	MRS25	1%	5K62	5322 116 53495
R 2542	MRS25	1%	3K48	4822 116 53315
R 2543	MRS25	1%	196E	5322 116 53492
R 2544	MRS25	1%	5K62	5322 116 53495
R 2546	MRS25	1%	1M	4822 116 52843
R 2547	MRS25	1%	162K	5322 116 53535
R 2548	MRS25	1%	1M	4822 116 52843
R 2549	MRS25	1%	5K62	5322 116 53495
R 2550	MRS25	1%	422E	5322 116 53592
R 2551	MRS25	1%	422E	5322 116 53592
R 2552	MRS25	1%	100E	5322 116 53126
R 2553	MRS25	1%	100E	5322 116 53126
R 2554	MRS25	1%	5K62	5322 116 53495
R 2555	MRS25	1%	100E	5322 116 53126
R 2556	MRS25	1%	287K	4822 116 53119
R 2557	MRS25	1%	287K	4822 116 53119
R 2558	MRS25	1%	42K2	5322 116 53431
R 2559	MRS25	1%	12K1	4822 116 52957
R 2560	MRS25	1%	100E	5322 116 53126
R 2561	MRS25	1%	383E	5322 116 53332
R 2562	MRS25	1%	215E	5322 116 53325
R 2563	MRS25	1%	215E	5322 116 53325
R 2564	MRS25	1%	511E	5322 116 53135
R 2565	MRS25	1%	31K6	5322 116 53262
R 2566	MTP10	20%	1K	5322 101 10294
R 2567	MRS25	1%	196E	5322 116 53492
R 2568	MRS25	1%	196E	5322 116 53492
R 2569	MRS25	1%	31K6	5322 116 53262
R 2570	MRS25	1%	4K64	5322 116 53212
R 2571	MTP10	20%	4K7	5322 101 14067
R 2572	MRS25	1%	2K61	5322 116 53327
R 2573	MRS25	1%	10K	4822 116 53022
R 2574	MRS25	1%	1K	4822 116 53108
R 2576	MRS25	1%	12K1	4822 116 52957
R 2577	MRS25	1%	681E	4822 116 53123
R 2578	MRS25	1%	1K33	5322 116 53512
R 2579	MRS25	1%	12K1	4822 116 52957
R 2581	MRS25	1%	681E	4822 116 53123
R 2582	MRS25	1%	28K7	4822 116 53215
R 2583	MRS25	1%	1M	4822 116 52843
R 2584	MRS25	1%	64K9	5322 116 50514
R 2586	MRS25	1%	1M	4822 116 52843
R 2587	MRS25	1%	28K7	4822 116 53215
R 2588	MRS25	1%	422E	5322 116 53592
R 2589	MRS25	1%	422E	5322 116 53592
R 2590	MRS25	1%	100E	5322 116 53126
R 2591	MRS25	1%	5E11	4822 116 52999
R 2592	MRS25	1%	1E	4822 116 52976
R 2593	MRS25	1%	5E11	4822 116 52999
R 2594	MRS25	1%	1E	4822 116 52976
R 2595	MRS25	1%	100E	5322 116 53126
R 2596	MRS25	1%	1E	4822 116 52976
R 2597	MRS25	1%	1E	4822 116 52976
R 2598	MRS25	1%	1E	4822 116 52976
R 2599	MRS25	1%	5E11	4822 116 52999
R 2601	MRS25	1%	1M	4822 116 52843

POSNR	DESCRIPTION			ORDERING CODE
R 2602	MRS25	1%	1M	4822 116 52843
R 2603	MRS25	1%	10K	4822 116 53022
R 2604	MRS25	1%	1M	4822 116 52843
R 2607	MRS25	1%	681K	5322 116 53593
R 2608	MRS25	1%	56K2	5322 116 53222
R 2609	MTP10	20%	10K	5322 101 14066
R 2611	MRS25	1%	4K22	5322 116 53246
R 2612	MRS25	1%	75K	5322 116 53266
R 2613	MRS25	1%	21K5	5322 116 53241
R 2614	MRS25	1%	90K9	5322 116 53582
R 2616	MRS25	1%	3K48	4822 116 53315
R 2617	MRS25	1%	287E	5322 116 53221
R 2621	MRS25	1%	2K15	5322 116 53239
R 2622	MRS25	1%	909E	4822 116 53533
R 2623	MRS25	1%	4K64	5322 116 53212
R 2624	MRS25	1%	2K87	5322 116 53513
R 2626	MRS25	1%	1K	4822 116 53108
R 2627	MRS25	1%	147E	5322 116 53569
R 2628	MRS25	1%	1K	4822 116 53108
R 2636	MRS25	1%	21K5	5322 116 53241
R 2637	MTP10	20%	22K	5322 100 10118
R 2638	MRS25	1%	23K7	5322 116 53537
R 2639	MRS25	1%	3K48	4822 116 53315
R 2641	MRS25	1%	23K7	5322 116 53537
R 2642	MRS25	1%	750E	5322 116 53265
R 2643	MRS25	1%	100K	4822 116 52973
R 2644	MRS25	1%	2K15	5322 116 53239
R 2646	MRS25	1%	82E5	5322 116 53538
R 2647	MRS25	1%	1K33	5322 116 53512
R 2648	MRS25	1%	100E	5322 116 53126
R 2651	MRS25	1%	1K	4822 116 53108
R 2654	MRS25	1%	51K1	4822 116 53121
R 2655	MRS25	1%	56K2	5322 116 53222
R 2657	MRS25	1%	56K2	5322 116 53222
R 2658	MTP10	20%	22K	5322 100 10118
R 2659	MTP10	20%	22K	5322 100 10118
R 2660	MRS25	1%	38K3	4822 116 53526
R 2661	MRS25	1%	38K3	4822 116 53526
R 2663	MRS25	1%	51K1	4822 116 53121
R 2666	MRS25	1%	1K	4822 116 53108
R 2671	MRS25	1%	1K	4822 116 53108
R 2674	MRS25	1%	147K	5322 116 53256
R 2677	MRS25	1%	196K	5322 116 53661
R 2678	MTP10	20%	22K	5322 100 10118
R 2679	MRS25	1%	90K9	5322 116 53582
R 2681	MRS25	1%	162K	5322 116 53535
R 2682	MTP10	20%	22K	5322 100 10118
R 2683	MRS25	1%	100K	4822 116 52973
R 2686	MRS25	1%	147K	5322 116 53256
R 2688	MRS25	1%	1K	4822 116 53108
R 2701	MRS25	1%	511E	5322 116 53135
R 2702	MRS25	1%	1K	4822 116 53108
R 2703	MTP10	20%	100E	5322 101 14072
R 2704	MRS25	1%	383E	5322 116 53332
R 2705	MRS25	1%	100K	4822 116 52973
R 2706	1/4W 0.1%		50E	5322 116 53165
R 2707	MRS25	1%	750E	5322 116 53265
R 2708	MRS25	1%	100K	4822 116 52973
R 2709	MRS25	1%	10K	4822 116 53022
R 2721	MRS25	1%	1M	4822 116 52843
R 2722	MRS25	1%	1M	4822 116 52843
R 2723	MRS25	1%	287K	4822 116 53119
R 2726	MRS25	1%	17K8	5322 116 53235
R 2727	MRS25	1%	17K8	5322 116 53235
R 2728	MTP10	20%	4K7	5322 101 14067
R 2729	MRS25	1%	13K3	5322 116 53489
R 2731	MRS25	1%	1M	4822 116 52843
R 2732	MRS25	1%	1M	4822 116 52843
R 2733	MRS25	1%	750K	5322 116 53727
R 2736	MRS25	1%	31K6	5322 116 53262
R 2737	MRS25	1%	31K6	5322 116 53262
R 2738	MTP10	20%	1K	5322 101 10294
R 2739	MRS25	1%	4K22	5322 116 53246
R 2741	MRS25	1%	316E	5322 116 53514
R 2742	MRS25	1%	21K5	5322 116 53241
R 2743	MRS25	1%	100K	4822 116 52973
R 2744	MRS25	1%	2K15	5322 116 53239
R 2746	MRS25	1%	1K	4822 116 53108
R 2748	MRS25	1%	10K	4822 116 53022
R 2749	MRS25	1%	10K	4822 116 53022
R 2751	MRS25	1%	2K15	5322 116 53239
R 2752	MRS25	1%	511E	5322 116 53135
R 2753	MRS25	1%	511E	5322 116 53135
R 2754	MRS25	1%	511E	5322 116 53135
R 2756	MRS25	1%	511E	5322 116 53135
R 2758	MRS25	1%	681E	4822 116 53123
R 2759	MRS25	1%	196E	5322 116 53492
R 2760	MRS25	1%	31K6	5322 116 53262
R 2801	MRS25	1%	10E	4822 116 52891
R 2802	MRS25	1%	511K	5322 116 53334

POSNR	DESCRIPTION	ORDERING CODE
R 2803	MRS25 1% 21K5	5322 116 53241
R 2804	MRS25 1% 68K1	5322 116 53338
R 2806	MRS25 1% 237E	5322 116 53259
R 2807	MRS25 1% 100K	4822 116 52973
R 2808	MRS25 1% 1M	4822 116 52843
R 2809	MRS25 1% 1M	4822 116 52843
R 2811	MRS25 1% 31K6	5322 116 53262
R 2812	VR25 5% 10M	4822 110 72214
R 2813	MRS25 1% 511E	5322 116 53135
R 2814	MRS25 1% 1K	4822 116 53108
R 2816	MRS25 1% 68K1	5322 116 53338
R 2821	VR37 5% 3M3	4822 110 42201
R 2822	VR37 5% 4M7	4822 110 42205
R 2823	VR25 5% 2M2	4822 110 72196
R 2824	VR25 5% 2M2	4822 110 72196
R 2826	VR25 5% 2M2	4822 110 72196
R 2827	VR25 5% 2M2	4822 110 72196
R 2828	MRS25 1% 100E	5322 116 53126
R 2831	MRS25 1% 19K6	5322 116 53258
R 2832	MTP10 20% 10K	5322 101 14066
R 2833	MRS25 1% 100K	4822 116 52973
R 2834	MRS25 1% 100K	4822 116 52973
R 2836	MRS25 1% 1K	4822 116 53108
R 3001	NFR25 5% 1E	4822 111 30483
R 3002	MRS25 1% 383E	5322 116 53332
R 3101	-105-102 1K	5322 111 90463
R 3102	-105-102 1K	5322 111 90463
R 3103	-105-102 1K	5322 111 90463
R 3104	MRS25 1% 1K	4822 116 53108
R 3106	MRS25 1% 1K	4822 116 53108
R 3107	MRS25 1% 1E	4822 116 52976
R 3108	MRS25 1% 1K	4822 116 53108
R 3109	MRS25 1% 1K	4822 116 53108
R 3111	MRS25 1% 2K87	5322 116 53513
R 3112	MRS25 1% 1K	4822 116 53108
R 3113	MRS25 1% 1K	4822 116 53108
R 3117	MRS25 1% 1E	4822 116 52976
R 3118	MRS25 1% 1E	4822 116 52976
R 3119	MRS25 1% 1E	4822 116 52976
R 3121	MRS25 1% 1E	4822 116 52976
R 3122	MRS25 1% 1E	4822 116 52976
R 3123	1/4W .25% 10K	5322 116 80232
R 3124	1/4W 0.1% 20K	5322 116 52697
R 3127	MRS25 1% 6K81	5322 116 53252
R 3128	0.3W 25% 4K7	5322 105 20034
R 3134	1/4W .25% 10K	5322 116 80232
R 3136	1/4W 0.1% 20K	5322 116 52697
R 3138	MRS25 1% 6K81	5322 116 53252
R 3139	0.3W 25% 4K7	5322 105 20034
R 3141	MRS25 1% 100K	4822 116 52973
R 3142	MRS25 1% 2K61	5322 116 53327
R 3143	MRS25 1% 100K	4822 116 52973
R 3144	MRS25 1% 619E	5322 116 53337
R 3146	MRS25 1% 82E5	5322 116 53538
R 3147	MRS25 1% 2K61	5322 116 53327
R 3148	MRS25 1% 619E	5322 116 53337
R 3149	MRS25 1% 82E5	5322 116 53538
R 3151	MRS25 1% 100K	4822 116 52973
R 3152	MRS25 1% 2K61	5322 116 53327
R 3153	MRS25 1% 100K	4822 116 52973
R 3154	MRS25 1% 619E	5322 116 53337
R 3156	MRS25 1% 82E5	5322 116 53538
R 3157	MRS25 1% 2K61	5322 116 53327
R 3158	MRS25 1% 619E	5322 116 53337
R 3159	MRS25 1% 82E5	5322 116 53538
R 3161	MRS25 1% 100K	4822 116 52973
R 3162	MRS25 1% 2K61	5322 116 53327
R 3163	MRS25 1% 100K	4822 116 52973
R 3164	MRS25 1% 619E	5322 116 53337
R 3166	MRS25 1% 82E5	5322 116 53538
R 3167	MRS25 1% 1E	4822 116 52976
R 3168	MRS25 1% 1E	4822 116 52976
R 3169	MRS25 1% 1K96	5322 116 53237
R 3171	0.3W 25% 470E	5322 105 20028
R 3172	MRS25 1% 3K16	4822 116 53021
R 3173	MRS25 1% 1K96	5322 116 53237
R 3174	MRS25 1% 1K96	5322 116 53237
R 3176	MRS25 1% 511E	5322 116 53135
R 3177	MRS25 1% 511E	5322 116 53135
R 3178	MRS25 1% 1K96	5322 116 53237
R 3179	0.3W 25% 470E	5322 105 20028
R 3181	MRS25 1% 3K16	4822 116 53021
R 3182	MRS25 1% 1K96	5322 116 53237
R 3183	MRS25 1% 1K96	5322 116 53237
R 3184	MRS25 1% 511E	5322 116 53135
R 3186	MRS25 1% 511E	5322 116 53135
R 3301	MRS25 1% 1K21	4822 116 52956
R 3302	MRS25 1% 16K2	5322 116 53589
R 3303	MRS25 1% 10K	4822 116 53022
R 3304	MRS25 1% 3K16	4822 116 53021

POSNR	DESCRIPTION	ORDERING CODE
R 3305	MRS25 1% 10K	4822 116 53022
R 3306	MRS25 1% 10K	4822 116 53022
R 3307	0.3W 25% 10K	4822 105 10455
R 3308	0.3W 25% 1K	5322 105 20032
R 3309	MRS25 1% 46E4	5322 116 53248
R 3310	MRS25 1% 10K	4822 116 53022
R 3311	MRS25 1% 10K	4822 116 53022
R 3312	MRS25 1% 100K	4822 116 52973
R 3313	MRS25 1% 2K61	5322 116 53327
R 3314	MRS25 1% 82E5	5322 116 53538
R 3315	MRS25 1% 75E	5322 116 53339
R 3316	MRS25 1% 619E	5322 116 53337
R 3317	MRS25 1% 75E	5322 116 53339
R 3318	MRS25 1% 4K64	5322 116 53212
R 3322	0.3W 25% 2K2	5322 105 20033
R 3323	MRS25 1% 3K16	4822 116 53021
R 3324	MRS25 1% 14K7	4822 116 53531
R 3326	MRS25 1% 19K6	5322 116 53258
R 3327	MRS25 1% 3K16	4822 116 53021
R 3328	MRS25 1% 511E	5322 116 53135
R 3329	MRS25 1% 11K	4822 116 52907
R 3331	MRS25 1% 316E	5322 116 53514
R 3332	MRS25 1% 4K22	5322 116 53246
R 3333	MRS25 1% 196E	5322 116 53492
R 3334	MRS25 1% 237E	5322 116 53259
R 3336	MRS25 1% 1E	4822 116 52976
R 3337	MRS25 1% 90E9	5322 116 53626
R 3338	MRS25 1% 6K19	5322 116 53263
R 3339	MRS25 1% 750E	5322 116 53265
R 3341	MRS25 1% 8K25	5322 116 53267
R 3342	MRS25 1% 464E	5322 116 53232
R 3343	MRS25 1% 90E9	5322 116 53626
R 3344	MRS25 1% 19K6	5322 116 53258
R 3345	MRS25 1% 10K	4822 116 53022
R 3346	0.3W 25% 22K	5322 105 20035
R 3347	MRS25 1% 2K61	5322 116 53327
R 3348	0.3W 25% 22K	5322 105 20035
R 3349	VR25 5% 10M	4822 110 72214
R 3350	MRS25 1% 10K	4822 116 53022
R 3351	MRS25 1% 82E5	5322 116 53538
R 3352	MRS25 1% 619E	5322 116 53337
R 3354	MRS25 1% 7K5	4822 116 53028
R 3355	MRS25 1% 1K96	5322 116 53237
R 3356	MRS25 1% 2K87	5322 116 53513
R 3357	MRS25 1% 1K96	5322 116 53237
R 3358	MRS25 1% 2K15	5322 116 53239
R 3359	MRS25 1% 10K	4822 116 53022
R 3361	MRS25 1% 316E	5322 116 53514
R 3362	MRS25 1% 316E	5322 116 53514
R 3363	MRS25 1% 1K	4822 116 53108
R 3364	MRS25 1% 316E	5322 116 53514
R 3365	MRS25 1% 464E	5322 116 53232
R 3366	MRS25 1% 316E	5322 116 53514
R 3367	MRS25 1% 100E	5322 116 53126
R 3368	MRS25 1% 100E	5322 116 53126
R 3369	MRS25 1% 1K	4822 116 53108
R 3370	MRS25 1% 3K16	4822 116 53021
R 3371	MRS25 1% 316E	5322 116 53514
R 3372	MRS25 1% 261E	5322 116 53549
R 3373	MRS25 1% 147E	5322 116 53569
R 3374	MRS25 1% 511E	5322 116 53135
R 3376	MRS25 1% 10K	4822 116 53022
R 3377	MRS25 1% 2K15	5322 116 53239
R 3378	MRS25 1% 2K87	5322 116 53513
R 3379	0.3W 25% 1K	5322 105 20032
R 3382	MRS25 1% 2K61	5322 116 53327
R 3383	MRS25 1% 10K	4822 116 53022
R 3384	0.3W 25% 2K2	5322 105 20033
R 3387	MRS25 1% 5K11	5322 116 53494
R 3388	MRS25 1% 10K	4822 116 53022
R 3389	MRS25 1% 100K	4822 116 52973
R 3390	MRS25 1% 619E	5322 116 53337
R 3391	MRS25 1% 2K61	5322 116 53327
R 3392	0.3W 25% 4K7	5322 105 20034
R 3393	MRS25 1% 2K61	5322 116 53327
R 3394	MRS25 1% 4K64	5322 116 53212
R 3395	MRS25 1% 825E	5322 116 53541
R 3396	MRS25 1% 82E5	5322 116 53538
R 3397	MRS25 1% 619E	5322 116 53337
R 3398	MRS25 1% 1K	4822 116 53108
R 3399	MRS25 1% 9K09	5322 116 53253
R 3400	MRS25 1% 316E	5322 116 53514
R 3401	MRS25 1% 9K09	5322 116 53253
R 3402	MRS25 1% 196K	5322 116 53661
R 3403	MRS25 1% 31E6	5322 116 54964
R 3404	MRS25 1% 2K37	5322 116 53536
R 3406	MRS25 1% 1K1	5322 116 53473
R 3407	MRS25 1% 17K8	5322 116 53235
R 3408	MRS25 1% 10E	4822 116 52891
R 3409	MRS25 1% 17K8	5322 116 53235

POSNR	DESCRIPTION	ORDERING CODE
R 3411	MRS25 1% 31E6	5322 116 54964
R 3412	MRS25 1% 14K7	4822 116 53531
R 3413	MRS25 1% 6K81	5322 116 53252
R 3416	MRS25 1% 1K1	5322 116 53473
R 3417	MRS25 1% 750E	5322 116 53265
R 3418	MRS25 1% 121E	4822 116 52955
R 3419	MRS25 1% 100K	4822 116 52973
R 3421	MRS25 1% 1E	4822 116 52976
R 3423	MRS25 1% 1E	4822 116 52976
R 3424	MRS25 1% 121E	4822 116 52955
R 3426	MRS25 1% 619E	5322 116 53337
R 3427	MRS25 1% 1E	4822 116 52976
R 3429	MRS25 1% 1E	4822 116 52976
R 3501	MCR18 1% 51E	5322 111 91352
R 3502	MCR18 1% 51E	5322 111 91352
R 3503	MCR18 1% 470E	5322 111 90109
R 3504	MCR18 1% 100E	5322 111 91134
R 3506	MCR18 1% 120E	4822 111 90339
R 3507	MCR18 1% 51E	5322 111 91352
R 3509	MCR18 1% 51E	5322 111 91352
R 3511	MCR18 1% 51E	5322 111 91352
R 3512	MCR18 1% 3K9	5322 111 91135
R 3513	MCR18 1% 10E	5322 111 90095
R 3514	MCR18 1% 10E	5322 111 90095
R 3515	MCR18 1% 10K	4822 111 90249
R 3517	MCR18 1% 33E	4822 111 90357
R 3518	MCR18 1% 82E	4822 111 90124
R 3519	MCR18 1% 8K2	5322 111 90118
R 3520	MCR18 1% 100K	4822 111 90214
R 3521	MCR18 1% 1K2	5322 111 90096
R 3523	MCR18 1% 51E	5322 111 91352
R 3524	MCR18 1% 910E	5322 111 91472
R 3525	MCR18 1% 910E	5322 111 91472
R 3526	MCR18 1% 51E	5322 111 91352
R 3529	MCR18 1% 51E	5322 111 91352
R 3530	MCR18 1% 10K	4822 111 90249
R 3531	MCR18 1% 51E	5322 111 91352
R 3532	MCR18 1% 2K7	4822 111 90569
R 3533	MCR18 1% 2K2	4822 111 90248
R 3534	MCR18 1% 100E	5322 111 91134
R 3535	MCR18 1% 130E	5322 116 80593
R 3536	MCR18 1% 1K1	5322 111 91466
R 3537	MCR18 1% 1K2	5322 111 90096
R 3539	MCR18 1% 2K7	4822 111 90569
R 3540	MCR18 1% 100E	5322 111 91134
R 3541	MCR18 1% 910E	5322 111 91472
R 3542	MCR18 1% 100E	5322 111 91134
R 3543	MCR18 1% 910E	5322 111 91472
R 3544	MCR18 1% 2K7	4822 111 90569
R 3545	MCR18 1% 100E	5322 111 91134
R 3546	MCR18 1% 13K	5322 116 80595
R 3547	MCR18 1% 4K3	5322 116 80605
R 3548	MCR18 1% 150E	5322 111 90098
R 3549	MCR18 1% 150E	5322 111 90098
R 3550	MCR18 1% 4K3	5322 116 80605
R 3551	MCR18 1% 100E	5322 111 91134
R 3552	MCR18 1% 2K	5322 116 80858
R 3553	MCR18 1% 2K	5322 116 80858
R 3554	MCR18 1% 100E	5322 111 91134
R 3555	MCR18 1% 100E	5322 111 91134
R 3556	MCR18 1% 820E	4822 111 90171
R 3557	MCR18 1% 33E	4822 111 90357
R 3558	MCR18 1% 820E	4822 111 90171
R 3559	MCR18 1% 51E	5322 111 91352
R 3560	MCR18 1% 51E	5322 111 91352
R 3561	MCR18 1% 100E	5322 111 91134
R 3562	MCR18 1% 51E	5322 111 91352
R 3563	MCR18 1% 39E	4822 111 90361
R 3564	MCR18 1% 10E	5322 111 90095
R 3566	MCR18 1% 51E	5322 111 91352
R 3567	MCR18 1% 330E	5322 111 90106
R 3568	MCR18 1% 560E	5322 111 90113
R 3569	MCR18 1% 270E	4822 111 90154
R 3570	MCR18 1% 270E	4822 111 90154
R 3571	MCR18 1% 750E	5322 111 91539
R 3573	MCR18 1% 390E	5322 111 91205
R 3574	MCR18 1% 75E	4822 111 90371
R 3575	MCR18 1% 51E	5322 111 91352
R 3576	MCR18 1% 51E	5322 111 91352
R 3577	MCR18 1% 3K3	4822 111 90157
R 3578	MCR18 1% 150E	5322 111 90098
R 3579	MCR18 1% 150E	5322 111 90098
R 3580	MCR18 1% 100E	5322 111 91134
R 3581	MCR18 1% 100E	5322 111 91134
R 3582	MCR18 1% 10E	5322 111 90095
R 3583	MCR18 1% 10E	5322 111 90095
R 3584	MCR18 1% 100E	5322 111 91134
R 3585	MCR18 1% 100E	5322 111 91134
R 3586	MCR18 1% 10E	5322 111 90095
R 3587	MCR18 1% 470E	5322 111 90109

POSNR	DESCRIPTION	ORDERING CODE
R 3588	MCR18 1% 200E	5322 116 80599
R 3589	RC-01 5% 1E	4822 111 90184
R 3590	RC-01 5% 1E	4822 111 90184
R 3591	MCR18 1% 39E	4822 111 90361
R 3592	MCR18 1% 220E	4822 111 90178
R 3594	MCR18 1% 10E	5322 111 90095
R 3595	MCR18 1% 51E	5322 111 91352
R 3596	MCR18 1% 130E	5322 116 80593
R 3601	MCR18 1% 33E	4822 111 90357
R 3603	MCR18 1% 51E	5322 111 91352
R 3604	MCR18 1% 100E	5322 111 91134
R 3605	MCR18 1% 100E	5322 111 91134
R 3606	MCR18 1% 100E	5322 111 91134
R 3607	MCR18 1% 100E	5322 111 91134
R 3608	MCR18 1% 15E	4822 111 90344
R 3609	MCR18 1% 15E	4822 111 90344
R 3611	MCR18 1% 5[illegible]E	4822 111 90245
R 3612	MCR18 1% 5[illegible]E	5322 111 90113
R 3613	MCR18 1% 1[illegible]	5322 111 90096
R 3614	MCR18 1% 1K[illegible]	5322 111 90096
R 3616	MCR18 1% 1[illegible]	5322 111 90095
R 3617	MCR18 1% 1[illegible]E	4822 111 90345
R 3618	MCR18 1% 1[illegible]	4822 111 90151
R 3619	MCR18 1% 8K[illegible]	5322 111 90118
R 3621	MCR18 1% 100K	4822 111 90214
R 3622	MCR18 1% 100E	5322 111 91134
R 3623	MCR18 1% 1[illegible]	5322 111 91349
R 3701	MRS25 1% 1[illegible]	4822 116 52976
R 3702	MRS25 1% 1[illegible]	4822 116 52976
R 3703	MRS25 1% 1[illegible]	4822 116 52976
R 3704	MRS25 1% 1[illegible]	4822 116 52976
R 3706	MRS25 1% 1[illegible]	4822 116 52976
R 3707	MRS25 1% 1[illegible]	4822 116 52976
R 3708	MRS25 1% 1[illegible]	4822 116 52976
R 3709	MRS25 1% 1[illegible]	4822 116 52976
R 3711	MRS25 1% 1[illegible]	4822 116 52976
R 3713	MRS25 1% 1[illegible]	4822 116 52976
R 3716	MRS25 1% 1[illegible]	4822 116 53108
R 3716	MRS25 1% 1[illegible]	4822 116 53108
R 3717	MRS25 1% 1[illegible]	4822 116 52976
R 3718	MRS25 1% 1[illegible]	4822 116 52976
R 3719	MRS25 1% 1[illegible]	4822 116 52976
R 3721	MRS25 1% 1[illegible]	4822 116 53108
R 3722	MRS25 1% 1[illegible]	4822 116 53569
R 3723	MRS25 1% 1[illegible]	5322 116 53327
R 3724	0.3W 25% [illegible]	5322 105 20031
R 3726	MRS25 1% [illegible]	5322 116 53549
R 3727	MRS25 1% [illegible]	5322 116 53645
R 3728	MRS25 1% [illegible]	5322 116 53126
R 3729	MRS25 1% [illegible]	5322 116 53265
R 4001	MRS25 1% 1[illegible]	4822 116 52906
R 4002	MRS25 1% 110E	4822 116 52906
R 4003	MRS25 1% 110E	4822 116 52906
R 4004	MRS25 1% 110E	4822 116 52906
R 4006	MRS25 1% 110E	4822 116 52906
R 4007	MRS25 1% 110E	4822 116 52906
R 4008	MRS25 1% 110E	4822 116 52906
R 4009	MRS25 1% 110E	4822 116 52906
R 4011	MRS25 1% 110E	4822 116 52906
R 4012	MRS25 1% 110E	4822 116 52906
R 4013	MRS25 1% 110E	4822 116 52906
R 4014	MRS25 1% 2K15	4822 116 53239
R 4016	MRS25 1% 2K15	5322 116 53239
R 4017	MRS25 1% 10E	4822 116 52891
R 4018	MRS25 1% 1E	4822 116 52976
R 4019	MRS25 1% 1E	4822 116 52976
R 4021	-101-333 33K	5322 111 90881
R 4022	-101-333 33K	5322 111 90881
R 4023	-105-103 10K	5322 111 90473
R 4024	-105-103 10K	5322 111 90473
R 4026	-105-103 10K	5322 111 90473
R 4027	-105-103 10K	5322 111 90473
R 4028	-101-333 33K	5322 111 90881
R 4029	-101-333 33K	5322 111 90881
R 4201	MRS25 1% 1K47	5322 116 53185
R 4202	-105-103 10K	5322 111 90473
R 4203	MRS25 1% 1K96	5322 116 53237
R 4204	-105-102 1K	5322 111 90463
R 4206	MRS25 1% 287E	5322 116 53221
R 4207	MRS25 1% 287E	5322 116 53221
R 4208	MRS25 1% 287E	5322 116 53221
R 4209	MRS25 1% 287E	5322 116 53221
R 4211	MRS25 1% 287E	5322 116 53221
R 4212	MRS25 1% 287E	5322 116 53221
R 4213	MRS25 1% 287E	5322 116 53221
R 4214	MRS25 1% 287E	5322 116 53221
R 4216	MRS25 1% 287E	5322 116 53221
R 4217	MRS25 1% 287E	5322 116 53221
R 4218	MRS25 1% 287E	5322 116 53221
R 4219	MRS25 1% 287E	5322 116 53221

POSNR	DESCRIPTION	ORDERING CODE
R 4221	MRS25 1% 287E	5322 116 53221
R 4222	-105-102 1K	5322 111 90463
R 4223	MRS25 1% 1E	4822 116 52976
R 4224	MRS25 1% 1E	4822 116 52976
R 4401	MRS25 1% 100K	4822 116 52973
R 4402	1.7A 20% 82E	4822 116 30069
R 4403	1.7A 20% 82E	4822 116 30069
R 4404	MRS25 1% 10E	4822 116 52891
R 4406	MRS25 1% 316K	4822 116 53058
R 4407	MRS25 1% 1M	4822 116 52843
R 4408	MRS25 1% 215K	5322 116 53425
R 4409	MRS25 1% 21K5	5322 116 53241
R 4411	MRS25 1% 34K8	5322 116 53429
R 4412	MRS25 1% 38K3	4822 116 53526
R 4413	MRS25 1% 26K1	5322 116 53261
R 4414	MRS25 1% 1M	4822 116 52843
R 4416	MRS25 1% 10K	4822 116 53022
R 4417	MRS25 1% 100K	4822 116 52973
R 4418	MRS25 1% 383K	5322 116 53576
R 4419	MRS25 1% 383K	5322 116 53576
R 4421	MRS25 1% 100K	4822 116 52973
R 4422	MRS25 1% 10K	4822 116 53022
R 4423	MRS25 1% 215K	5322 116 53425
R 4424	MRS25 1% 215K	5322 116 53425
R 4426	MRS25 1% 100E	5322 116 53126
R 4427	MRS25 1% 51K1	4822 116 53121
R 4428	MRS25 1% 51K1	4822 116 53121
R 4429	MRS25 1% 51K1	4822 116 53121
R 4431	MRS25 1% 51K1	4822 116 53121
R 4432	MRS25 1% 2E15	5322 116 53722
R 4434	MRS25 1% 215K	5322 116 53425
R 4436	MRS25 1% 215K	5322 116 53425
R 4437	MRS25 1% 100E	5322 116 53126
R 4438	MRS25 1% 464E	5322 116 53232
R 4439	MRS25 1% 10K	4822 116 53022
R 4440	MRS25 1% 21E5	5322 116 53426
R 4441	MRS25 1% 100E	5322 116 53126
R 4442	MRS25 1% 10K	4822 116 53022
R 4443	MRS25 1% 14K7	4822 116 53531
R 4444	0.5W 10% 1K5	4822 116 30248
R 4446	MRS25 1% 215E	5322 116 53325
R 4447	MRS25 1% 215E	5322 116 53325
R 4448	MRS25 1% 1E1	4822 116 52908
R 4449	MRS25 1% 1E1	4822 116 52908
R 4451	MRS25 1% 1E1	4822 116 52908
R 4452	MRS25 1% 1E1	4822 116 52908
R 4454	MRS25 1% 21K5	5322 116 53241
R 4456	MRS25 1% 1K	4822 116 53108
R 4459	MRS25 1% 10K	4822 116 53022
R 4461	MRS25 1% 100K	4822 116 52973
R 4462	MRS25 1% 1K	4822 116 53108
R 4463	MRS25 1% 4K64	5322 116 53212
R 4464	MRS25 1% 100K	4822 116 52973
R 4466	MRS25 1% 5K11	5322 116 53494
R 4467	MRS25 1% 1K	4822 116 53108
R 4468	MRS25 1% 100E	5322 116 53126
R 4469	70 DEG C	5322 116 40093
R 4471	MRS25 1% 1K	4822 116 53108
R 4472	1/4W .25% 14K	5322 116 53194
R 4473	MRS25 1% 348E	5322 116 53591
R 4474	1/4W .25% 10K	5322 116 80232
R 4476	MRS25 1% 348E	5322 116 53591
R 4477	1/4W .25% 10K	5322 116 80232
R 4478	1/4W .25% 14K	5322 116 53194
R 4479	MRS25 1% 100K	4822 116 52973
R 4481	MRS25 1% 100E	5322 116 53126
R 4481	10% 4.7NF	4822 122 31125
R 4482	10% 1NF	4822 122 30027
R 4483	1/4W .25% 10K	5322 116 80232
R 4483	-20+50% 10NF	4822 122 31414
R 4484	1/4W .25% 4K48	5322 116 80237
R 4484	10% 1NF	4822 122 30027
R 4486	MRS25 1% 750E	5322 116 53265
R 4487	1/4W .25% 10K	5322 116 80232
R 4488	1/4W .25% 4K48	5322 116 80237
R 4489	MRS25 1% 750E	5322 116 53265
R 4491	MRS25 1% 8K25	5322 116 53267
R 4492	MRS25 1% 1K	4822 116 53108
R 4493	MRS25 1% 14E7	4822 116 53037
R 4494	MRS25 1% 1K	4822 116 53108
R 4496	MRS25 1% 10E	4822 116 52891
R 4497	MRS25 1% 511E	5322 116 53135
R 4498	MRS25 1% 21E5	5322 116 53426
R 4499	MRS25 1% 21E5	5322 116 53426
R 4601	MRS25 1% 1K47	5322 116 53185
R 4602	MRS25 1% 196K	5322 116 53661
R 4603	MRS25 1% 422E	5322 116 53592
R 4604	MRS25 1% 3K48	4822 116 53315
R 4606	MRS25 1% 26K1	5322 116 53261
R 4607	MTP10 20% 10K	5322 101 14066

POSNR	DESCRIPTION	ORDERING CODE
R 4608	MRS25 1% 6K81	5322 116 53252
R 4609	1/4W 0.1% 147K	5322 116 80246
R 4611	VR37 1% 31M6	5322 116 64103
R 4612	MRS25 1% 681K	5322 116 53593
R 4613	MRS25 1% 16K2	5322 116 53589
R 4614	MRS25 1% 10K	4822 116 53022
R 4616	MRS25 1% 464E	5322 116 53232
R 4617	MRS25 1% 4K64	5322 116 53212
R 4618	MRS25 1% 46E4	5322 116 53248
R 4619	MRS25 1% 46K4	5322 116 53314
R 4621	MRS25 1% 215E	5322 116 53325
R 4622	MRS25 1% 4K64	5322 116 53212
R 4623	MRS25 1% 1E	4822 116 52976
R 4624	MRS25 1% 100E	5322 116 53126
R 4626	MRS25 1% 100E	5322 116 53126
R 4627	MRS25 1% 10K	4822 116 53022
R 4628	MRS25 1% 19K6	5322 116 53258
R 4629	MRS25 1% 19K6	5322 116 53258
R 4631	MRS25 1% 10K	4822 116 53022
R 4632	MRS25 1% 1M	4822 116 52843
R 4633	MRS25 1% 287K	4822 116 53119
R 4634	MRS25 1% 147K	5322 116 53256
R 4636	MRS25 1% 100K	4822 116 52973
R 4637	MRS25 1% 100E	5322 116 53126
R 4638	MRS25 1% 10K	4822 116 53022
R 4639	MRS25 1% 11K	4822 116 52907
R 4641	MRS25 1% 16K2	5322 116 53589
R 4643	MRS25 1% 2K87	5322 116 53513
R 4644	MRS25 1% 100K	4822 116 52973
R 4646	MRS25 1% 3K48	4822 116 53315
R 4647	MRS25 1% 28K7	4822 116 53215
R 4648	MRS25 1% 10K	4822 116 53022
R 4649	MRS25 1% 10K	4822 116 53022
R 4651	MRS25 1% 1K	4822 116 53108
R 4652	MRS25 1% 1K	4822 116 53108
R 4653	MRS25 1% 3K16	4822 116 53021
R 4654	MRS25 1% 750E	5322 116 53265
R 4656	0.5W 10% 3K3	5322 116 30234
R 4657	MRS25 1% 196E	5322 116 53492
R 4658	MRS25 1% 12K1	4822 116 52957
R 4659	MRS25 1% 2K15	5322 116 53239
R 4661	MRS25 1% 1K47	5322 116 53185
R 4662	MRS25 1% 681E	4822 116 53123
R 4663	MRS25 1% 10E	4822 116 52891
R 4664	MRS25 1% 10E	4822 116 52891
R 4666	MRS25 1% 3K16	4822 116 53021
R 4667	VR68 5% 68M	5322 116 64035
R 4667	VR68 5% 68M	5322 116 64035
R 5001	MRS25 1% 3K16	4822 116 53021
R 5002	MRS25 1% 2K87	5322 116 53513
R 5003	MRS25 1% 2K87	5322 116 53513
R 5004	MRS25 1% 2K61	5322 116 53327
R 5006	MRS25 1% 2K61	5322 116 53327
R 5007	MRS25 1% 2K61	5322 116 53327
R 5008	MRS25 1% 7K5	4822 116 53028
R 5009	MRS25 1% 7K5	4822 116 53028
R 5011	MRS25 1% 7K5	4822 116 53028
R 5012	MRS25 1% 7K5	4822 116 53028
R 5013	MRS25 1% 1K47	5322 116 53185
R 5014	0.3W 25% 4K7	5322 105 20034
R 5016	MRS25 1% 2K87	5322 116 53513
R 5017	MRS25 1% 2K87	5322 116 53513
R 5018	MRS25 1% 51E1	5322 116 53213
R 5019	MRS25 1% 68E1	5322 116 53264
R 5020	0.3W 25% 100E	5322 105 20029
R 5021	MRS25 1% 3K83	4822 116 53079
R 5023	MRS25 1% 38K3	4822 116 53526
R 5024	MRS25 1% 3K16	4822 116 53021
R 5025	MRS25 1% 100E	5322 116 53126
R 5026	MRS25 1% 4K64	5322 116 53212
R 5027	VR25 5% 1M5	4822 110 72192
R 5028	MRS25 1% 10K	4822 116 53022
R 5029	MRS25 1% 215E	5322 116 53325
R 5030	MRS25 1% 100E	5322 116 53126
R 5031	0.3W 25% 2K2	5322 105 20033
R 5032	MRS25 1% 2K15	5322 116 53239
R 5033	MRS25 1% 3K83	4822 116 53079
R 5034	MRS25 1% 215E	5322 116 53325
R 5035	MRS25 1% 3K83	4822 116 53079
R 5036	MRS25 1% 3K16	4822 116 53021
R 5040	MRS25 1% 1K78	5322 116 53208
R 5045	MRS25 1% 100E	5322 116 53126
R 5050	MRS25 1% 21K5	5322 116 53241
R 5051	MRS25 1% 4K22	5322 116 53246
R 5052	MRS25 1% 3K16	4822 116 53021
R 5053	1/4W .25% 10K	5322 116 80232
R 5056	1/4W 0.1% 4K99	5322 116 80854
R 5058	1/4W .25% 10K	5322 116 80232
R 5061	1/4W 0.1% 4K99	5322 116 80854
R 5062	1/4W .25% 10K	5322 116 80232

POSNR	DESCRIPTION	ORDERING CODE
R 5063	1/4W 0.1% 1K	5322 116 52698
R 5064	MRS25 1% 10E	4822 116 52891
R 5066	1/4W .25% 2K41	5322 116 80855
R 5067	1/4W 0.1% 3K32	5322 116 80866
R 5068	1/4W 0.1% 111E	5322 116 80865
R 5071	MRS25 1% 110E	4822 116 52906
R 5072	MRS25 1% 3K48	4822 116 53315
R 5073	MRS25 1% 237K	5322 116 80145
R 5074	MRS25 1% 1K78	5322 116 53208
R 5076	MRS25 1% 28K7	4822 116 53215
R 5077	MRS25 1% 3K48	4822 116 53315
R 5078	MRS25 1% 1K	4822 116 53108
R 5079	MRS25 1% 4K22	5322 116 53246
R 5081	MRS25 1% 1K	4822 116 53108
R 5082	MRS25 1% 6K81	5322 116 53252
R 5084	MRS25 1% 4K22	5322 116 53246
R 5086	MRS25 1% 38K3	4822 116 53526
R 5087	MRS25 1% 1K	4822 116 53108
R 5088	MRS25 1% 7K5	4822 116 53028
R 5089	MRS25 1% 11K	4822 116 52907
R 5091	MRS25 1% 38K3	4822 116 53526
R 5092	MRS25 1% 5K11	5322 116 53494
R 5094	MRS25 1% 5K11	5322 116 53494
R 5096	0.3W 25% 10K	4822 105 10455
R 5103	MRS25 1% 2K61	5322 116 53327
R 5106	MRS25 1% 2K61	5322 116 53327
R 5107	MRS25 1% 7K5	4822 116 53028
R 5108	MRS25 1% 1K	4822 116 53108
R 5111	MRS25 1% 1K	4822 116 53108
R 5112	MRS25 1% 56K2	5322 116 53222
R 5113	MRS25 1% 3K16	4822 116 53021
R 5114	MRS25 1% 9K09	5322 116 53253
R 5116	MRS25 1% 511E	5322 116 53135
R 5117	MRS25 1% 6K19	5322 116 53263
R 5118	0.3W 25% 47K	5322 105 20036
R 5119	MRS25 1% 100K	4822 116 52973
R 5121	MRS25 1% 261E	5322 116 53549
R 5122	MRS25 1% 511E	5322 116 53135
R 5123	MRS25 1% 1K	4822 116 53108
R 5124	MRS25 1% 42K2	5322 116 53431
R 5126	MRS25 1% 2K15	5322 116 53239
R 5127	0.3W 25% 1K	5322 105 20032
R 5128	MRS25 1% 8K25	5322 116 53267
R 5129	MRS25 1% 5K11	5322 116 53494
R 5132	MRS25 1% 3K16	4822 116 53021
R 5133	MRS25 1% 100K	4822 116 52973
R 5134	MRS25 1% 10E	4822 116 52891
R 5136	MRS25 1% 100K	4822 116 52973
R 5137	MRS25 1% 10E	4822 116 52891
R 5139	MRS25 1% 10K	4822 116 53022
R 5141	MRS25 1% 10K	4822 116 53022
R 5142	MRS25 1% 10K	4822 116 53022
R 5143	MRS25 1% 5K11	5322 116 53494
R 5144	MRS25 1% 1K78	5322 116 53208
R 5146	MRS25 1% 10E	4822 116 52891
R 5147	MRS25 1% 10K	4822 116 53022
R 5148	MRS25 1% 10E	4822 116 52891
R 5149	MRS25 1% 10K	4822 116 53022
R 5152	MRS25 1% 10K	4822 116 53022
R 5153	MRS25 1% 10E	4822 116 52891
R 5154	MRS25 1% 10K	4822 116 53022
R 5156	MRS25 1% 10E	4822 116 52891
R 5157	MRS25 1% 10K	4822 116 53022
R 5158	MRS25 1% 10K	4822 116 53022
R 5159	MRS25 1% 10K	4822 116 53022
R 5161	MRS25 1% 10E	4822 116 52891
R 5162	MRS25 1% 10E	4822 116 52891
R 5163	MRS25 1% 10E	4822 116 52891
R 5164	MRS25 1% 10E	4822 116 52891
R 5167	MRS25 1% 10E	4822 116 52891
R 5168	MRS25 1% 10E	4822 116 52891
R 5169	MRS25 1% 10E	4822 116 52891
R 5171	MRS25 1% 10E	4822 116 52891
R 5172	MRS25 1% 10K	4822 116 53022
R 5173	VR25 5% 2M7	4822 110 72198
R 5201	MCR18 1% 51E	5322 111 91352
R 5202	MCR18 1% 51E	5322 111 91352
R 5203	MCR18 1% 2K7	4822 111 90569
R 5206	MCR18 1% 160E	4822 111 90345
R 5207	MCR18 1% 75E	4822 111 90371
R 5208	MCR18 1% 1K3	5322 116 80594
R 5209	MCR18 1% 160E	4822 111 90345
R 5211	MCR18 1% 75E	4822 111 90371
R 5212	MCR18 1% 3K3	4822 111 90157
R 5213	MCR18 1% 22E	4822 111 90186
R 5214	MCR18 1% 1K3	5322 116 80594
R 5216	MCR18 1% 100E	5322 111 91134
R 5217	MCR18 1% 1K	5322 111 90092
R 5218	MCR18 1% 100E	5322 111 91134
R 5219	MCR18 1% 51E	5322 111 91352

POSNR	DESCRIPTION	ORDERING CODE
R 5221	MCR18 1% 1K	5322 111 90092
R 5222	MCR18 1% 2K	5322 116 80858
R 5223	MCR18 1% 2K	5322 116 80858
R 5224	MCR18 1% 51E	5322 111 91352
R 5225	MCR18 1% 51E	5322 111 91352
R 5226	MCR18 1% 51E	5322 111 91352
R 5228	MCR18 1% 51E	5322 111 91352
R 5229	MCR18 1% 100E	5322 111 91134
R 5231	MCR18 1% 2K7	4822 111 90569
R 5233	MCR18 1% 160E	4822 111 90345
R 5234	MCR18 1% 160E	4822 111 90345
R 5236	MCR18 1% 75E	4822 111 90371
R 5237	MCR18 1% 75E	4822 111 90371
R 5238	MCR18 1% 3K3	4822 111 90157
R 5239	MCR18 1% 1K3	5322 116 80594
R 5240	MCR18 1% 22E	4822 111 90186
R 5241	MCR18 1% 1K3	5322 116 80594
R 5242	MCR18 1% 51E	5322 111 91352
R 5243	MCR18 1% 1K	5322 111 90092
R 5244	MCR18 1% 51E	5322 111 91352
R 5246	MCR18 1% 100E	5322 111 91134
R 5247	MCR18 1% 1K	5322 111 90092
R 5248	MCR18 1% 2K	5322 116 80858
R 5249	MCR18 1% 2K	5322 116 80858
R 5250	MCR18 1% 51E	5322 111 91352
R 5251	MCR18 1% 51E	5322 111 91352
R 5252	MCR18 1% 51E	5322 111 91352
R 5256	MCR18 1% 51E	5322 111 91352
R 5257	MCR18 1% 100E	5322 111 91134
R 5258	MCR18 1% 2K7	4822 111 90569
R 5261	MCR18 1% 160E	4822 111 90345
R 5262	MCR18 1% 160E	4822 111 90345
R 5263	MCR18 1% 75E	4822 111 90371
R 5264	MCR18 1% 1K3	5322 116 80594
R 5266	MCR18 1% 3K3	4822 111 90157
R 5267	MCR18 1% 22E	4822 111 90186
R 5268	MCR18 1% 1K3	5322 116 80594
R 5269	MCR18 1% 51E	5322 111 91352
R 5271	MCR18 1% 75E	4822 111 90371
R 5272	MCR18 1% 100E	5322 111 91134
R 5273	MCR18 1% 1K	5322 111 90092
R 5274	MCR18 1% 51E	5322 111 91352
R 5275	MCR18 1% 51E	5322 111 91352
R 5276	MCR18 1% 1K	5322 111 90092
R 5277	MCR18 1% 680E	4822 111 90162
R 5278	MCR18 1% 51E	5322 111 91352
R 5279	MCR18 1% 680E	4822 111 90162
R 5280	MCR18 1% 51E	5322 111 91352
R 5281	MCR18 1% 100E	5322 111 91134
R 5282	MCR18 1% 100E	5322 111 91134
R 5283	MCR18 1% 680E	4822 111 90162
R 5284	MCR18 1% 220E	4822 111 90178
R 5286	MCR18 1% 220E	4822 111 90178
R 5287	MCR18 1% 680E	4822 111 90162
R 5288	MCR18 1% 20E	4822 111 90352
R 5289	MCR18 1% 20E	4822 111 90352
R 5291	MCR18 1% 680E	4822 111 90162
R 5293	MCR18 1% 100E	5322 111 91134
R 5294	MCR18 1% 100E	5322 111 91134
R 5296	MCR18 1% 680E	4822 111 90162
R 5297	MCR18 1% 2K7	4822 111 90569
R 5298	MCR18 1% 100E	5322 111 91134
R 5299	MCR18 1% 1K	5322 111 90092
R 5301	MCR18 1% 220E	4822 111 90178
R 5302	MCR18 1% 220E	4822 111 90178
R 5303	MCR18 1% 100E	5322 111 91134
R 5304	MCR18 1% 100E	5322 111 91134
R 5306	MCR18 1% 100E	5322 111 91134
R 5307	MCR18 1% 100E	5322 111 91134
R 5308	MCR18 1% 33E	4822 111 90357
R 5309	MCR18 1% 10E	5322 111 90095
R 5311	MCR18 1% 130E	5322 116 80593
R 5312	MCR18 1% 130E	5322 116 80593
R 5313	MCR18 1% 5K1	5322 111 91471
R 5314	MCR18 1% 10K	4822 111 90249
R 5316	MCR18 1% 3K3	4822 111 90157
R 5317	MCR18 1% 20K	5322 116 80601
R 5318	MCR18 1% 680E	4822 111 90162
R 5319	MCR18 1% 51E	5322 111 91352
R 5321	MCR18 1% 100E	5322 111 91134
R 5322	MCR18 1% 100E	5322 111 91134
R 5323	MCR18 1% 100E	5322 111 91134
R 5324	MCR18 1% 100E	5322 111 91134
R 5326	MCR18 1% 33E	4822 111 90357
R 5327	MCR18 1% 10E	5322 111 90095
R 5328	MCR18 1% 130E	5322 116 80593
R 5329	MCR18 1% 130E	5322 116 80593
R 5331	MCR18 1% 3K6	5322 116 80604
R 5332	MCR18 1% 3K6	5322 116 80604
R 5333	MCR18 1% 1K	5322 111 90092

POSNR	DESCRIPTION	ORDERING CODE
R 5334	MCR18 1% 51E	5322 111 91352
R 5336	MCR18 1% 51E	5322 111 91352
R 5337	MCR18 1% 1K2	5322 111 90096
R 5338	MCR18 1% 750E	5322 111 91539
R 5339	MCR18 1% 2K4	5322 111 91468
R 5341	MCR18 1% 1K5	4822 111 90151
R 5342	MCR18 1% 10K	4822 111 90249
R 5344	MCR18 1% 5K1	5322 111 91471
R 5346	MCR18 1% 470E	5322 111 90109
R 5347	MCR18 1% 470E	5322 111 90109
R 5348	MCR18 1% 2K7	4822 111 90569
R 5349	MCR18 1% 56K	5322 116 80864
R 5351	MCR18 1% 10K	4822 111 90249
R 5353	MCR18 1% 10E	5322 111 90095
R 5354	MCR18 1% 10K	4822 111 90249
R 5355	MCR18 1% 51E	5322 111 91352
R 5356	MCR18 1% 430E	5322 116 80863
R 5359	MCR18 1% 470E	5322 111 90109
R 5360	MCR18 1% 1K	5322 111 90092
R 5361	MCR18 1% 36E	5322 116 80862
R 5362	MCR18 1% 470E	5322 111 90109
R 5364	MCR18 1% 51E	5322 111 91352
R 5365	MCR18 1% 430E	5322 116 80863
R 5366	MCR18 1% 100E	5322 111 91134
R 5369	MCR18 1% 51E	5322 111 91352
R 5370	MCR18 1% 100E	5322 111 91134
R 5371	MCR18 1% 100E	5322 111 91134
R 5372	MCR18 1% 360E	5322 116 80861
R 5373	MCR18 1% 680E	4822 111 90162
R 5374	MCR18 1% 240E	5322 116 80859
R 5376	MCR18 1% 270E	4822 111 90154
R 5377	MCR18 1% 150E	5322 111 90098
R 5378	MCR18 1% 150E	5322 111 90098
R 5379	MCR18 1% 51E	5322 111 91352
R 5381	MCR18 1% 10E	5322 111 90095
R 5382	MCR18 1% 200E	5322 116 80599
R 5383	MCR18 1% 200E	5322 116 80599
R 5384	MCR18 1% 240E	5322 116 80859
R 5386	MCR18 1% 51E	5322 111 91352
R 5387	MCR18 1% 51E	5322 111 91352
R 5388	MCR18 1% 270E	4822 111 90154
R 5389	MCR18 1% 100E	5322 111 91134
R 5391	MCR18 1% 680E	4822 111 90162
R 5392	MCR18 1% 100E	5322 111 91134
R 5393	MCR18 1% 100E	5322 111 91134
R 5394	MCR18 1% 82E	4822 111 90124
R 5396	MCR18 1% 100E	5322 111 91134
R 5397	0.3W 25% 100E	5322 105 20029
R 5398	MCR18 1% 82E	4822 111 90124
R 5399	MCR18 1% 51E	5322 111 91352
R 5401	MCR18 1% 750E	5322 111 91539
R 5402	MCR18 1% 1K3	5322 116 80594
R 5403	MCR18 1% 1K5	4822 111 90151
R 5404	MCR18 1% 10K	4822 111 90249
R 5406	MCR18 1% 5K1	5322 111 91471
R 5409	MCR18 1% 22E	4822 111 90186
R 5411	MCR18 1% 22E	4822 111 90186
R 5412	MCR18 1% 100E	5322 111 91134
R 5413	MCR18 1% 100E	5322 111 91134
R 5414	MCR18 1% 22E	4822 111 90186
R 5416	MCR18 1% 22E	4822 111 90186
R 5417	MCR18 1% 100E	5322 111 91134
R 5418	MCR18 1% 100E	5322 111 91134
R 5419	MCR18 1% 22E	4822 111 90186
R 5421	MCR18 1% 22E	4822 111 90186
R 5422	MCR18 1% 100E	5322 111 91134
R 5423	MCR18 1% 100E	5322 111 91134
R 5434	MCR18 1% 51E	5322 111 91352
R 5436	MCR18 1% 6K8	4822 111 90544
R 5437	MCR18 1% 4K3	5322 116 80605
R 5438	MCR18 1% 1K	5322 111 90092
R 5439	MCR18 1% 390E	5322 111 91205
R 5441	MCR18 1% 100E	5322 111 91134
R 5442	MCR18 1% 110E	4822 111 90335
R 5443	MCR18 1% 110E	4822 111 90335
R 5444	MCR18 1% 430E	5322 116 80863
R 5446	MCR18 1% 110E	4822 111 90335
R 5447	MCR18 1% 390E	5322 111 91205
R 5448	MCR18 1% 1K	5322 111 90092
R 5449	MCR18 1% 100E	5322 111 91134
R 5451	MCR18 1% 4K3	5322 116 80605
R 5452	MCR18 1% 6K8	4822 111 90544
R 5453	MCR18 1% 51E	5322 111 91352
R 5454	MCR18 1% 510E	4822 111 90245
R 5455	0.3W 25% 100E	5322 105 20029
R 5456	MCR18 1% 510E	4822 111 90245
R 5457	MCR18 1% 510E	4822 111 90245
R 5458	MCR18 1% 200E	5322 116 80599
R 5459	MCR18 1% 200E	5322 116 80599
R 5461	MCR18 1% 200E	5322 116 80599

POSNR	DESCRIPTION	ORDERING CODE
R 5462	MCR18 1% 51E	5322 111 91352
R 5463	MCR18 1% 120E	4822 111 90339
R 5464	MCR18 1% 120E	4822 111 90339
R 5466	MCR18 1% 120E	4822 111 90339
R 5467	MCR18 1% 120E	4822 111 90339
R 5468	MCR18 1% 120E	4822 111 90339
R 5469	MCR18 1% 120E	4822 111 90339
R 5471	MCR18 1% 120E	4822 111 90339
R 5472	MCR18 1% 120E	4822 111 90339
R 5473	MCR18 1% 120E	4822 111 90339
R 5474	MCR18 1% 120E	4822 111 90339
R 5476	MCR18 1% 120E	4822 111 90339
R 5477	MCR18 1% 120E	4822 111 90339
R 5478	MCR18 1% 120E	4822 111 90339
R 5479	MCR18 1% 120E	4822 111 90339
R 5481	MCR18 1% 120E	4822 111 90339
R 5482	MCR18 1% 120E	4822 111 90339
R 5483	MCR18 1% 120E	4822 111 90339
R 5484	MCR18 1% 120E	4822 111 90339
R 5486	MCR18 1% 120E	4822 111 90339
R 5487	MCR18 1% 120E	4822 111 90339
R 5488	MCR18 1% 120E	4822 111 90339
R 5489	MCR18 1% 120E	4822 111 90339
R 5491	MCR18 1% 51E	5322 111 91352
R 5492	MCR18 1% 16E	5322 116 80857
R 5493	MCR18 1% 120E	4822 111 90339
R 5494	MCR18 1% 120E	4822 111 90339
R 5496	MCR18 1% 120E	4822 111 90339
R 5497	MCR18 1% 120E	4822 111 90339
R 5498	MCR18 1% 120E	4822 111 90339
R 5499	MCR18 1% 120E	4822 111 90339
R 6001	MRS25 1% 3K16	4822 116 53021
R 6002	MRS25 1% 2K87	5322 116 53513
R 6003	MRS25 1% 2K87	5322 116 53513
R 6004	MRS25 1% 2K61	5322 116 53327
R 6006	MRS25 1% 2K61	5322 116 53327
R 6007	MRS25 1% 2K61	5322 116 53327
R 6008	MRS25 1% 7K5	4822 116 53028
R 6009	MRS25 1% 7K5	4822 116 53028
R 6011	MRS25 1% 7K5	4822 116 53028
R 6012	MRS25 1% 7K5	4822 116 53028
R 6013	MRS25 1% 1K47	5322 116 53185
R 6014	0.3W 25% 4K7	5322 105 20034
R 6016	MRS25 1% 2K87	5322 116 53513
R 6017	MRS25 1% 2K87	5322 116 53513
R 6018	MRS25 1% 51E1	5322 116 53213
R 6019	MRS25 1% 68E1	5322 116 53264
R 6020	0.3W 25% 100E	5322 105 20029
R 6021	MRS25 1% 3K83	4822 116 53079
R 6023	MRS25 1% 38K3	4822 116 53526
R 6024	MRS25 1% 3K16	4822 116 53021
R 6025	MRS25 1% 100E	5322 116 53126
R 6026	MRS25 1% 4K64	5322 116 53212
R 6027	VR25 5% 1M5	4822 110 72192
R 6028	MRS25 1% 10K	4822 116 53022
R 6029	MRS25 1% 215E	5322 116 53325
R 6030	MRS25 1% 100E	5322 116 53126
R 6031	0.3W 25% 2K2	5322 105 20033
R 6032	MRS25 1% 2K15	5322 116 53239
R 6033	MRS25 1% 3K83	4822 116 53079
R 6034	MRS25 1% 215E	5322 116 53325
R 6035	MRS25 1% 3K83	4822 116 53079
R 6036	MRS25 1% 3K16	4822 116 53021
R 6040	MRS25 1% 1K78	5322 116 53208
R 6045	MRS25 1% 100E	5322 116 53126
R 6050	MRS25 1% 21K5	5322 116 53241
R 6051	MRS25 1% 4K22	5322 116 53246
R 6052	MRS25 1% 3K16	4822 116 53021
R 6053	1/4W .25% 10K	5322 116 80232
R 6056	1/4W 0.1% 4K99	5322 116 80854
R 6058	1/4W .25% 10K	5322 116 80232
R 6061	1/4W 0.1% 4K99	5322 116 80854
R 6062	1/4W .25% 10K	5322 116 80232
R 6063	1/4W 0.1% 1K	5322 116 52698
R 6064	MRS25 1% 10E	4822 116 52891
R 6066	1/4W .25% 2K41	5322 116 80855
R 6067	1/4W 0.1% 3K32	5322 116 80866
R 6068	1/4W 0.1% 111E	5322 116 80865
R 6071	MRS25 1% 110E	4822 116 52906
R 6072	MRS25 1% 3K48	4822 116 53315
R 6073	MRS25 1% 237K	5322 116 80145
R 6074	MRS25 1% 1K78	5322 116 53208
R 6076	MRS25 1% 28K7	4822 116 53215
R 6077	MRS25 1% 3K48	4822 116 53315
R 6078	MRS25 1% 1K	4822 116 53108
R 6079	MRS25 1% 4K22	5322 116 53246
R 6081	MRS25 1% 1K	4822 116 53108
R 6082	MRS25 1% 6K81	5322 116 53252
R 6084	MRS25 1% 4K22	5322 116 53246
R 6086	MRS25 1% 38K3	4822 116 53526

POSNR	DESCRIPTION	ORDERING CODE
R 6087	MRS25 1% 1K	4822 116 53108
R 6088	MRS25 1% 7K5	4822 116 53028
R 6089	MRS25 1% 11K	4822 116 52907
R 6091	MRS25 1% 38K3	4822 116 53526
R 6092	MRS25 1% 5K11	5322 116 53494
R 6094	MRS25 1% 5K11	5322 116 53494
R 6096	0.3W 25% 10K	4822 105 10455
R 6103	MRS25 1% 2K61	5322 116 53327
R 6106	MRS25 1% 2K61	5322 116 53327
R 6107	MRS25 1% 7K5	4822 116 53028
R 6108	MRS25 1% 1K	4822 116 53108
R 6111	MRS25 1% 1K	4822 116 53108
R 6112	MRS25 1% 56K2	5322 116 53222
R 6113	MRS25 1% 3K16	4822 116 53021
R 6114	MRS25 1% 9K09	5322 116 53253
R 6116	MRS25 1% 511E	5322 116 53135
R 6117	MRS25 1% 6K19	5322 116 53263
R 6118	0.3W 25% 47K	5322 105 20036
R 6119	MRS25 1% 100K	4822 116 52973
R 6121	MRS25 1% 261E	5322 116 53549
R 6122	MRS25 1% 511E	5322 116 53135
R 6123	MRS25 1% 1K	4822 116 53108
R 6124	MRS25 1% 42K2	5322 116 53431
R 6126	MRS25 1% 2K15	5322 116 53239
R 6127	0.3W 25% 1K	5322 105 20032
R 6128	MRS25 1% 8K25	5322 116 53267
R 6129	MRS25 1% 5K11	5322 116 53494
R 6132	MRS25 1% 3K16	4822 116 53021
R 6133	MRS25 1% 100K	4822 116 52973
R 6136	MRS25 1% 100K	4822 116 52973
R 6139	MRS25 1% 10K	4822 116 53022
R 6141	MRS25 1% 10K	4822 116 53022
R 6142	MRS25 1% 10K	4822 116 53022
R 6143	MRS25 1% 5K11	5322 116 53494
R 6144	MRS25 1% 1K78	5322 116 53208
R 6146	MRS25 1% 10E	4822 116 52891
R 6147	MRS25 1% 10K	4822 116 53022
R 6148	MRS25 1% 10E	4822 116 52891
R 6149	MRS25 1% 10K	4822 116 53022
R 6151	MRS25 1% 10K	4822 116 53022
R 6152	MRS25 1% 10K	4822 116 53022
R 6153	MRS25 1% 10E	4822 116 52891
R 6154	MRS25 1% 10K	4822 116 53022
R 6156	MRS25 1% 10E	4822 116 52891
R 6157	MRS25 1% 10K	4822 116 53022
R 6158	MRS25 1% 10K	4822 116 53022
R 6159	MRS25 1% 10K	4822 116 53022
R 6161	MRS25 1% 10E	4822 116 52891
R 6162	MRS25 1% 10E	4822 116 52891
R 6163	MRS25 1% 10E	4822 116 52891
R 6164	MRS25 1% 10E	4822 116 52891
R 6166	MRS25 1% 10E	4822 116 52891
R 6167	MRS25 1% 10E	4822 116 52891
R 6168	MRS25 1% 10E	4822 116 52891
R 6172	MRS25 1% 10K	4822 116 53022
R 6173	VR25 5% 2M7	4822 110 72198
R 7001	MRS25 1% 10K	4822 116 53022
R 7002	MRS25 1% 5K11	5322 116 53494
R 7003	0.3W 25% 470E	5322 105 20028
R 7004	MRS25 1% 10K	4822 116 53022
R 7005	MRS25 1% 2K15	5322 116 53239
R 7006	MRS25 1% 5K11	5322 116 53494
R 7007	MRS25 1% 19K6	5322 116 53258
R 7008	MRS25 1% 5K11	5322 116 53494
R 7009	MRS25 1% 2K15	5322 116 53239
R 7011	0.3W 25% 10K	4822 105 10455
R 7012	MRS25 1% 7K5	4822 116 53028
R 7013	MRS25 1% 26K1	5322 116 53261
R 7014	MRS25 1% 7K5	4822 116 53028
R 7015	MRS25 1% 10E	4822 116 52891
R 7015	MRS25 1% 26K1	5322 116 53261
R 7016	0.3W 25% 10K	4822 105 10455
R 7017	0.3W 25% 2M2	5322 100 20693
R 7018	MRS25 1% 11K	4822 116 52907
R 7019	0.3W 25% 2K2	5322 105 20033
R 7021	0.3W 25% 2K2	5322 105 20033
R 7022	MRS25 1% 1K47	5322 116 53185
R 7023	MRS25 1% 1K47	5322 116 53185
R 7024	MRS25 1% 31E6	5322 116 54964
R 7025	MRS25 1% 10E	4822 116 52891
R 7026	MRS25 1% 31E6	5322 116 54964
R 7028	MRS25 1% 100K	4822 116 52973
R 7029	MRS25 1% 100K	4822 116 52973
R 7030	MRS25 1% 10E	4822 116 52891
R 7031	MRS25 1% 100K	4822 116 52973
R 7032	MRS25 1% 31K6	5322 116 53262
R 7033	0.3W 25% 100K	5322 105 20038
R 7035	MRS25 1% 10E	4822 116 52891

SEMICONDUCTORS

POSNR	DESCRIPTION		ORDERING CODE
V 1	D18-190GH/129		5322 131 20205
V 0601	BFQ22S	PEL	5322 130 42031
V 0602	BFQ22S	PEL	5322 130 42031
V 0603	BC558B	PEL	4822 130 44197
V 0604	BFQ24	PEL	5322 130 41664
V 0606	BFQ24	PEL	5322 130 41664
V 0607	BFQ22S	PEL	5322 130 42031
V 0608	BFQ24	PEL	5322 130 41664
V 0609	BC558B	PEL	4822 130 44197
V 0611	BF199	PEL	4822 130 44154
V 0612	BC548C	PEL	4822 130 44196
V 0613	BZX79-C4V7	PEL	4822 130 34174
V 0614	BZX79-C4V7	PEL	4822 130 34174
V 0616	BZV46-C1V5	PEL	5322 130 34865
V 0617	BAW62	PEL	4822 130 30613
V 0618	BAW62	PEL	4822 130 30613
V 0619	BZX79-C5V1	PEL	4822 130 34233
V 0620	BZX79-C5V1	PEL	4822 130 34233
V 0621	BC558B	PEL	4822 130 44197
V 0622	BC548C	PEL	4822 130 44196
V 0623	BC548C	PEL	4822 130 44196
V 0624	BC558B	PEL	4822 130 44197
V 0626	BSV78	PEL	5322 130 44093
V 0901	BFR53	PEL	5322 130 61244
V 0902	BFR53	PEL	5322 130 61244
V 0903	BFR53	PEL	5322 130 61244
V 0904	5082-0830	H.P	5322 130 80949
V 0906	5082-0830	H.P	5322 130 80949
V 0907	BAT14-095D	SIE	5322 130 80951
V 0908	BAT14-095D	SIE	5322 130 80951
V 0911	BAT17	PEL	5322 130 31544
V 0912	BAT17	PEL	5322 130 31544
V 1308	BAT17	PEL	5322 130 31544
V 1311	BAV99	PEL	5322 130 34337
V 1312	BCW30	PEL	5322 130 44335
V 1313	BFT92R	PEL	5322 130 44713
V 1401	BSX20	PEL	4822 130 41705
V 1402	BSX20	PEL	4822 130 41705
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V 1702	BC548C	PEL	4822 130 44196
V 1703	BAW62	PEL	4822 130 30613
V 1704	BC548C	PEL	4822 130 44196
V 1706	BC548C	PEL	4822 130 44196
V 1707	BAT85	PEL	4822 130 31983
V 1708	BC558B	PEL	4822 130 44197
V 1709	BZX79-C3V9	PEL	4822 130 31981
V 1711	BC548C	PEL	4822 130 44196
V 1712	BD140	PEL	4822 130 40824
V 1713	BZX79-C3V9	PEL	4822 130 31981
V 1714	BAW62	PEL	4822 130 30613
V 1791	BAT85	PEL	4822 130 31983
V 1801	BAT85	PEL	4822 130 31983
V 1802	BAT85	PEL	4822 130 31983
V 2001	BSX20	PEL	4822 130 41705
V 2002	BSX20	PEL	4822 130 41705
V 2201	BC558B	PEL	4822 130 44197
V 2202	BC558B	PEL	4822 130 44197
V 2203	BAW62	PEL	4822 130 30613
V 2204	BC548C	PEL	4822 130 44196
V 2205	BAT85	PEL	4822 130 31983
V 2206	BC558B	PEL	4822 130 44197
V 2207	BC558B	PEL	4822 130 44197
V 2208	BAW62	PEL	4822 130 30613
V 2209	BAW62	PEL	4822 130 30613
V 2211	BC548C	PEL	4822 130 44196
V 2212	BAT85	PEL	4822 130 31983
V 2213	BAT85	PEL	4822 130 31983
V 2301	BC558B	PEL	4822 130 44197
V 2302	BC558B	PEL	4822 130 44197
V 2303	ON4057	PEL	5322 130 42366
V 2304	BC548C	PEL	4822 130 44196
V 2306	BSX20	PEL	4822 130 41705
V 2307	BC548C	PEL	4822 130 44196
V 2308	BSX20	PEL	4822 130 41705
V 2309	BC558B	PEL	4822 130 44197
V 2311	BC558B	PEL	4822 130 44197
V 2312	BZX79-C4V3	PEL	4822 130 31554
V 2317	ON4057	PEL	5322 130 42366
V 2318	BC548C	PEL	4822 130 44196
V 2321	BC548C	PEL	4822 130 44196
V 2323	BZV12	PEL	5322 130 34269
V 2501	BAW62	PEL	4822 130 30613
V 2502	BAW62	PEL	4822 130 30613
V 2503	BAW62	PEL	4822 130 30613
V 2506	BAW62	PEL	4822 130 30613
V 2507	BC548C	PEL	4822 130 44196

POSNR	DESCRIPTION		ORDERING CODE
V 2508	BC558B	PEL	4822 130 44197
V 2509	BC548C	PEL	4822 130 44196
V 2511	BF199	PEL	4822 130 44154
V 2512	BF199	PEL	4822 130 44154
V 2513	BZV46-C1V5	PEL	5322 130 34865
V 2514	BZV46-C1V5	PEL	5322 130 34865
V 2516	BF199	PEL	4822 130 44154
V 2517	BF199	PEL	4822 130 44154
V 2521	BAW62	PEL	4822 130 30613
V 2522	BAW62	PEL	4822 130 30613
V 2523	BAW62	PEL	4822 130 30613
V 2524	BC548C	PEL	4822 130 44196
V 2526	BC558B	PEL	4822 130 44197
V 2527	BC548C	PEL	4822 130 44196
V 2528	BF422	PEL	4822 130 41782
V 2529	BF422	PEL	4822 130 41782
V 2531	BZV46-C1V5	PEL	5322 130 34865
V 2532	BZV46-C1V5	PEL	5322 130 34865
V 2533	BF422	PEL	4822 130 41782
V 2534	BF422	PEL	4822 130 41782
V 2535	BC558B	PEL	4822 130 44197
V 2601	BAW62	PEL	4822 130 30613
V 2602	BAW62	PEL	4822 130 30613
V 2604	BZV46-C1V5	PEL	5322 130 34865
V 2605	BAW62	PEL	4822 130 30613
V 2606	BF199	PEL	4822 130 44154
V 2607	BC548C	PEL	4822 130 44196
V 2608	BSX20	PEL	4822 130 41705
V 2609	BZV46-C1V5	PEL	5322 130 34865
V 2611	BC548C	PEL	4822 130 44196
V 2613	BC558B	PEL	4822 130 44197
V 2616	BZX79-C3V9	PEL	4822 130 31981
V 2623	BC558B	PEL	4822 130 44197
V 2626	BC558B	PEL	4822 130 44197
V 2627	BF199	PEL	4822 130 44154
V 2628	BSX20	PEL	4822 130 41705
V 2631	BF450	PEL	4822 130 44237
V 2632	BAT82	PEL	4822 130 32964
V 2633	BAT82	PEL	4822 130 32964
V 2634	BF450	PEL	4822 130 44237
V 2636	BF450	PEL	4822 130 44237
V 2637	BAT82	PEL	4822 130 32964
V 2638	BAT82	PEL	4822 130 32964
V 2639	BF450	PEL	4822 130 44237
V 2646	BF423	PEL	4822 130 41646
V 2647	BAV21	PEL	4822 130 30842
V 2648	BAV21	PEL	4822 130 30842
V 2649	BF423	PEL	4822 130 41646
V 2651	BF423	PEL	4822 130 41646
V 2652	BAV21	PEL	4822 130 30842
V 2653	BAV21	PEL	4822 130 30842
V 2654	BF423	PEL	4822 130 41646
V 2662	BC548C	PEL	4822 130 44196
V 2663	BC558B	PEL	4822 130 44197
V 2664	BZX79-C4V7	PEL	4822 130 34174
V 2666	BZX79-C4V7	PEL	4822 130 34174
V 2671	BAT82	PEL	4822 130 32964
V 2674	BC548C	PEL	4822 130 44196
V 2676	BC548C	PEL	4822 130 44196
V 2677	BC548C	PEL	4822 130 44196
V 2679	BD435	PEL	5322 130 50405
V 2681	BZX79-C33	PEL	4822 130 34142
V 2801	BF422	PEL	4822 130 41782
V 2802	BF422	PEL	4822 130 41782
V 2803	BF423	PEL	4822 130 41646
V 2804	BAV21	PEL	4822 130 30842
V 2806	BAV21	PEL	4822 130 30842
V 2807	BZX79-C7V5	PEL	4822 130 30861
V 2808	BF422	PEL	4822 130 41782
V 2809	BF422	PEL	4822 130 41782
V 2816	BF423	PEL	4822 130 41646
V 2817	BF423	PEL	4822 130 41646
V 2818	BF423	PEL	4822 130 41646
V 2819	BF423	PEL	4822 130 41646
V 2821	BAW62	PEL	4822 130 30613
V 2822	BAV21	PEL	4822 130 30842
V 3001	BC548C	PEL	4822 130 44196
V 3002	BC558B	PEL	4822 130 44197
V 3003	BD140	PEL	4822 130 40824
V 3101	BAW62	PEL	4822 130 30613
V 3103	BC558B	PEL	4822 130 44197
V 3104	BZV46-C2V0	PEL	4822 130 31248
V 3106	BZV46-C2V0	PEL	4822 130 31248
V 3107	BZV46-C2V0	PEL	4822 130 31248
V 3108	BZV46-C2V0	PEL	4822 130 31248
V 3109	BZV46-C2V0	PEL	4822 130 31248
V 3111	BZV46-C2V0	PEL	4822 130 31248
V 3112	BZV12	PEL	5322 130 34269
V 3113	BAW62	PEL	4822 130 30613
V 3114	BZV12	PEL	5322 130 34269

POSNR	DESCRIPTION		ORDERING CODE
V 3116	BAW62	PEL	4822 130 30613
V 3117	BC548C	PEL	4822 130 44196
V 3118	BC548C	PEL	4822 130 44196
V 3119	BCY88	PEL	5322 130 41805
V 3121	BC558B	PEL	4822 130 44197
V 3122	BC558B	PEL	4822 130 44197
V 3123	BC558B	PEL	4822 130 44197
V 3124	BCY88	PEL	5322 130 41805
V 3126	BC558B	PEL	4822 130 44197
V 3127	BC558B	PEL	4822 130 44197
V 3128	BC558B	PEL	4822 130 44197
V 3301	BZV12	PEL	5322 130 34269
V 3302	BZV46-C2V0	PEL	4822 130 31248
V 3304	BZV46-C2V0	PEL	4822 130 31248
V 3307	BAW62	PEL	4822 130 30613
V 3308	BZV12	PEL	5322 130 34269
V 3309	BAW62	PEL	4822 130 30613
V 3310	BAW62	PEL	4822 130 30613
V 3312	BF324	PEL	4822 130 41448
V 3314	BSX20	PEL	4822 130 41705
V 3316	BC548C	PEL	4822 130 44196
V 3317	BC558B	PEL	4822 130 44197
V 3318	BF410C	PEL	4822 130 41482
V 3319	BC548C	PEL	4822 130 44196
V 3320	BC548C	PEL	4822 130 44196
V 3321	BC548C	PEL	4822 130 44196
V 3323	BC558B	PEL	4822 130 44197
V 3324	BC558B	PEL	4822 130 44197
V 3325	BC548C	PEL	4822 130 44196
V 3326	BC548C	PEL	4822 130 44196
V 3327	BC548C	PEL	4822 130 44196
V 3328	BC548C	PEL	4822 130 44196
V 3501	BCW33R	PEL	5322 130 44342
V 3503	BFT92R	PEL	5322 130 44713
V 3504	BFT92R	PEL	5322 130 44713
V 3505	BFR92R	PEL	5322 130 44606
V 3506	BCW30R	PEL	5322 130 44341
V 3507	BCW30R	PEL	5322 130 44341
V 3508	BFR92R	PEL	5322 130 44606
V 3509	BFR92R	PEL	5322 130 44606
V 3511	BCW33	PEL	5322 130 44337
V 3512	BF512	PEL	5322 130 44875
V 3513	BCW33	PEL	5322 130 44337
V 3514	BCW33R	PEL	5322 130 44342
V 3516	BFR92A	PEL	5322 130 60647
V 3517	BFT92R	PEL	5322 130 44713
V 3518	BFT92	PEL	5322 130 44711
V 3519	BFR92R	PEL	5322 130 44606
V 3520	BAV99	PEL	5322 130 34337
V 3521	BFR92	PEL	5322 130 42145
V 3522	BFR92R	PEL	5322 130 44606
V 3523	BFR92	PEL	5322 130 42145
V 3524	BFR92	PEL	5322 130 42145
V 3526	BFR92R	PEL	5322 130 44606
V 3527	BFR92	PEL	5322 130 42145
V 3528	BFT92R	PEL	5322 130 44713
V 3529	BFT92	PEL	5322 130 44711
V 3530	BFT92R	PEL	5322 130 44713
V 3531	BFT92R	PEL	5322 130 44713
V 3532	BAV99	PEL	5322 130 34337
V 3533	BCW33R	PEL	5322 130 44342
V 3534	BCW33	PEL	5322 130 44337
V 3535	BCW30	PEL	5322 130 44335
V 3536	BFR92R	PEL	5322 130 44606
V 3537	BFR92	PEL	5322 130 42145
V 3538	BFR92	PEL	5322 130 42145
V 3539	BFR92R	PEL	5322 130 44606
V 3541	BFR92	PEL	5322 130 42145
V 3542	BFR92R	PEL	5322 130 44606
V 3543	BFT92R	PEL	5322 130 44713
V 3544	BFT92	PEL	5322 130 44711
V 3546	BFT92R	PEL	5322 130 44713
V 3547	BFT92	PEL	5322 130 44711
V 3547	BAT82	PEL	4822 130 32964
V 3548	BCW33R	PEL	5322 130 44342
V 3548	BAT82	PEL	4822 130 32964
V 3549	BAT74	PEL	5322 130 80948
V 3552	BA483	PEL	4822 130 32656
V 3559	BAV99	PEL	5322 130 34337
V 3561	BAT82	PEL	4822 130 32964
V 3562	BAT82	PEL	4822 130 32964
V 3564	BCW30	PEL	5322 130 44335
V 3566	BAV99	PEL	5322 130 34337
V 3568	BFT92R	PEL	5322 130 44713
V 3569	BFT92R	PEL	5322 130 44713
V 3701	BZV46-C1V5	PEL	5322 130 34865
V 3702	BAT82	PEL	4822 130 32964
V 3703	BSX20	PEL	4822 130 41705
V 3704	BSX20	PEL	4822 130 41705
V 3706	BAT82	PEL	4822 130 32964

POSNR	DESCRIPTION		ORDERING CODE
V 3707	BAT82	PEL	4822 130 32964
V 3708	BAT82	PEL	4822 130 32964
V 3709	BAT82	PEL	4822 130 32964
V 3711	BAT82	PEL	4822 130 32964
V 4201	BAW62	PEL	4822 130 30613
V 4202	BAW62	PEL	4822 130 30613
V 4203	BAW62	PEL	4822 130 30613
V 4204	BAW62	PEL	4822 130 30613
V 4206	BAW62	PEL	4822 130 30613
V 4207	BAW62	PEL	4822 130 30613
V 4208	BAW62	PEL	4822 130 30613
V 4209	BAW62	PEL	4822 130 30613
V 4211	BAW62	PEL	4822 130 30613
V 4212	BAW62	PEL	4822 130 30613
V 4213	BAW62	PEL	4822 130 30613
V 4214	BAW62	PEL	4822 130 30613
V 4216	BAW62	PEL	4822 130 30613
V 4217	BAW62	PEL	4822 130 30613
V 4218	BAW62	PEL	4822 130 30613
V 4219	BAW62	PEL	4822 130 30613
V 4221	BAW62	PEL	4822 130 30613
V 4222	BAW62	PEL	4822 130 30613
V 4223	BAW62	PEL	4822 130 30613
V 4224	BAW62	PEL	4822 130 30613
V 4226	BAW62	PEL	4822 130 30613
V 4227	BAW62	PEL	4822 130 30613
V 4228	BAW62	PEL	4822 130 30613
V 4229	BAW62	PEL	4822 130 30613
V 4231	BAW62	PEL	4822 130 30613
V 4232	BAW62	PEL	4822 130 30613
V 4233	BAW62	PEL	4822 130 30613
V 4234	BAW62	PEL	4822 130 30613
V 4236	BAW62	PEL	4822 130 30613
V 4237	BAW62	PEL	4822 130 30613
V 4238	BAW62	PEL	4822 130 30613
V 4239	BAW62	PEL	4822 130 30613
V 4241	BAW62	PEL	4822 130 30613
V 4242	BAW62	PEL	4822 130 30613
V 4243	BAW62	PEL	4822 130 30613
V 4244	BAW62	PEL	4822 130 30613
V 4246	BAW62	PEL	4822 130 30613
V 4247	BAW62	PEL	4822 130 30613
V 4248	BAW62	PEL	4822 130 30613
V 4249	BAW62	PEL	4822 130 30613
V 4251	BAW62	PEL	4822 130 30613
V 4252	BAW62	PEL	4822 130 30613
V 4253	BAW62	PEL	4822 130 30613
V 4254	BAW62	PEL	4822 130 30613
V 4256	BAW62	PEL	4822 130 30613
V 4257	BAW62	PEL	4822 130 30613
V 4258	BAW62	PEL	4822 130 30613
V 4401	BYM56E	PEL	4822 130 60254
V 4402	BYM56E	PEL	4822 130 60254
V 4403	BYM56E	PEL	4822 130 60254
V 4404	BYM56E	PEL	4822 130 60254
V 4406	BF423	PEL	4822 130 41646
V 4407	BF423	PEL	4822 130 41646
V 4408	BF423	PEL	4822 130 41646
V 4409	BZX79-C15	PEL	4822 130 34281
V 4411	BYW56	PEL	5322 130 34973
V 4412	BYW56	PEL	5322 130 34973
V 4413	BT151-500R	PEL	5322 130 24081
V 4414	BT149-E	PEL	5322 130 80268
V 4416	BT149-E	PEL	5322 130 80268
V 4417	BT151-500R	PEL	5322 130 24081
V 4418	BYV26C	PEL	4822 130 32343
V 4419	BYV28-150	PEL	5322 130 32043
V 4422	BYV26C	PEL	4822 130 32343
V 4423	BYV26C	PEL	4822 130 32343
V 4424	BUZ41A	PEL	5322 130 60065
V 4426	BUZ41A	PEL	5322 130 60065
V 4427	BZX79-C15	PEL	4822 130 34281
V 4428	BYV26C	PEL	4822 130 32343
V 4429	BUW13A	PEL	5322 130 42047
V 4431	BYV27-150	PEL	4822 130 31628
V 4433	BC337	PEL	4822 130 40855
V 4434	BAX12	PEL	5322 130 34605
V 4436	BZX79-C3V6	PEL	5322 130 34834
V 4437	BAX12	PEL	5322 130 34605
V 4438	BAX12	PEL	5322 130 34605
V 4439	BZX79-C15	PEL	4822 130 34281
V 4441	BRY39	PEL	5322 130 40482
V 4442	BAX12	PEL	5322 130 34605
V 4443	BZX79-C5V6	PEL	4822 130 34173
V 4444	BZT03-C220	PEL	5322 130 80269
V 4446	BZT03-C220	PEL	5322 130 80269
V 4447	BYV43-45	PEL	5322 130 33656
V 4448	BYV43-45	PEL	5322 130 33656
V 4449	BYV95C	PEL	4822 130 41487
V 4451	BYV95C	PEL	4822 130 41487

POSNR	DESCRIPTION		ORDERING CODE
V 4452	BYV95C	PEL	4822 130 41487
V 4453	BYV95C	PEL	4822 130 41487
V 4454	BYV95C	PEL	4822 130 41487
V 4455	BYV19-45	PEL	5322 130 32703
V 4456	BYV19-45	PEL	5322 130 32703
V 4457	BYV19-45	PEL	5322 130 32703
V 4459	BAX12 DO-35	PEL	5322 130 34605
V 4461	BYV28-150	PEL	5322 130 32043
V 4462	BYV28-150	PEL	5322 130 32043
V 4463	BYV28-150	PEL	5322 130 32043
V 4464	BYV28-150	PEL	5322 130 32043
V 4466	BYV95C	PEL	4822 130 41487
V 4467	BYV95C	PEL	4822 130 41487
V 4468	BYV95C	PEL	4822 130 41487
V 4469	BYV95C	PEL	4822 130 41487
V 4471	BZX79-C7V5	PEL	4822 130 30861
V 4472	BAX12	PEL	5322 130 34605
V 4473	BC548C	PEL	4822 130 44196
V 4474	BC327	PEL	4822 130 40854
V 4476	BC548C	PEL	4822 130 44196
V 4477	BAX12	PEL	5322 130 34605
V 4478	BZX79-C5V1	PEL	4822 130 34233
V 4479	BZX79-C15	PEL	4822 130 34281
V 4481	BAX12	PEL	5322 130 34605
V 4482	BZX79-C9V1	PEL	4822 130 30862
V 4483	BAX12	PEL	5322 130 34605
V 4484	BAX12	PEL	5322 130 34605
V 4485	BC327	PEL	4822 130 40854
V 4491	BZV12	PEL	5322 130 34269
V 4492	BAX12	PEL	5322 130 34605
V 4494	BC337	PEL	4822 130 40855
V 4495	BZX79-C22	PEL	4822 130 34441
V 4496	BAV21	PEL	4822 130 30842
V 4497	BAV21	PEL	4822 130 30842
V 4498	BC327	PEL	4822 130 40854
V 4499	BAV21	PEL	4822 130 30842
V 4511	BYV27-150	PEL	4822 130 31628
V 4512	BUV26A	PEL	5322 130 42722
V 4513	BY509	PEL	4822 130 41485
V 4516	BAX12	PEL	5322 130 34605
V 4517	BSV78	PEL	5322 130 44093
V 4518	BZX79-C22	PEL	4822 130 34441
V 4519	BAX12	PEL	5322 130 34605
V 4521	BC639	PEL	4822 130 41053
V 4522	BC639	PEL	4822 130 41053
V 4523	BZX79-C27	PEL	4822 130 34379
V 4524	BAX12	PEL	5322 130 34605
V 5001	BZV12	PEL	5322 130 34269
V 5002	BFW11	PEL	4822 130 40408
V 5005	BC549C	PEL	4822 130 44246
V 5006	BC559B	PEL	4822 130 44358
V 5008	BC559B	PEL	4822 130 44358
V 5009	BF494	PEL	4822 130 44195
V 5010	BC559B	PEL	4822 130 44358
V 5011	BZV12	PEL	5322 130 34269
V 5014	BAW62	PEL	4822 130 30613
V 5016	BC559B	PEL	4822 130 44358
V 5017	BSV78	PEL	5322 130 44093
V 5018	BSV78	PEL	5322 130 44093
V 5021	BF494	PEL	4822 130 44195
V 5023	BSV78	PEL	5322 130 44093
V 5025	BSV78	PEL	5322 130 44093
V 5026	BC559B	PEL	4822 130 44358
V 5028	BZV46-C2V0	PEL	4822 130 31248
V 5027	BAW62	PEL	4822 130 30613
V 5028	BZV46-C2V0	PEL	4822 130 31248
V 5029	BAW62	PEL	4822 130 30613
V 5031	BSV78	PEL	5322 130 44093
V 5032	BZX79-C8V2	PEL	4822 130 34382
V 5033	BC549C	PEL	4822 130 44246
V 5034	BC559B	PEL	4822 130 44358
V 5036	BC549C	PEL	4822 130 44246
V 5043	BZV12	PEL	5322 130 34269
V 5044	BC549C	PEL	4822 130 44246
V 5046	BC549C	PEL	4822 130 44246
V 5047	BAT85	PEL	4822 130 31983
V 5201	BFR92	PEL	5322 130 42145
V 5202	BFR92R	PEL	5322 130 44606
V 5203	BFR92	PEL	5322 130 42145
V 5204	BFR92R	PEL	5322 130 44606
V 5206	BFR92R	PEL	5322 130 44606
V 5207	BFR92R	PEL	5322 130 44606
V 5208	BFR92R	PEL	5322 130 44606
V 5209	BFT92	PEL	5322 130 44711
V 5211	BFT92R	PEL	5322 130 44713
V 5212	BFT92	PEL	5322 130 44711
V 5213	BFT92	PEL	5322 130 44711
V 5214	BFR92R	PEL	5322 130 44606
V 5216	BFR92	PEL	5322 130 42145
V 5217	BFR92	PEL	5322 130 42145

POSNR	DESCRIPTION		ORDERING CODE
V 5218	BFR92R	PEL	5322 130 44606
V 5219	BFR92R	PEL	5322 130 44606
V 5220	BFR92R	PEL	5322 130 44606
V 5221	BFR92R	PEL	5322 130 44606
V 5222	BFT92	PEL	5322 130 44711
V 5223	BFT92R	PEL	5322 130 44713
V 5224	BFT92	PEL	5322 130 44711
V 5226	BFT92	PEL	5322 130 44711
V 5227	BFR92R	PEL	5322 130 44606
V 5228	BFR92	PEL	5322 130 42145
V 5229	BFR92	PEL	5322 130 42145
V 5231	BFR92R	PEL	5322 130 44606
V 5232	BFR92R	PEL	5322 130 44606
V 5233	BFR92R	PEL	5322 130 44606
V 5234	BFR92R	PEL	5322 130 44606
V 5236	BFT92	PEL	5322 130 44711
V 5237	BFT92R	PEL	5322 130 44713
V 5238	BFR92R	PEL	5322 130 44606
V 5239	BFR92R	PEL	5322 130 44606
V 5241	BCW30	PEL	5322 130 44335
V 5242	BFR92	PEL	5322 130 42145
V 5243	BAV99	PEL	5322 130 34337
V 5244	BZX84-C3V0	PEL	5322 130 32739
V 5246	BZX84-C5V1	PEL	5322 130 32835
V 5247	BZX84-C5V1	PEL	5322 130 32835
V 5248	BCW30R	PEL	5322 130 44341
V 5249	BFR92	PEL	5322 130 42145
V 5251	BZX84-C3V0	PEL	5322 130 32739
V 5252	BCW33	PEL	5322 130 44337
V 5253	BCW33R	PEL	5322 130 44342
V 5254	BAV99	PEL	5322 130 34337
V 5255	BZX84-C4V7	PEL	5322 130 31937
V 5256	BCW30	PEL	5322 130 44335
V 5257	BAT17	PEL	5322 130 31544
V 5258	BAT17	PEL	5322 130 31544
V 5259	BAT17	PEL	5322 130 31544
V 5261	BCW30	PEL	5322 130 44335
V 5496	BFT92	PEL	5322 130 44711
V 5498	BFT92R	PEL	5322 130 44713
V 6001	BZV12	PEL	5322 130 34269
V 6002	BFW11	PEL	4822 130 40408
V 6003	BC549C	PEL	4822 130 44246
V 6004	BC559B	PEL	4822 130 44358
V 6006	BC559B	PEL	4822 130 44358
V 6007	BF494	PEL	4822 130 44195
V 6008	BC559B	PEL	4822 130 44358
V 6013	BZV12	PEL	5322 130 34269
V 6014	BAW62	PEL	4822 130 30613
V 6016	BC559B	PEL	4822 130 44358
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V 6018	BSV78	PEL	5322 130 44093
V 6021	BF494	PEL	4822 130 44195
V 6022	BSV78	PEL	5322 130 44093
V 6023	BSV78	PEL	5322 130 44093
V 6024	BC559B	PEL	4822 130 44358
V 6026	BZV46-C2V0	PEL	4822 130 31248
V 6027	BAW62	PEL	4822 130 30613
V 6028	BZV46-C2V0	PEL	4822 130 31248
V 6029	BAW62	PEL	4822 130 30613
V 6031	BSV78	PEL	5322 130 44093
V 6032	BZX79-C8V2	PEL	4822 130 34382
V 6033	BC549C	PEL	4822 130 44246
V 6034	BC559B	PEL	4822 130 44358
V 6036	BC549C	PEL	4822 130 44246
V 6043	BZV12	PEL	5322 130 34269
V 6044	BC549C	PEL	4822 130 44246
V 6046	BC549C	PEL	4822 130 44246
V 6047	BAT85	PEL	4822 130 31983
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V 7002	BAW62	PEL	4822 130 30613
V 7003	BC549C	PEL	4822 130 44246
V 7004	BC549C	PEL	4822 130 44246
V 7006	BF422	PEL	4822 130 41782
V 7007	BF422	PEL	4822 130 41782
V 7008	BZX79-C6V8	PEL	4822 130 34278
V 7009	BZV12	PEL	5322 130 34269
V 7011	BZV12	PEL	5322 130 34269

INTEGRATED CIRCUITS

D 0603	N74LS266N	SIG	5322 209 86163
D 0604	PC74HCT374P	PEL	5322 209 11119
D 0606	PC74HCT374P	PEL	5322 209 11119
D 0607	74F08PC	FSC	5322 209 81574
D 0608	PC74HCT74P	PEL	5322 209 11109
D 0609	PC74HCT74P	PEL	5322 209 11109
D 0611	PC74HCT161P	PEL	5322 209 11476
D 0612	ARRAY OQ 0127		5322 209 80992
D 0614	PC74HCT04P	PEL	4822 209 82341
D 1201	PC74HCT04P	PEL	4822 209 82341
D 1202	PC74HCT11P	PEL	4822 209 11427
D 1203	PC74HCT245P	PEL	5322 209 11117
D 1204	PC74HCT243P	PEL	5322 209 11474
D 1206	PC74HCT243P	PEL	5322 209 11474
D 1207	PC74HCT373P	PEL	5322 209 11118
D 1208	PC74HCT373P	PEL	5322 209 11118
D 1209	74F08PC	FSC	5322 209 81574
D 1211	PC74HCT86P	PEL	5322 209 11473
D 1212	PC74HCT86P	PEL	5322 209 11473
D 1213	PC74HCT86P	PEL	5322 209 11473
D 1214	PC74HCT86P	PEL	5322 209 11473
D 1216	PC74HCT273P	PEL	5322 209 11485
D 1217	PC74HCT273P	PEL	5322 209 11485
D 1218	74F283PC	FSC	5322 209 81588
D 1219	74F283PC	FSC	5322 209 81588
D 1221	74F283PC	FSC	5322 209 81588
D 1222	74F283PC	FSC	5322 209 81588
D 1223	74F86PC	FSC	5322 209 81539
D 1224	PC74HCT374P	PEL	5322 209 11119
D 1226	PC74HCT374P	PEL	5322 209 11119
D 1227	74F32PC	FSC	4822 209 82133
D 1228	74F00PC	FSC	5322 209 81534
D 1229	74F32PC	FSC	4822 209 82133
D 1231	74F74PC	FSC	5322 209 81474
D 1232	PC74HCT157P	PEL	5322 209 11263
D 1233	74F175PC	FSC	5322 209 81542
D 1234	74F257APC	FSC	5322 209 71672
D 1236	PC74HCT257P	PEL	5322 209 11114
D 1237	PC74HCT257P	PEL	5322 209 11114
D 1238	PC74HCT257P	PEL	5322 209 11114
D 1239	PC74HCT257P	PEL	5322 209 11114
D 1241	PC74HCT257P	PEL	5322 209 11114
D 1242	PC74HCT299P	PEL	5322 209 11486
D 1243	PC74HCT299P	PEL	5322 209 11486
D 1244	PC74HCT04P	PEL	4822 209 82341
D 1246	PC74HCT04P	PEL	4822 209 82341
D 1247	PC74HCT30P	PEL	5322 209 11492
D 1248	PC74HCT30P	PEL	5322 209 11492
D 1249	HM6264P-10	HIT	5322 209 83327
D 1251	HM6264P-10	HIT	5322 209 83327
D 1252	D2147H	INT	5322 209 11495
D 1253	D2147H	INT	5322 209 11495
D 1254	74F139PC	FSC	5322 209 82234
D 1301	U862BS	AEG	5322 209 73381
D 1302	U664B	AEG	5322 209 73379
D 1401	PC74HCT138P	PEL	5322 209 11111
D 1402	74F251APC	FSC	5322 209 71656
D 1403	74F251APC	FSC	5322 209 71656
D 1404	PC74HCT11P	PEL	4822 209 11427
D 1406	74F04PC	FSC	5322 209 81577
D 1407	74F08PC	FSC	5322 209 81574
D 1408	SN74LS38N	T.I	5322 209 85605
D 1409	74F257APC	FSC	5322 209 71672
D 1411	74F257APC	FSC	5322 209 71672
D 1412	74F257APC	FSC	5322 209 71672
D 1413	PC74HCT541P	PEL	5322 209 11487
D 1414	PC74HCT541P	PEL	5322 209 11487
D 1416	PC74HCT541P	PEL	5322 209 11487
D 1417	PC74HCT541P	PEL	5322 209 11487
D 1418	74F574PC	FSC	5322 209 72659
D 1419	PC74HCT574P	PEL	5322 209 11489
D 1421	PC74HCT574P	PEL	5322 209 11489
D 1422	PC74HCT173P	PEL	5322 209 11477
D 1423	SN74LS125AN	T.I	5322 209 81569
D 1424	74F74PC	FSC	5322 209 81474
D 1426	TMM2016AP-90		5322 209 71653
D 1427	TMM2016AP-90		5322 209 71653
D 1428	TMM2016AP-90		5322 209 71653
D 1429	TMM2016AP-90		5322 209 71653
D 1431	74F574PC	FSC	5322 209 72659
D 1432	74F574PC	FSC	5322 209 72659
D 1433	74F574PC	FSC	5322 209 72659
D 1434	74F574PC	FSC	5322 209 72659
D 1436	74F574PC	FSC	5322 209 72659
D 1437	74F174PC	FSC	5322 209 83326
D 1438	74F174PC	FSC	5322 209 83326
D 1439	74F174PC	FSC	5322 209 83326
D 1441	74F174PC	FSC	5322 209 83326
D 1442	74F174PC	FSC	5322 209 83326
D 1443	PC74HCT174P	PEL	5322 209 11478
D 1444	PC74HCT174P	PEL	5322 209 11478
D 1446	74F283PC	FSC	5322 209 81588
D 1447	74F283PC	FSC	5322 209 81588
D 1448	74F283PC	FSC	5322 209 81588
D 1449	PC74HCT257P	PEL	5322 209 11114
D 1451	PC74HCT257P	PEL	5322 209 11114
D 1452	PC74HCT257P	PEL	5322 209 11114
D 1453	PC74HCT191P	PEL	5322 209 11481
D 1454	PC74HCT191P	PEL	5322 209 11481
D 1456	PC74HCT191P	PEL	5322 209 11481

POSNR	DESCRIPTION		ORDERING CODE
D 1457	FPLS		5322 209 51456
D 1458	74F175PC	FSC	5322 209 81542
D 1459	74F175PC	FSC	5322 209 81542
D 1461	74F32PC	FSC	4822 209 82133
D 1702	74F04PC	FSC	5322 209 81577
D 1703	PC74HCT393P	PEL	4822 209 83045
D 1704	74F74PC	FSC	5322 209 81474
D 1706	PC74HCT390P	PEL	5322 209 11483
D 1707	PC74HCT390P	PEL	5322 209 11483
D 1708	SN74LS148N	T.I	4822 209 80452
D 1709	PC74HCT123P	PEL	5322 209 11379
D 1712	PC74HCT132P	PEL	4822 209 83044
D 1713	PC74HCT175P	PEL	5322 209 11479
D 1714	SN74LS05N	T.I	5322 209 84994
D 1716	PC74HCT03P	PEL	5322 209 11316
D 1717	MC68000RC8	MOT	5322 209 71666
D 1718	SN74LS541N	T.I	5322 209 71671
D 1719	SN74LS541N	T.I	5322 209 71671
D 1721	SN74LS541N	T.I	5322 209 71671
D 1722	SN74LS245N	T.I	5322 209 86225
D 1723	SN74LS245N	T.I	5322 209 86225
D 1729	PC74HCT04P	PEL	4822 209 82341
D 1731	C2606NQD	SIG	5322 209 84197
D 1732	PC74HCT32P	PEL	5322 209 11266
D 1733	PC74HCT00P	PEL	5322 209 11105
D 1734	PC74HCT08P	PEL	5322 209 11265
D 1736	PC74HCT74P	PEL	5322 209 11109
D 1737	PC74HCT10P	PEL	5322 209 11107
D 1738	PC74HCT32P	PEL	5322 209 11266
D 1739	PC74HCT32P	PEL	5322 209 11266
D 1741	PC74HCT139P	PEL	5322 209 11112
D 1742	PC74HCT02P	PEL	5322 209 11106
D 1743	PC74HCT30P	PEL	5322 209 11492
D 1744	PC74HCT138P	PEL	5322 209 11111
D 1746	SN74LS541N	T.I	5322 209 71671
D 1747	SN74LS541N	T.I	5322 209 71671
D 1751	PC74HCT164P	PEL	5322 209 11268
D 1801	PC74HCT4538P		4822 209 71585
D 1802	PC74HCT74P	PEL	5322 209 11109
D 1803	PC74HCT4538P		4822 209 71585
D 1804	PC74HCT4538P		4822 209 71585
D 1805	PC74HCT4538P		4822 209 71585
D 1806	PC74HCT4538P		4822 209 71585
D 1807	PC74HCT74P	PEL	5322 209 11109
D 1808	PC74HCT74P	PEL	5322 209 11109
D 1809	PC74HCT74P	PEL	5322 209 11109
D 1810	PC74HCT393P	PEL	4822 209 83045
D 1811	PC74HCT151P	PEL	5322 209 11442
D 1812	HEF4047BP	PEL	4822 209 10259
D 1813	PC74HCT193P	PEL	5322 209 11381
D 1814	TEA1017/N8	PEL	5322 209 70023
D 1815	PC74HCT02P	PEL	5322 209 11106
D 1816	PC74HCT00P	PEL	5322 209 11105
D 1817	PC74HCT00P	PEL	5322 209 11105
D 1818	PC74HCT02P	PEL	5322 209 11106
D 1819	N74LS02N	SIG	5322 209 85312
D 1820	PC74HCT74P	PEL	5322 209 11109
D 1823	SN74LS245N	T.I	5322 209 86225
D 1824	SN74LS245N	T.I	5322 209 86225
D 1826	PC74HCT574P	PEL	5322 209 11489
D 1827	PC74HCT574P	PEL	5322 209 11489
D 1828	PC74HCT573P	PEL	5322 209 11488
D 1829	PC74HCT32P	PEL	5322 209 11266
D 1831	PC74HCT32P	PEL	5322 209 11266
D 1832	SN74LS38N	T.I	5322 209 85605
D 1833	CD74HCT4066E	RC	5322 209 71655
D 1834	HM62256LP-12		5322 209 72129
D 1836	HM62256LP-12		5322 209 72129
D 1837	HM62256LP-12		5322 209 72129
D 1838	HM62256LP-12		5322 209 72129
D 1839	PC74HCT14P	PEL	5322 209 11378
D 2001	PC74HCT373P	PEL	5322 209 11118
D 2002	PC74HCT373P	PEL	5322 209 11118
D 2003	SN74LS652N	T.I	5322 209 71654
D 2004	SN74LS652N	T.I	5322 209 71654
D 2006	PC74HCT245P	PEL	5322 209 11117
D 2007	PC74HCT245P	PEL	5322 209 11117
D 2008	HM6264LP-15	HIT	5322 209 50671
D 2009	HM6264LP-15	HIT	5322 209 50671
D 2011	HM6264LP-15	HIT	5322 209 50671
D 2012	HM6264LP-15	HIT	5322 209 50671
D 2013	CD74HCT4066E	RC	5322 209 71655
D 2014	HM6264LP-15	HIT	5322 209 50671
D 2016	HM6264LP-15	HIT	5322 209 50671
D 2017	PC74HCT74P	PEL	5322 209 11109
D 2018	PC74HCT161P	PEL	5322 209 11476
D 2019	PC74HCT161P	PEL	5322 209 11476
D 2021	PC74HCT161P	PEL	5322 209 11476
D 2022	PC74HCT174P	PEL	5322 209 11478
D 2023	PC74HCT174P	PEL	5322 209 11478

POSNR	DESCRIPTION		ORDERING CODE
D 2024	PC74HCT85P	PEL	5322 209 11484
D 2026	PC74HCT85P	PEL	5322 209 11484
D 2027	PC74HCT85P	PEL	5322 209 11484
D 2028	PC74HCT374P	PEL	5322 209 11119
D 2029	PC74HCT374P	PEL	5322 209 11119
D 2031	PC74HCT374P	PEL	5322 209 11119
D 2032	PC74HCT374P	PEL	5322 209 11119
D 2033	PC74HCT173P	PEL	5322 209 11477
D 2034	PC74HCT374P	PEL	5322 209 11119
D 2036	PC74HCT374P	PEL	5322 209 11119
D 2037	74F257APC	FSC	5322 209 71672
D 2038	74F257APC	FSC	5322 209 71672
D 2039	74F257APC	FSC	5322 209 71672
D 2041	PC74HCT173P	PEL	5322 209 11477
D 2101	PC74HCT541P	PEL	5322 209 11487
D 2102	PC74HCT541P	PEL	5322 209 11487
D 2103	PC74HCT574P	PEL	5322 209 11489
D 2104	PC74HCT574P	PEL	5322 209 11489
D 2105	PC74HCT574P	PEL	5322 209 11489
D 2107	PC74HCT574P	PEL	5322 209 11489
D 2108	PC74HCT574P	PEL	5322 209 11489
D 2109	74F04PC	FSC	5322 209 81577
D 2111	PC74HCT191P	PEL	5322 209 11481
D 2112	PC74HCT191P	PEL	5322 209 11481
D 2113	PC74HCT191P	PEL	5322 209 11481
D 2114	PC74HCT109P	PEL	5322 209 11475
D 2115	PC74HCT74P	PEL	5322 209 11109
D 2116	PC74HCT02P	PEL	5322 209 11106
D 2118	PC74HCT257P	PEL	5322 209 11114
D 2119	PC74HCT08P	PEL	5322 209 11265
D 2121	PC74HCT244P	PEL	5322 209 11116
D 2122	PC74HCT244P	PEL	5322 209 11116
D 2123	PC74HCT244P	PEL	5322 209 11116
D 2124	PC74HCT244P	PEL	5322 209 11116
D 2126	P8254	INT	5322 209 82406
D 2127	PC74HCT123P	PEL	5322 209 11379
D 2128	SN74LS38N	T.I	5322 209 85605
D 2129	PC74HCT32P	PEL	5322 209 11266
D 2131	PC74HCT139P	PEL	5322 209 11112
D 2132	PC74HCT138P	PEL	5322 209 11111
D 2133	PC74HCT107P	PEL	5322 209 11108
D 2134	74F163APC	FSC	5322 209 83343
D 2135	74F04PC	FSC	5322 209 81577
D 2137	PC74HCT32P	PEL	5322 209 11266
D 2138	PC74HCT08P	PEL	5322 209 11265
D 2139	74F109PC	FSC	5322 209 81669
D 2140	74F109PC	FSC	5322 209 81669
D 2141	FPLS		5322 209 51452
D 2143	PC74HCT00P	PEL	5322 209 11105
D 2144	PC74HCT123P	PEL	5322 209 11379
D 2145	PC74HCT27P	PEL	5322 209 11472
D 2147	74F32PC	FSC	4822 209 82133
D 2148	74F74PC	FSC	5322 209 81474
D 2149	74F08PC	FSC	5322 209 81574
D 2151	FPLA		5322 209 51453
D 2152	74F32PC	FSC	4822 209 82133
D 2153	74F11PC	FSC	5322 209 81556
D 2154	74F00PC	FSC	5322 209 81574
D 2156	PC74HCT174P	PEL	5322 209 11478
D 2157	PC74HCT27P	PEL	5322 209 11472
D 2159	74F32PC	FSC	4822 209 82133
D 2201	PC74HCT00P	PEL	5322 209 11105
D 2202	PC74HCT4538P		4822 209 71585
D 2204	PC74HCT132P	PEL	4822 209 83044
D 2206	PC74HCT74P	PEL	5322 209 11109
D 2207	PC74HCT00P	PEL	5322 209 11105
D 2208	PC74HCT132P	PEL	4822 209 83044
D 2209	PC74HCT00P	PEL	5322 209 11105
D 2211	PC74HCT390P	PEL	5322 209 11483
D 2212	PC74HCT00P	PEL	5322 209 11105
D 2213	PC74HCT4538P		4822 209 71585
D 2214	PC74HCT4538P		4822 209 71585
D 2216	PC74HCT4538P		4822 209 71585
D 2217	PC74HCT74P	PEL	5322 209 11109
D 2218	PC74HCT74P	PEL	5322 209 11109
D 2219	PC74HCT74P	PEL	5322 209 11109
D 2221	PC74HCT00P	PEL	5322 209 11105
D 2222	TEA1017/N8	PEL	5322 209 70023
D 2301	FPLS		5322 209 51449
D 2302	FPLS		5322 209 51451
D 2303	PC74HCT244P	PEL	5322 209 11116
D 2304	PC74HCT244P	PEL	5322 209 11116
D 2306	PC74HCT257P	PEL	5322 209 11114
D 2307	PC74HCT257P	PEL	5322 209 11114
D 2308	PC74HCT257P	PEL	5322 209 11114
D 2309	PC74HCT175P	PEL	5322 209 11479
D 2311	PC74HCT257P	PEL	5322 209 11114
D 2312	PC74HCT257P	PEL	5322 209 11114
D 2313	PC74HCT257P	PEL	5322 209 11114
D 2314	PC74HCT574P	PEL	5322 209 11489

POSNR	DESCRIPTION	ORDERING CODE
D 2316	PC74HCT574P PEL	5322 209 11489
D 2317	PC74HCT574P PEL	5322 209 11489
D 2318	PC74HCT574P PEL	5322 209 11489
D 2319	PC74HCT283P PEL	5322 209 11493
D 2321	PC74HCT283P PEL	5322 209 11493
D 2322	PC74HCT283P PEL	5322 209 11493
D 2323	PC74HCT283P PEL	5322 209 11493
D 2324	PC74HCT283P PEL	5322 209 11493
D 2326	PC74HCT283P PEL	5322 209 11493
D 2327	PC74HCT283P PEL	5322 209 11493
D 2328	PC74HCT283P PEL	5322 209 11493
D 2329	PC74HCT174P PEL	5322 209 11478
D 2331	PC74HCT174P PEL	5322 209 11478
D 2332	PC74HCT574P PEL	5322 209 11489
D 2333	SN74LS298N T.I	5322 209 85937
D 2334	SN74LS298N T.I	5322 209 85937
D 2336	SN74LS298N T.I	5322 209 85937
D 2337	PC74HCT00P PEL	5322 209 11105
D 2338	PC74HCT27P PEL	5322 209 11472
D 2339	PC74HCT08P PEL	5322 209 11265
D 2341	PC74HCT4053P	4822 209 71584
D 2342	PC74HCT4053P	4822 209 71584
D 2343	PC74HCT4053P	4822 209 71584
D 2501	HEF4053BP PEL	5322 209 10576
D 2502	PC74HCT390P PEL	5322 209 11483
D 2503	PC74HCT74P PEL	5322 209 11109
D 2504	PC74HCT86P PEL	5322 209 11473
D 3101	SN74LS641N-1 T	5322 209 83215
D 3102	PC74HCT573P PEL	5322 209 11488
D 3103	PC74HCT541P PEL	5322 209 11487
D 3104	PC74HCT238P PEL	5322 209 11482
D 3106	PC74HCT238P PEL	5322 209 11482
D 3107	PC74HCT238P PEL	5322 209 11482
D 3108	PC74HCT74P PEL	5322 209 11109
D 3109	PC74HCT74P PEL	5322 209 11109
D 3111	PC74HCT74P PEL	5322 209 11109
D 3112	PC74HCT74P PEL	5322 209 11109
D 3113	PC74HCT74P PEL	5322 209 11109
D 3114	PC74HCT74P PEL	5322 209 11109
D 3116	PC74HCT74P PEL	5322 209 11109
D 3117	PC74HCT14P PEL	5322 209 11378
D 3119	PC74HCT32P PEL	5322 209 11266
D 3121	PC74HCT00P PEL	5322 209 11105
D 3122	PC74HCT574P PEL	5322 209 11489
D 3123	PC74HCT574P PEL	5322 209 11489
D 3124	PC74HCT574P PEL	5322 209 11489
D 3126	PC74HCT574P PEL	5322 209 11489
D 3142	TEA1017/N8 PEL	5322 209 70023
D 3144	TEA1017/N8 PEL	5322 209 70023
D 3301	PC74HCT14P PEL	5322 209 11378
D 3302	PC74HCT4040P PH	5322 209 72465
D 3304	TEA1017/N8 PEL	5322 209 70023
D 3701	PC74HCT390P PEL	5322 209 11483
D 3702	INTEGR CIRC OQ-0044	5322 209 11008
D 4001	HEF40106BP PEL	4822 209 10318
D 4002	HEF40106BP PEL	4822 209 10318
D 4003	HEF4070BP PEL	4822 209 10265
D 4004	HEF4070BP PEL	4822 209 10265
D 4006	HEF4082BP PEL	4822 209 10271
D 4007	HEF4070BP PEL	4822 209 10265
D 4008	HEF40106BP PEL	4822 209 10318
D 4009	PC74HCT374P PEL	5322 209 11119
D 4011	PC74HCT374P PEL	5322 209 11119
D 4012	PC74HCT374P PEL	5322 209 11119
D 4013	PC74HCT138P PEL	5322 209 11111
D 4014	HEF4073BP PEL	4822 209 10266
D 4016	HEF4013BP PEL	4822 209 10248
D 4017	HEF40106BP PEL	4822 209 10318
D 4201	PC74HCT4051P	5322 209 71662
D 4202	PC74HCT27P PEL	5322 209 11472
D 4203	SN74LS245N T.I	5322 209 86225
D 4204	PC74HCT138P PEL	5322 209 11111
D 4206	PC74HCT374P PEL	5322 209 11119
D 4207	PC74HCT374P PEL	5322 209 11119
D 5001	TEA1017/N8 PEL	5322 209 70023
D 5002	TEA1017/N8 PEL	5322 209 70023
D 5201	HF TRANS ARR OQ0127T	5322 209 72905
D 5202	HF MULTIPL OQ0146T	5322 209 71708
D 5203	HF MULTIPL OQ0146T	5322 209 71708
D 5204	HF TRANS ARR OQ0127T	5322 209 72905
D 5206	HF MULTIPL OQ0146T	5322 209 71708
D 5207	HF TRANS ARR OQ0127T	5322 209 72905
D 5208	HF TRANS ARR OQ0127T	5322 209 72905
D 5494	100114FC FSC	5322 209 73375
D 5496	100131FC FSC	5322 209 82939
D 5497	100131FC FSC	5322 209 82939
D 5498	100131FC FSC	5322 209 82939
D 5499	6XECL/TTL 100125FC	5322 209 73377
D 6001	TEA1017/N8 PEL	5322 209 70023
D 6002	TEA1017/N8 PEL	5322 209 70023
D 7001	HEF4053BP PEL	5322 209 10576
D 7002	PC74HCT4538P	4822 209 71585
D 7003	PC74HCT4538P	4822 209 71585

POSNR	DESCRIPTION		ORDERING CODE
N 0601	CA3086	RCA	5322 209 11225
N 0602	LM79L15ACZ	N.S	5322 209 82751
N 0603	LM78L15ACZ	N.S	4822 209 80889
N 0604	LM78L15ACZ	N.S	4822 209 80889
N 0606	LM337LZ	NSC	5322 209 83228
N 0606	ADC803CM	BBR	5322 209 71668
N 0607	LM317LZ	MOT	5322 209 82943
N 1301	MSA-0404	AVA	5322 130 42745
N 1302	MSA-0304	AVA	5322 209 73376
N 1303	MSA-0404	AVA	5322 130 42745
N 1304	MSA-0304	AVA	5322 209 73376
N 1306	MSA-0404	AVA	5322 130 42745
N 1307	MSA-0304	AVA	5322 209 73376
N 1311	UA741SC	FSC	5322 209 71669
N 1711	LM311N	NSC	5322 209 85503
N 2201	UA7805UC	FSC	5322 209 84841
N 2202	LM337LZ	NSC	5322 209 83228
N 2203	LM337T	N.S	5322 209 81236
N 2204	UA741TC	FSC	4822 209 80617
N 2301	DAC10FX	PMI	5322 209 71665
N 2302	DAC-08EP	PMI	5322 209 11253
N 2303	DAC10FX	PMI	5322 209 71665
N 2304	LM358N	N.S	4822 209 70672
N 2306	LM79L15ACZ	N.S	5322 209 82751
N 2307	LM79L05ACZ	NSC	5322 209 86434
N 2503	LM358N	N.S	4822 209 70672
N 2506	TL082CP	T.I	5322 209 86064
N 2507	LF398N	N.S	5322 209 83291
N 2508	LF398N	N.S	5322 209 83291
N 3127	AD7541AJN	AND	5322 209 11277
N 3128	AD7541AJN	AND	5322 209 11277
N 3129	HA3-2525-5	HAR	5322 209 71661
N 3131	HA3-2525-5	HAR	5322 209 71661
N 3132	LM79L12ACZ	NSC	5322 209 86435
N 3133	HA3-2525-5	HAR	5322 209 71661
N 3134	HA3-2525-5	HAR	5322 209 71661
N 3136	TDA1540P	PEL	4822 209 81453
N 3137	TDA1540P	PEL	4822 209 81453
N 3138	TDA1540P	PEL	4822 209 81453
N 3139	TDA1540P	PEL	4822 209 81453
N 3141	TDA1540P	PEL	4822 209 81453
N 3143	AD7541AJN	AND	5322 209 11277
N 3146	AD7541AJN	AND	5322 209 11277
N 3147	HA3-2525-5	HAR	5322 209 71661
N 3148	HA3-2525-5	HAR	5322 209 71661
N 3301	UA714TC	FSC	5322 209 70275
N 3302	UA714TC	FSC	5322 209 70275
N 3303	LM358N	N.S	4822 209 70672
N 3304	AD7541AJN	AND	5322 209 11277
N 3306	TDA1540P	PEL	4822 209 81453
N 3307	UA714TC	FSC	5322 209 70275
N 3308	UA714TC	FSC	5322 209 70275
N 3309	TDA1540P	PEL	4822 209 81453
N 3311	UA714TC	FSC	5322 209 70275
N 3312	UA714TC	FSC	5322 209 70275
N 3313	TDA1540P	PEL	4822 209 81453
N 3314	UA714TC	FSC	5322 209 70275
N 3316	UA714TC	FSC	5322 209 70275
N 3317	UA714TC	FSC	5322 209 70275
N 3318	UA714TC	FSC	5322 209 70275
N 3319	UA714TC	FSC	5322 209 70275
N 3321	LM337LZ	NSC	5322 209 83228
N 3322	LM79L05ACZ	NSC	5322 209 86434
N 3323	LM78L05ACZ	N.S	5322 209 80903
N 3701	LM78L15ACZ	N.S	4822 209 80889
N 3702	LM79L15ACZ	N.S	5322 209 82751
N 3703	LM317LZ	MOT	5322 209 82943
N 4401	LM358N	N.S	4822 209 70672
N 4601	UA324PC	FSC	5322 209 82561
N 4602	LM339AN	N.S	4822 209 80631
N 5001	LT1012CN8	L.T	5322 209 83584
N 5002	CA3096AE	RCA	5322 209 73374
N 5004	HA3-2525-5	HAR	5322 209 71661
N 5006	HA1-5320-5	HAR	5322 209 73378
N 5007	NE5514N	SIG	4822 209 81451
N 5008	LT1012CN8	L.T	5322 209 83584
N 5011	LM339AN	N.S	4822 209 80631
N 5012	LM393N	NSC	4822 209 80797
N 5013	AD7541AJN	AND	5322 209 11277
N 5014	HA3-2525-5	HAR	5322 209 71661
N 5499	LM337LZ	NSC	5322 209 83228
N 6001	LT1012CN8	L.T	5322 209 83584
N 6002	CA3096AE	RCA	5322 209 73374
N 6004	HA3-2525-5	HAR	5322 209 71661
N 6006	HA1-5320-5	HAR	5322 209 73378
N 6007	NE5514N	SIG	4822 209 81451
N 6008	LT1012CN8	L.T	5322 209 83584
N 6011	LM339AN	N.S	4822 209 80631
N 6012	LM393N	NSC	4822 209 80797
N 6013	AD7541AJN	AND	5322 209 11277
N 6014	HA3-2525-5	HAR	5322 209 71661
N 7001	HA3-2525-5	HAR	5322 209 71661
N 7002	LM78L05ACZ	N.S	5322 209 80903
N 7003	LM358N	N.S	4822 209 70672

MISCELLANEOUS

POSNR	DESCRIPTION		ORDERING CODE
E 0001	T13/4 28V 80MA		5322 134 40534
E 0002	T13/4 28V 80MA		5322 134 40534
E1-E2.	ILLUM LAMPUNIT+CABLE		5322 218 41033
F 1	FUSE 2.5A TZ		4822 253 30026
F 0001	2.5A TZ		4822 253 30026
G 1701	LOCO16.0	PEL	5322 216 61456
G 3701	SN74LS321N	T.I	5322 209 81679
G 3702	4000,000KHZ		4822 242 70668
H 1	LED COW54-VI		5322 130 32704
H 0001	COW54-6	PEL	5322 130 32704
H 4001	BPW22A-I	PEL	4822 130 41541
H 4002	CQY58A	PEL	5322 130 31643
H 4003	CQY58A	PEL	5322 130 31643
H 4004	BPW22A-I	PEL	4822 130 41541
H 4006	BPW22A-I	PEL	4822 130 41541
H 4007	CQY58A	PEL	5322 130 31643
H 4008	CQY58A	PEL	5322 130 31643
H 4009	BPW22A-I	PEL	4822 130 41541
H 4011	BPW22A-I	PEL	4822 130 41541
H 4012	CQY58A	PEL	5322 130 31643
H 4013	CQY58A	PEL	5322 130 31643
H 4014	BPW22A-I	PEL	4822 130 41541
H 4016	BPW22A-I	PEL	4822 130 41541
H 4017	CQY58A	PEL	5322 130 31643
H 4018	CQY58A	PEL	5322 130 31643
H 4019	BPW22A-I	PEL	4822 130 41541
H 4021	BPW22A-I	PEL	4822 130 41541
H 4022	CQY58A	PEL	5322 130 31643
H 4023	CQY58A	PEL	5322 130 31643
H 4024	BPW22A-I	PEL	4822 130 41541
H 4026	BPW22A-I	PEL	4822 130 41541
H 4027	CQY58A	PEL	5322 130 31643
H 4028	CQY58A	PEL	5322 130 31643
H 4029	BPW22A-I	PEL	4822 130 41541
H 4031	BPW22A-I	PEL	4822 130 41541
H 4032	CQY58A	PEL	5322 130 31643
H 4033	CQY58A	PEL	5322 130 31643
H 4034	BPW22A-I	PEL	4822 130 41541
H 4036	BPW22A-I	PEL	4822 130 41541
H 4037	CQY58A	PEL	5322 130 31643
H 4038	CQY58A	PEL	5322 130 31643
H 4039	BPW22A-I	PEL	4822 130 41541
H 4041	BPW22A-I	PEL	4822 130 41541
H 4042	CQY58A	PEL	5322 130 31643
H 4043	CQY58A	PEL	5322 130 31643
H 4044	BPW22A-I	PEL	4822 130 41541
H 4046	BPW22A-I	PEL	4822 130 41541
H 4047	CQY58A	PEL	5322 130 31643
H 4048	CQY58A	PEL	5322 130 31643
H 4049	BPW22A-I	PEL	4822 130 41541
H 4051	BPW22A-I	PEL	4822 130 41541
H 4052	CQY58A	PEL	5322 130 31643
H 4053	CQY58A	PEL	5322 130 31643
H 4054	BPW22A-I	PEL	4822 130 41541
H 4201	CQY54A-2	PEL	5322 130 80547
H 4202	CQY54A-2	PEL	5322 130 80547
H 4203	CQY54A-2	PEL	5322 130 80547
H 4204	CQY54A-2	PEL	5322 130 80547
H 4206	CQY54A-2	PEL	5322 130 80547
H 4207	CQY54A-2	PEL	5322 130 80547
H 4208	CQY54A-2	PEL	5322 130 80547
H 4401	CNX35	PEL	5322 130 90137
K 3301	360E 5-15DC		5322 280 24046
K 3302	360E 5-15DC		5322 280 24046
K 3303	360E 5-15DC		5322 280 24046
K 3304	360E 5-15DC		5322 280 24046
K 3306	360E 5-15DC		5322 280 24046
K 5001	EED-RELAIS 12V		5322 280 20125
K 5002	EED-RELAIS 12V		5322 280 20125
K 5003	EED-RELAIS 12V		5322 280 20125
K 6001	EED-RELAIS 12V		5322 280 20125
K 6002	EED-RELAIS 12V		5322 280 20125
K 6003	EED-RELAIS 12V		5322 280 20125
L 0019	KE 2X1.2MH 4A		5322 219 81131
L 1201	2.2UH	TDK	4822 157 51757
L 1301	COIL ASSY		5322 157 53597
L 1302	82UH		4822 158 10563
L 1303	COIL ASSY		5322 157 53597
L 1304	COIL ASSY		5322 157 53597
L 1306	COIL ASSY		5322 157 53597
L 1307	COIL ASSY		5322 157 53597
L 1308	COIL ASSY		5322 157 53596
L 1309	COIL ASSY		5322 157 53596
L 1311	COIL ASSY		5322 157 53596
L 1312	COIL ASSY		5322 157 53596
L 1401	2.2UH	TDK	4822 157 51757
L 1701	2.2UH	TDK	4822 157 51757

POSNR	DESCRIPTION		ORDERING CODE
L 1702	2.2UH	TDK	4822 157 51757
L 1703	2.2UH	TDK	4822 157 51757
L 3301	82UH		4822 158 10563
L 3701	82UH		4822 158 10563
L 3702	82UH		4822 158 10563
L 3703	82UH		4822 158 10563
L 3704	82UH		4822 158 10563
L 3706	82UH		4822 158 10563
L 3707	82UH		4822 158 10563
L 3708	82UH		4822 158 10563
L 3709	82UH		4822 158 10563
L 3711	82UH		4822 158 10563
L 3712	82UH		4822 158 10563
L 3714	82UH		4822 158 10563
L 3716	82UH		4822 158 10563
L 3718	82UH		4822 158 10563
L 3719	82UH		4822 158 10563
L 3721	82UH		4822 158 10563
L 3722	82UH		4822 158 10563
L 3723	82UH		4822 158 10563
L 3724	82UH		4822 158 10563
L 3726	82UH		4822 158 10563
L 3727	82UH		4822 158 10563
L 3728	82UH		4822 158 10563
L 4401	2X2,5MH 2,5A		5322 157 53346
L 4402	47UH	TDK	4822 152 10106
L 4403	47UH	TDK	4822 152 10106
L 4404	5.6UH		4822 157 52259
L 4408	L		5322 157 53376
L 4411	3.3UH	TDK	5322 157 53017
L 4412	3.3UH	TDK	5322 157 53017
L 4414	10UH	TDK	5322 157 52913
L 4416	22UH	TDK	5322 157 52707
L 4417	22UH	TDK	5322 157 52707
L 4418	22UH	TDK	5322 157 52707
L 4419	22UH	TDK	5322 157 52707
L 4421	10UH	TDK	5322 157 53016
L 4423	10UH	TDK	5322 157 53016
L 4424	82UH		4822 158 10563
L 4426	10UH	TDK	5322 157 53016
L 4601	1500UH	TDK	5322 157 53018
L 4602	0.01H	TDK	5322 157 53019
L 4603	82UH		4822 158 10563
L 4604	82UH		4822 158 10563
L 5003	1500UH	TDK	4822 156 21293
L 5004	1500UH	TDK	4822 156 21293
L 5005	2.2UH	TDK	4822 157 51757
L 5201	1500UH	TDK	4822 156 21293
L 5202	15UH		5322 157 52939
L 5203	82UH		4822 158 10563
L 6003	1500UH	TDK	4822 156 21293
L 6004	1500UH	TDK	4822 156 21293
L 6005	2.2UH	TDK	4822 157 51757
M 1	FAN		5322 361 10453
M 0001			5322 361 10453
S 1	POWER ON SWITCH		5322 276 11859
S 0001	AAR 70060-007		5322 276 12411
S 0002	2-P MET LED		5322 276 11459
S 0003	2-P MET LED		5322 276 11459
S 0004			5322 276 14338
S 0005			5322 276 14338
S 0006			5322 276 14338
S 0007			5322 276 14338
S 0008			5322 276 14338
S 0009			5322 276 14338
S 0010			5322 276 14338
S 0011			5322 276 14338
S 4216			5322 276 14338
S 4217			5322 276 14338
S 4218			5322 276 14338
S 4219			5322 276 14338
S 4221			5322 276 14338
S 4222			5322 276 14338
S 4223			5322 276 14338
S 4224			5322 276 14338
S 4226			5322 276 14338
S 4227			5322 276 14338
S 4228			5322 276 14338
S 4229			5322 276 14338
S 4231	2-P MET LED		5322 276 11459
S 4232			5322 276 11856
S 4233	2-P MET LED		5322 276 11459
S 4234	2-P MET LED		5322 276 11459
S 4236			5322 276 11856
S 4237	2-P MET LED		5322 276 11459
S 4238	BR		5322 277 10878
S 4239	BR		5322 277 10878
S 4241	BR		5322 277 10878
S 5002	1-P	TS2	5322 277 24045
S 5003	1-P	TS2	5322 277 24045
S 6002	1-P	TS2	5322 277 24045
S 6003	1-P	TS2	5322 277 24045

POSNR	DESCRIPTION	ORDERING CODE
T 3501	PULSE TRANSFORMER	5322 142 60403
T 5001	PULSE TRANSFORMER	5322 142 60404
T 6001	PULSE TRANSFORMER	5322 142 60404
X 1	CAL BNL OUTPUT SOCK	5322 267 10004
X 17	PLOT OUTPUT SOCKET	4822 267 40039
X 19	POWER INLET + FUSEH.	5322 265 20353
X 0001	SOCKET	5322 267 10191
X 0017	5-P 4A	4822 267 40039
X 0101	10-P DBL RT.ANG	5322 265 51188
X 0103	4-P SNG RT.ANG	5322 265 30533
X 0104	5-P SNG RT.ANG	5322 265 30529
X 0106	10-P DBL RT.ANG	5322 265 51188
X 0501	64-P RGHT ANGL	5322 265 61124
X 0502	64-P SKT 2.54	5322 267 70233
X 0503	64-P SKT 2.54	5322 267 70233
X 0504	96-P BUS A-B-C	5322 267 70234
X 0506	96-P BUS A-B-C	5322 267 70234
X 0507	96-P BUS A-B-C	5322 267 70234
X 0508	96-P BUS A-B-C	5322 267 70234
X 0509	96-P BUS A-B-C	5322 267 70234
X 0511	64-P SKT 2.54	5322 267 70233
X 0512	96-P BUS A-B-C	5322 267 70234
X 0513	96-P BUS A-B-C	5322 267 70234
X 0514	64-P SKT 2.54	5322 267 70233
X 0516	96-P BUS A-B-C	5322 267 70234
X 0517	64-P SKT 2.54	5322 267 70233
X 0518	96-P BUS A-B-C	5322 267 70234
X 0519	64-P SKT 2.54	5322 267 70233
X 0521	96-P BUS A-B-C	5322 267 70234
X 0522	64-P SKT 2.54	5322 267 70233
X 0523	96-P BUS A-B-C	5322 267 70234
X 0524	64-P SKT 2.54	5322 267 70233
X 0526	P RECHT QF50	5322 265 51185
X 0527	P RECHT QF50	5322 265 51185
X 0528	4-P SNG STRGHT	5322 265 30534
X 0607	64-P PIN 2.54MM	5322 265 61146
X 0609	3-P SNG 2.54	5322 265 30392
X 0609	2-P	5322 263 60062
X 0901	5P DBL ST11MM	5322 265 30629
X 0902	5P DBL ST11MM	5322 265 30629
X 0903	5P DBL ST11MM	5322 265 30629
X 0904	21 SMA-50-0-52	5322 263 21007
X 0906	21 SMA-50-0-52	5322 263 21007
X 1201	64-P PIN 2.54MM	5322 265 61146
X 1202	64-P PIN 2.54MM	5322 265 61146
X 1301	7-P DBL 2.54	5322 265 40559
X 1401	96-P PIN 2.54	5322 265 61147
X 1402	64-P PIN 2.54MM	5322 265 61146
X 1501	10-P DBL STRGHT	5322 265 40485
X 1502	4-P SNG STRGHT	5322 265 30474
X 1503	3-P SNG RT.ANG	5322 265 30433
X 1504	55595 PEL	5322 255 40502
X 1504	CRT SOCKET	5322 255 40502
X 1701	96-P PIN 2.54	5322 265 61147
X 1702	10-P DBL RT.ANG	5322 265 51188
X 1703	3-P SNG 2.54	5322 265 30392
X 1703	2-P	5322 263 60062
X 1704	3-P SNG 2.54	5322 265 30392
X 1704	2-P	5322 263 60062
X 1706	3-P SNG 2.54	5322 265 30392
X 1706	2-P	5322 263 60062
X 1707	3-P SNG 2.54	5322 265 30392
X 1707	2-P	5322 263 60062
X 1716	2-P SNG 2.54	5322 265 20266
X 1716	2-P	5322 263 60062
X 1801	96-P PEN 2.54	5322 265 61029
X 1802	64-P PEN 2.54	5322 265 61025
X 2001	96-P PIN 2.54	5322 265 61147
X 2002	96-P PIN 2.54	5322 265 61147
X 2101	96-P PIN 2.54	5322 265 61147
X 2102	96-P PIN 2.54	5322 265 61147
X 2301	64-P PIN 2.54MM	5322 265 61146
X 2302	64-P PIN 2.54MM	5322 265 61146
X 2501	64-P PIN 2.54MM	5322 265 61146
X 3001	3-P SNG RT.ANG	5322 265 30433
X 3002	4-P SNG RT.ANG	5322 265 30533
X 3003	10-P DBL RT.ANG	5322 265 51188
X 3004	16-P DBL RT.ANG	5322 265 61119
X 3051	16-P DBL STRGHT	5322 265 61117
X 3101	64-P RGHT ANGL	5322 265 61124
X 3102	40-P DBL STRGHT	5322 265 61072
X 3301	2-P SNG 2.54	5322 265 20266
X 3301	2-P	5322 263 60062
X 3306	16-P DBL STRGHT	5322 265 61117
X 3307	34-P DBL STRGHT	5322 265 61069
X 3308	10-P SNG 2.54	5322 267 50836
X 3309	15-P SNG 2.54	5322 267 50837
X 3311	7-P SNG 2.54	5322 267 50835
X 3312	6-P SNG 2.54	5322 267 40796
X 3509	15-P SNG 2.54	5322 265 40735
X 3511	7-P SNG 2.54	5322 265 40736

POSNR	DESCRIPTION	ORDERING CODE
X 3512	6-P SNG 2.54	5322 265 30472
X 3701	40-P DBL STRGHT	5322 265 61072
X 3702	64-P PEN 2.54	5322 265 61025
X 3703	40-P DBL STRGHT	5322 265 61072
X 3704	34-P DBL STRGHT	5322 265 61069
X 4001	20-P DBL RT.ANG	5322 265 61121
X 4201	20-P DBL STRGHT	5322 265 51129
X 4202	16-P DBL RT.ANG	5322 265 61119
X 4401	5-P SNG STRGHT	5322 265 30436
X 4402	3-P SNG STRGHT	5322 265 30434
X 4403	50-P DBL STRGHT	5322 265 61123
X 4404	4-P SNG STRGHT	5322 265 30534
X 4406	20-P DBL STRGHT	5322 265 51129
X 4601	3-P SNG STRGHT	5322 265 30434
X 4602	3-P SNG STRGHT	5322 265 30434
X 4603	3-P SNG STRGHT	5322 265 30434
X 4604	64-P BUS 2.54	5322 267 74092
X 4606	50-P DBL STRGHT	5322 265 61123
X 5001	5P DBL ST10.2MM	5322 267 40797
X 5201	16-P DBL STRGHT	5322 265 61117
X 6001	5P DBL ST10.2MM	5322 267 40797
X 7001	5P DBL ST10.2MM	5322 267 40797
X 7002	40-P DBL STRGHT	5322 265 61072
X 7003	2-P SNG STRGHT	5322 265 20275
X 7004	8-P SNG 2.54	5322 267 50834
X 7004	10-P SNG 2.54	5322 267 50836
X 7006	8-P SNG 2.54	5322 267 50834
X 7006	10-P SNG 2.54	5322 267 50836
X2-X3.	N INPUT SOCKET	5322 263 21009

ACCESSORY INFORMATION

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16.0 ACCESSORY INFORMATION

16.1 ACCESSORIES SUPPLIED WITH THE INSTRUMENT

16.1.1 Passive probe with automatic range indication

For operating or service information refer to the separate booklet, supplied with the probes.

16.1.2 Blue contrast filter

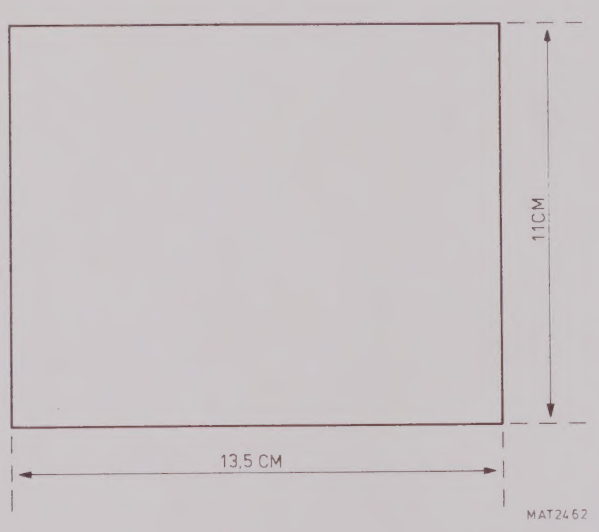

Figure 16.9 Blue contrast filter. (Factory installed !)

16.1.3 Front cover

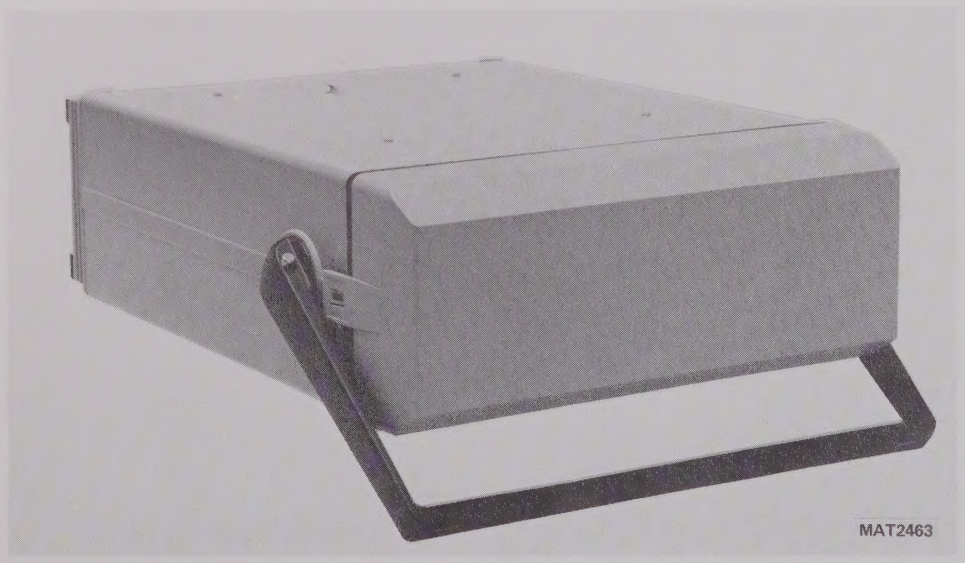

Figure 16.10 Oscilloscope with front cover.

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